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Impact of Temperature and Switching Rate on Properties of Crosstalk on Symmetrical & Asymmetrical Double-trench SiC Power MOSFET

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Abstract—In this paper, the properties of crosstalk on SiC planar MOSFET, SiC symmetrical double-trench MOSFET and SiC asymmetrical double-trench MOSFET is investigated on a half-bridge topology, to enable analysis of the impact of temperature, drain-source transition speed and gate resistance on the severity of the shoot-through current and induced gate voltage. The experimental measurements, performed on a wide range of temperatures and switching rates, show that the two selected symmetrical and asymmetrical double-trench MOSFETs exhibit higher induced gate voltage during crosstalk with the same external gate resistance compared with the planar SiC MOSFET, yielding a higher shoot-through current. Therefore, in continuous initiation of intentional crosstalk, the two double-trench MOSFETs experience more temperature rise, especially for symmetrical one which leads the device to verge of failure within minutes while the temperature rise in other two devices is significantly lower. The different trends of shoot-through current with temperature on DUTs reveals that they are dominated by different mechanisms, i.e., influenced by threshold voltage and inversion layer carriers' mobility. A model is developed for prediction of shoot-through current during crosstalk which is validated for the 3 device structures. The comparison of the modelled results with the measurement proves its capability to predict the crosstalk behaviour.

Index Terms—Crosstalk, Silicon Carbide, Double-trench, MOSFET

I. INTRODUCTION

With the introduction of SiC technology as a replacement of Silicon MOSFETs, better performance is achieved in a wide range of industrial application. One of the main advantages of SiC MOSFETs is its smaller die size which enables fast switching. Therefore, the switching loss is minimized along with smaller passive filter required for application. However,

in half bridge arrangements, the high drain-source voltage switching rate would cause crosstalk on the complementary device. During the turn-ON process, positive gate voltage is induced on the complementary device by current flowing through gate-drain capacitance and gate resistance thus initiates parasitic turn-ON and shoot-through current. Therefore, the selection of gate resistance requires consideration of the trade-off between switching rate and the likelihood of parasitic turn-ON. This undesired effect has the MOSFET operating in semi-short-circuit and results in significant thermal loss as well as electrothermal stress which arises reliability concerns. Research is performed to evaluate crosstalk on planar SiC power MOSFETs [1], [2] & [3], but symmetrical and asymmetrical double-trench structures still remain largely unexplored.

In this paper, a model is developed for predicting the shoot-through current during crosstalk, the performance at crosstalk is compared for three devices of similar power rating with different structures under different switching rate, ambient temperature and gate resistance. Their cross-sectional schematic drawing is shown in Fig. 1 as planar structure, symmetrical double-trench structure and asymmetric double-trench structure. Compared with conventional planar structure, symmetrical double-trench removes the JFET region which enables high channel-density design. Asymmetrical double-trench structure further removes the JFET between the gate and source trench thus allows more unit cell scaling-down than symmetrical one [4].

II. MODELING OF CROSSTALK

The modeling for SiC MOSFET during crosstalk has been introduced in [1], [5] & [6] by considering the displacement current flowing through reverse transfer capacitance C_{GD} and

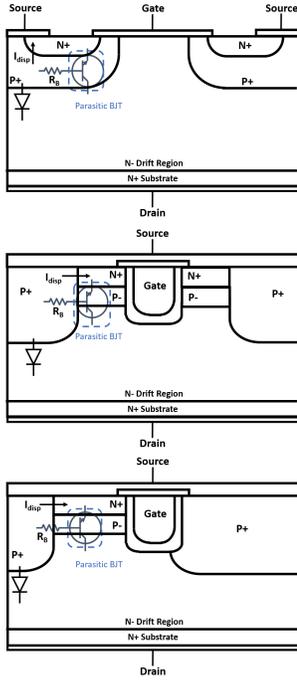


Fig. 1. Cross-sectional schematics of SiC planar MOSFET, symmetrical SiC double-trench MOSFET and SiC asymmetrical double-trench MOSFET.

gate resistance R_G , thus a positive gate voltage is induced and would result in parasitic turn-ON. However, these models ignore the impact of shoot-through current incorporating the parasitic inductance on the power loop, and therefore, are unable to predict the peak shoot-through on the device. In this paper, a model for crosstalk is developed with shoot-through current considered.

The crosstalk can be divided into two stages. The first stage is when the induced gate voltage has not exceeded the threshold value, that is, no shoot-through current occurs and there is only displacement current flowing in the device. The second stage is when the induced gate voltage reaches the threshold value and MOSFET channel is parasitically turned-ON. The MOSFET at this stage is operating at saturation region. The equivalent circuit for these two stages are presented in Fig. 2 where drain, source and gate are represented as D, S and G respectively. In both cases, the drain-source capacitance C_{DS} is omitted as a result of small die area of SiC MOSFET [7], yielding rather small displacement current through it. The voltage source V_{Ramp} represents the voltage transition over the DUT initiated by the turn-ON of top device, expressed as:

$$V_{Ramp} = K * t \quad (1)$$

Where K is the slew rate until reaching the supply voltage.

During the first stage. Since the shoot-through is not happening, the parasitic inductances on the power loop is neglected for simplification. According to [3] [4], the induced gate voltage has been calculated as

$$V_{GS} = R_G \cdot C_{GD} \cdot K(1 - e^{-\frac{t}{R_G \cdot C_{GD}}}) \quad (2)$$

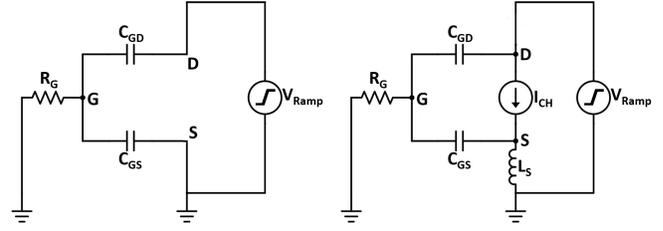


Fig. 2. Equivalent circuit of crosstalk at (L) first stage, and (R) second stage.

In the second stage, with the increase of induced gate voltage above threshold, a current source representing the MOSFET channel is added to the equivalent circuit as well as the parasitic inductances which produce voltage under channel conduction. Parasitic inductance at drain is neglected since it is shown to have small impact on the induced gate voltage than that at source [5]. The equation for the current source of MOSFET channel is given as:

$$I_{CH} = g_{fs} * (V_{GS} - V_{TH}) \quad (3)$$

where g_{fs} is the device transconductance. At this stage, the gate voltage V_G has an initial value of V_{TH} , therefore, can be written as:

$$V_G = V'_G + V_{TH} \quad (4)$$

Where V'_G is the variation of V_G during the second stage. It is assumed that $\frac{dV'_G}{dt}(0)$ and $V_{Ramp}(0)$ are equal to zero. C_{GD} at high voltage is used here as a constant since it decreases fast with voltage increase. Hence, equations can be written for the equivalent circuit as:

$$V_D = V_{Ramp} \quad (5)$$

$$C_{GD} \frac{d(V_D - V_G)}{dt} = \frac{V_G}{R_G} + C_{GS} \frac{d(V_G - V_S)}{dt} \quad (6)$$

$$V_S = L_S \frac{dI_S}{dt} \quad (7)$$

$$I_S = I_{CH} + C_{GS} \frac{d(V_G - V_S)}{dt} \quad (8)$$

To simplify the calculation, V_G in the term $\frac{V_G}{R_G}$ in (6) is assumed to be dominated by V'_G . Then, by performing Laplace transform, the solution for V_G can be derived as:

$$V'_G(s) = \frac{N_1 s^3 + N_2 s}{D_1 s^3 + D_2 s^2 + D_3 s + 1} * \frac{K}{s^2} \quad (9)$$

Where the coefficients for the numerator and denominator are expressed as:

$$N_1 = C_{GD} * R_G * L_S * C_{GS}$$

$$N_2 = C_{GD} * R_G$$

and

$$D_1 = (C_{GS} + C_{GD}) * R_G * L_S * C_{GS} - L_{GS} C_{GS}^2$$

$$D_2 = L_{GS}C_{GS} - L_{GS}C_{GS} * g_{fs}$$

$$D_3 = (C_{GS} + C_{GD}) * R_G$$

By doing this, the induced gate voltage and peak shoot-through current can be predicted for the three DUTs. The peak values of shoot-through current are extracted from model and measurement for three different structured MOSFETs are plotted in Fig. 3 for the case of top gate resistance R_{G_Top} and bottom gate resistance R_{G_Bot} equal to 47 Ω and 330 Ω respectively and good matching between them can be observed.

III. EXPERIMENTAL SETUP

Experimental measurement are carried out on Rohm SiC planar MOSFET, Rohm SiC symmetrical double-trench MOSFET and Infineon asymmetrical double-trench MOSFET. The test circuit is shown in Fig. 4 with its schematic which is a half-bridge. The top switching device is fixed to make a fair comparison for DUTs placed at bottom. A single pulse from 18V/0V gate driver is fed to top switching device so that the full supply voltage V_{DD} falls on DUT at bottom and initiates crosstalk. R_{G_Top} ranges from 10 Ω to 100 Ω for different switching speed while R_{G_Bot} ranges from 10 Ω to 330 Ω to achieve different shoot-through current level. The shoot-through current is measured at the source of DUT with CWT Ultra-mini Rogowski coil (CWT1) and voltage is measured with GW-Instek GDP-100 100 MHz voltage probe on a

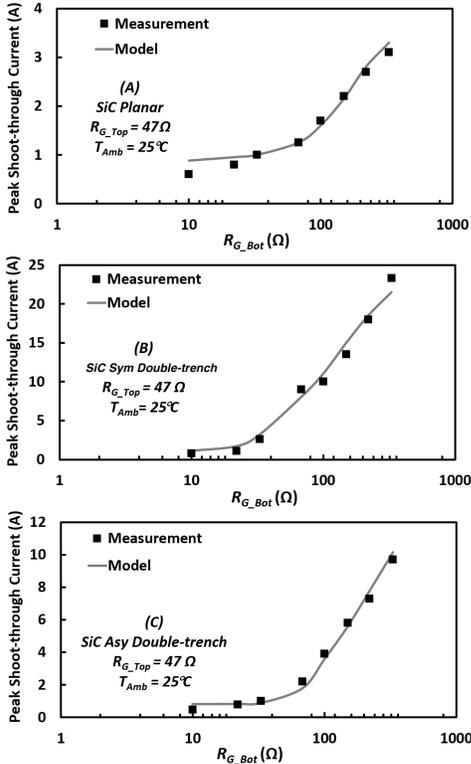


Fig. 3. Modelling of crosstalk shoot-through current, compared with measurements of SiC planar, symmetric & asymmetric double-trench MOSFETs.

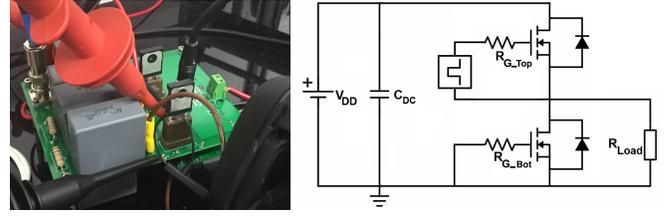


Fig. 4. Testing set-up and its schematic for crosstalk measurements.

TABLE I
MEASUREMENT BOARD COMPONENTS.

Parameter	Symbol	Value
DC Capacitor	C_{DC}	9.4 μF
Load Resistor	R_{Load}	2000 Ω
Voltage	V_{DD}	800 V
Ambient Temperature Range	T_{Amb}	25-175 $^{\circ}\text{C}$
Top Gate Resistance Range	R_{G_Top}	10-100 Ω
Bottom Gate Resistance Range	R_{G_Bot}	10-330 Ω

TABLE II
KEY DEVICE PARAMETERS OF THE THREE DUTS.

	4H-SiC	4H-SiC	4H-SiC
Model	SCT2160	SCT3160	IMW120R140M1H
Make	Rohm	Rohm	Infineon
Structure	Planar	Sym-DT	Asym-DT
Voltage Rating (V)	1200	1200	1200
Current Rating (A)	22	17	19
C_{GS} (pF) @ $V = 0$ V	2355	744	622
C_{GD} (pF) @ $V = 0$ V	1324	344	121
R_{G-int} (Ω)	13.7	18	14
$R_{TH(jc)}$ (K/W)	0.7	1.12	1.2

Keysight MSO7104A 1 GHz 4 GSa/s oscilloscope. Ambient temperature on DUTs is varied from 25 $^{\circ}\text{C}$ to 175 $^{\circ}\text{C}$ by using a heating block controlled with a PID temperature controller. Table.I indicates the key parameters for the testing board and experiment conditions and Table.II shows key parameters of three selected DUTs from datasheet and measured parasitic capacitance at 1 MHz.

IV. MEASUREMENT AND ANALYSIS

A. Impact of Bottom Gate Resistance

Fig. 5 compares the peak value of shoot-through current on each DUT with different value of R_{G_Bot} with ambient temperature fixed at 25 $^{\circ}\text{C}$ and R_{G_Top} at 47 Ω while Fig. 6 shows the transient waveforms. It can be seen that as R_{G_Bot} increases, SiC symmetrical double-trench MOSFET experiences the most significant rise in shoot-through current followed by SiC asymmetric double-trench MOSFET and the least change in SiC planar MOSFET. The general increasing trend of shoot-through current with R_{G_Bot} is due to the induced gate voltage

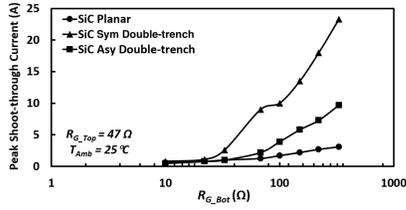


Fig. 5. Peak shoot-through current at a range of R_{G_Bot} in the 3 device structures.

raised by the displacement current via C_{GD} coupled with the increased overall impedance of R_{G_Bot} in parallel with C_{GS} . High induced gate voltage allows the channel to conduct more current with DUT operating in saturation region. The variation level of the induced gate voltage is affected by C_{GS} of device. With larger C_{GS} , the overall impedance of R_{G_Bot} in parallel with C_{GS} would be more dominated by C_{GS} since it behaves as a path of lower impedance at high frequency in such parallel circuit. Therefore, as indicated in Table.II, the high C_{GS} grants planar MOSFET low sensitivity of induced gate voltage to R_{G_Bot} whereas low C_{GS} gives two double-trench MOSFETs higher sensitivity and thereby shoot-through current. Since oscillations occur on the measurement of gate voltage, peak induced gate voltage is not representative enough for characterization. Transient gate voltage waveform for three DUTs are plotted in Fig. 7 for a specific case with R_{G_Top} and R_{G_Bot} equal to 47Ω and 330Ω respectively under $25^\circ C$, R_{G_Bot} is intentionally chosen to be large to amplify the difference of DUT characteristic. The impact of the induced gate voltage on shoot-through current on the 3 device technologies is clear in Fig. 8. It shows that the induced gate voltage is the highest for SiC symmetrical double-trench followed by asymmetrical double-trench MOSFET and planar being the smallest despite more serious oscillations showing up on planar MOSFET. The reason for the lower induced gate voltage of asymmetrical double-trench MOSFET compared with symmetrical double-trench one can be attributed to its structure which intrinsically features low C_{GD} [8].

Another consideration is that with the increase of R_{G_Bot} , the actual dV_{DS}/dt occur on DUT is slowed down due to more current drawn to channel from C_{DS} . This phenomenon is the most noticeable on SiC double-trench MOSFET, as shown in Fig. 9 due to its large shoot-through current.

B. Impact of Top Gate Resistance

Fig. 10 shows the shoot-through current of each DUT under different switching rate by replacing R_{G_Top} at $25^\circ C$. In this case, R_{G_Bot} is selected to be 330Ω so that there is significant shoot-through to exaggerate the impact of R_{G_Top} . The shoot-through current experiences decrease as R_{G_Top} increases, because low switching rate generates less displacement current through C_{GD} of DUT for a reduced induced gate voltage. As already indicated in Fig. 9, the actual dV_{DS}/dt on DUT is not only controlled by R_{G_Top} but also affected by DUT itself. The peak shoot-through current on each DUT is normalized and given on Fig. 11 against R_{G_Top} at both case R_{G_Bot} equal to 330Ω and 150Ω . It can be seen that SiC symmet-

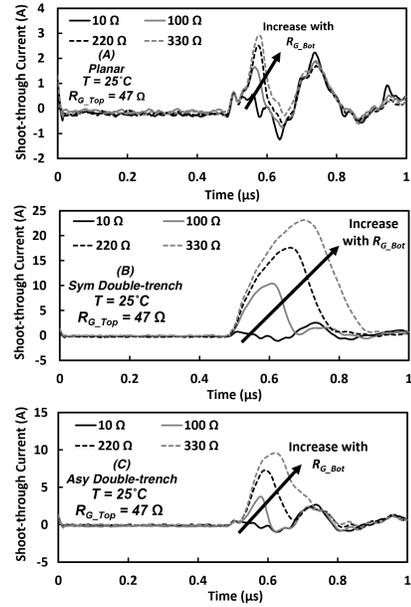


Fig. 6. Transient shoot-through current at a range of R_{G_Bot} for (a) SiC planar MOSFET (b) SiC symmetrical double-trench MOSFET (c) SiC asymmetrical double-trench MOSFET.

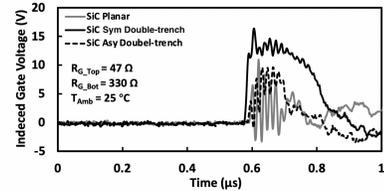


Fig. 7. Induced gate voltage in the 3 device structures with R_{G_Bot} of 330Ω under identical test conditions.

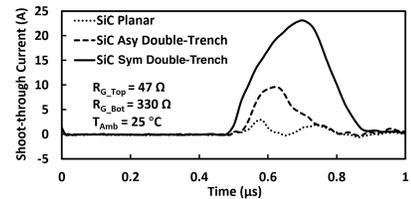


Fig. 8. Shoot-through current in the 3 device structures with R_{G_Bot} of 330Ω under identical test conditions.

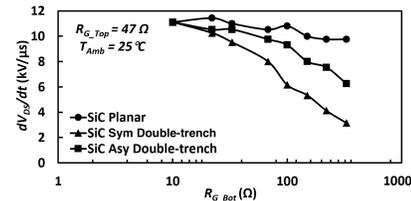


Fig. 9. dV_{DS}/dt in the 3 device structures at a range of R_{G_Bot} .

rical double-trench MOSFET is the one that has the lowest sensitivity to R_{G_Top} , though this dependence is enhanced if its R_{G_Bot} is reduced. This is because that the highest shoot-

through current on SiC symmetrical double-trench MOSFET minimizes change of dV_{DS}/dt on it at increasing R_{G_Top} . Due to fairly low shoot-through current, SiC asymmetrical double-trench MOSFET and planar MOSFET maintains good sensitivity to R_{G_Top} in terms of peak shoot-through current.

C. Impact of Temperature

Silicon Carbide has superior thermal conductivity to Silicon, making SiC MOSFET good candidate for harsh working condition. The peak shoot-through current for three DUTs is plotted in Fig. 12 against temperature with R_{G_Bot} equal to 330 Ω and 10 Ω . When R_{G_Bot} is 330 Ω , three devices shows three different trend regarding to the temperature increase in peak shoot-through current. SiC planar MOSFET has increased shoot-through with temperature while it is opposite for SiC symmetrical double-trench MOSFET, and SiC

asymmetric double-trench MOSFET is nearly constant at all temperature. Since during shoot-through, MOSFET is under saturation region operation. The shoot-through current I_{ST} is approximated to MOSFET channel current and subject to (3). By expanding g_{fs} in (3), it yields:

$$I_{ST} = \frac{Z_{CH}\mu_n C_{OX}}{L_{CH}}(V_{GS} - V_{TH})^2 \quad (10)$$

where Z_{CH} & L_{CH} are channel width & length, C_{OX} is specific oxide capacitance and μ_n is the inversion carrier mobility.

According to (10), the parameters that have temperature-dependence are the channel mobility μ_n and the threshold voltage V_{TH} . It is commonly known that high temperature raises intrinsic carrier density thus reduces V_{TH} [9], as shown in the Fig. 13. The change of V_{TH} would enhance the shoot-through at high temperature. However, the mobility μ_n acts adversely on shoot-through due to the more pronounced scattering at high temperature [9], [10]. Therefore, It can be revealed that, with R_{G_Bot} equal to 330 Ω , μ_n acts as a more dominated factor to shoot-through in SiC double-trench MOSFET whereas it is V_{TH} in SiC planar MOSFET, these two mechanisms almost balance each other out in SiC asymmetric double-trench MOSFET. According to (10), the higher the V_{GS} is, the less impact the V_{TH} has on the term $(V_{GS} - V_{TH})$. Referring to Fig. 7, V_{TH} is more dominant in SiC planar MOSFET with the lowest induced gate voltage, while asymmetric and symmetric double-trench MOSFET have the impact of μ_n comparable to or even outweigh the impact of V_{TH} as a consequence of raised induced gate voltage. This suggests that the SiC double-trench MOSFET will not have thermal runaway despite high shoot-through current. With the R_{G_Bot} reduced to 10 Ω , induced gate voltage is effectively damped. Therefore, all DUTs are exhibiting an increasing shoot-through in regard to temperature increase as shown in Fig. 12.

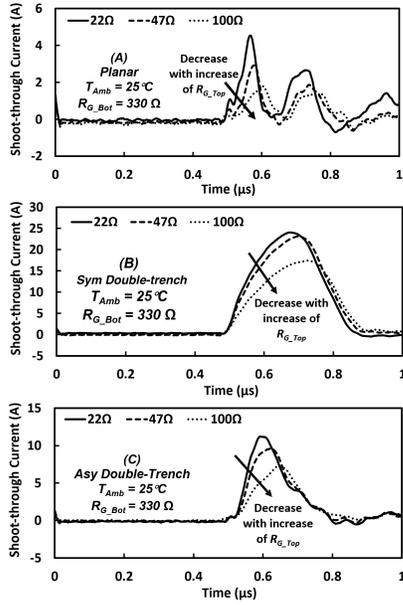


Fig. 10. Transient shoot-through current at a range of R_{G_Top} for (a) SiC planar MOSFET (b) SiC symmetrical double-trench MOSFET (c) SiC asymmetrical double-trench MOSFET.

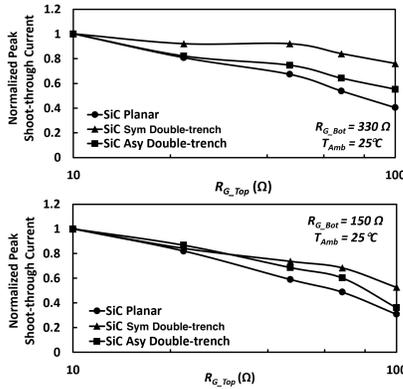


Fig. 11. Normalized peak shoot-through current at a range of R_{G_Top} in the 3 device structures with R_{G_Bot} of 330 Ω and 150 Ω .

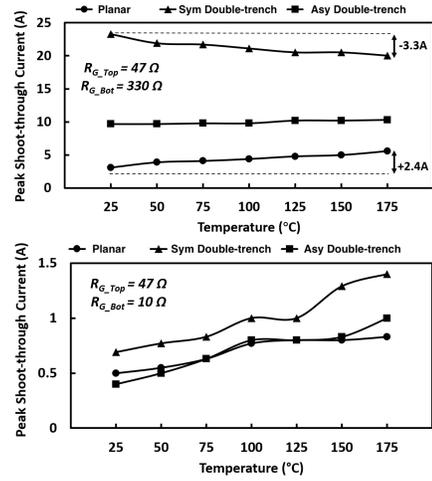


Fig. 12. Peak shoot-through current at a range of temperature in the 3 device structures with R_{G_Bot} of 330 Ω and 10 Ω .

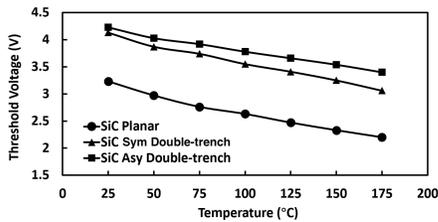


Fig. 13. Threshold voltage against temperature in the 3 device structures measured at $V_{GS} = V_{DS}, I_{DS} = 4 \text{ mA}$.

D. Continuous Switching

One concern for crosstalk on MOSFET is the heat generated while operating in such short-circuit circumstance, so that the device would soon work above the allowed temperature. Three DUTs are driven continuously at 1 kHz, supply voltage equal to 600 V, room temperature and the temperature rise is recorded using FLIR-63900 thermal camera. The gate resistance is chosen to be $2 \text{ k}\Omega$ to amplify the impact of different device characteristics. The results is plotted on Fig. 14 and thermal image corresponding to the highest captured temperature is shown in Fig. 15. It shows that compared with soaring to nearly 160°C within 2 minute for symmetrical double-trench MOSFET, planar and asymmetrical double-trench MOSFET, after a small rise initially, maintain stably at low temperature though asymmetrical double-trench MOSFET is still higher than planar.

V. CONCLUSION

The crosstalk behaviour for planar and two double-trench structured SiC MOSFETs has been modeled and experimentally measured. Higher gate voltage is induced at crosstalk for two double-trench structured MOSFETs and thereby higher shoot-through current compared with the selected planar MOSFET. Such high induced gate voltage potentially amplifies the impact of channel mobility on shoot-through current at increasing temperature, so that symmetrical double-trench and asymmetrical double-trench MOSFET have decreasing or constant shoot-through current respectively in response to the increase of temperature, in contrast to the increasing trend observed on the selected SiC planar MOSFET. As a consequence of the large shoot-through current on symmetrical double-trench structured MOSFET, it undergoes fast temperature rise under continuous operation. Also, minimization of

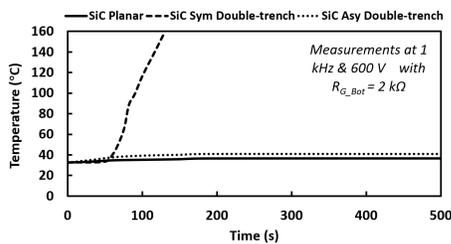


Fig. 14. Temperature rise in the 3 device structures.



Fig. 15. Maximum temperature recorded in the 3 device structures with $R_{G_Bot} = 2 \text{ k}\Omega$.

shoot-through by replacing large gate resistance of complementary device for symmetrical double-trench MOSFET is not as effective as that on the selected planar MOSFET and asymmetric double-trench MOSFET.

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