Trapezoidal operation of modular multilevel DC-DC converter for HVDC interconnections

Beeond M. Saleh, Felipe Donoso Merlet, Alessandro Costabeber, Alan J. Watson, Jon C. Clare
Department of Electrical and Electronic Engineering
University of Nottingham
Nottingham, United Kingdom
beeond.msaleh@nottingham.ac.uk

***Abstract*—High Voltage Direct Current (HVDC) grids are becoming a preferred option for the expansion of the traditional electrical networks as a result of their potential economic, technical and environmental benefits. Developing HVDC grids includes the linking of existing HVDC buses which may be implemented with different voltage levels, different HVDC technology and various grounding schemes. Interconnecting these HVDC systems will require DC-DC converters to provide voltage matching, isolation and a means for splitting the HVDC grid into sub systems. This paper presents a modified trapezoidal operation of MMC-DC-DC converter, MTrMMC-DC-DC, with high semiconductor device utilization and lower device current rating in addition to an increase of converter's energy density. Better utilization of the semiconductor devices results from conducting the current through the arms of the TrMMC-DC-DC converter continuously. The reduction of the energy storage requirements is achieved through careful design of the submodule (SM) capacitors and arm inductors to achieve resonance between the effective equivalent capacitor of each arm and the arm inductor at a frequency below twice the fundamental operating frequency. The circuit parameter design is validated for an 800MW, 400kV HVDC-based system through PLECS simulations.**

***Index Terms*—High voltage DC-DC power converter, DC transformer for HVDC, modular multilevel converter (MMC)**

I. Introduction

High-voltage direct current (HVDC) transmission systems are the preferred choice for transmitting electrical energy particularly over the long distances because of their well known economic, technical and environmental benefits in comparison to high voltage alternative current transmission systems, HVAC. The use of HVDC-based solutions for future electrical energy transmission system planning has been widely accepted in the industry and academia; many point to point HVDC systems have been established to transmit power over the long distances and offshore wind energy parks have steadily increased in number [1], [2]. Due to the differences of each HVDC link, several technical challenges have been presented with the development of HVDC grids. Although, organizations such as CIGRE, IEEE, and IEC are developing guidelines to standardize HVDC grids, many non standardized point to point HVDC links have been planned and commissioned [3], [4]. Developing HVDC grids mostly includes the existing HVDC links which are planned with different voltage levels, different HVDC technologies and various grounding schemes. Therefore, the development of HVDC grids will require DC-DC power converters which provide voltage stepping and DC voltage regulation. In addition, implementing DC-DC power converters in HVDC grids can also provide fault isolation capability, bidirectional power flow and an interface between different HVDC transmission schemes such as bipolar and monopolar schemes [2], [5].

As a result of the perceived importance of the application of DC-DC converters in HVDC grids several modular multilevel DC-DC power converter topologies have been proposed for HVDC interconnections over the last decade. Additionally, a number of non modular multilevel based DC-DC converter topologies were proposed for HVDC applications in literature, in particular, cascaded multi dual active bridge (DAB) DC-DC converters are the most addressed topologies for various HVDC applications [6]–[8]. However, implementing the non modular structures can be challenging due to the dv/dt stress on the transformer insulation and complications resulting from the series connection of devices. For instance, in a cascaded multi DAB DC-DC converter, many elementary cells are used to support the systems' high voltage and overcome the issue of connecting many semiconductor devices in series. A single phase low voltage transformer with either a half-bridge or an H-bridge converter are comprised in one cell whereas the need of many single phase transformers with different voltage insulation requirement makes the implementation of cascaded multi DAB DC-DC converters difficult in HVDC applications. As a result, modular multilevel converters are potentially the more reliable topologies for HVDC applications.

The focus on this paper will be mainly on the isolated DC-DC converter topologies with different voltage levels and isolation systems which may be required to split the bulky system into several sub systems to prevent blackout in case of system failure. However, in cases of similar HVDC systems with the same dc voltage level a non isolated DC-DC converter topologies can be used [9]–[12].

The sinusoidal operation of MMC-DC-DC converters was proposed in [13], [14] where two three phase MMCs are connected front-to-front (F2F) by their ac sides through a medium frequency transformer ($250Hz - 400Hz$). The advantage of this operation is the full control over the modulation index and during normal operation the arm current is continuous. As a result all semiconductor devices (IGBTs) are utilized and a dc

link filter is not required. Additionally, there is no dv/dt stress concern on the transformer insulation due to the production of high quality sinusoidal voltage waveforms. However, these approaches require high energy storage requirements even at medium-frequency operation.

Trapezoidal operation of three phase MMC-DC-DC (TrMMC-DC-DC) converter was proposed in [15] where two MMCs are connected F2F through a medium frequency transformer. In this operational mode, the submodules (SMs) in each arm are all inserted for half of the fundamental cycle and then they are bypassed for the other half. Therefore, the generated ac phase voltage is similar to that of a two-level voltage but to limit the dv/dt stress on the transformer the insertion and bypassing of the submodules is applied in a sequential manner over the transition period, T_t. The advantage of this is the dramatic reduction in the energy storage requirements when compared to a sinusoidal MMC-DC-DC converter. However, the current in the arm is discontinuous when operated in this way and this results in low IGBT utilisation ($\approx 55\%$) and also requires dc bus filters to smooth the dc current. Considering the same system conditions and based on the T_t, the TrMMC-DC-DC requires approximately 25% to 35% of the energy storage requirements for the sinusoidal operation of MMC-DC-DC and this significant reduction makes it preferable to sinusoidal operation for HVDC interconnections.

In [16] the author proposed a single phase trapezoidal operation of MMC-DC-DC with soft switching capability which is achieved with the addition of a capacitor in parallel with each IGBT device. The advantage of this approach is that continuous current is achieved through the converter arms and this results in better utilization of IGBT devices and a lower number of submodules as compared to two level three phase trapezoidal operation. However, control complexity, the challenge of building a single transformer to support high power for HVDC applications, the requirements of the bulky dc line filters, large arm inductors and the need for additional inductance (for the ac link) are the main drawbacks of this operation, although the converter can be operated at higher fundamental frequency.

The trapezoidal operation of the controlled transition bridge DC-DC converter (CTB-DC-DC) proposed in [17] and derived topologies from trapezoidal operation of transition arm converters proposed in [18] will require less energy storage due to the use of half of the submodules in comparison to TrMMC-DC-DC. Additionally, the required silicon area (semiconductor area) is reduced in trapezoidal operation of transition arm DC-DC converter topologies. In these topologies the submodules are used only during a transition period to reduce dv/dt stress on the transformer insulation. The arm current is discontinuously passes through the director switches for most of the period. However, the main drawback of these topologies is that during a dc fault, significant current will pass through the director semiconductor devices.

This paper proposes a modified three phase trapezoidal operation, MTrMMC-DC-DC and this proposed operation mode combines certain advantages over the mentioned topologies in [13], [15], [16]. Similar to all trapezoidal topologies the submodules of each chain-link are inserted for the majority of the half of the cycle period and bypassed for the majority of the other half of the cycle period. This trapezoidal operation is based on the selection of the arm inductors to keep the current conducting continuously and the choice of the submodule capacitor to reduce the energy storage requirements. The components of the converter should be selected carefully to ensure resonance between the arm inductor and the effective equivalent capacitor at lower than twice the fundamental frequency. As a result a continuous current conduction and the reduction of energy storage requirements are achieved. Better utilization of semiconductor devices (IGBTs), and a reduced semiconductor area is required since a lower semiconductor device current rating required in comparison to proposed operation in [15]. Lower switching losses due to having the switching actions only during transition time and eliminating DC link filters due to the smooth dc current are other advantages of the proposed MTrMMC-DC-DC.

The rest of this paper will be divided into following sections. Firstly, the converter topology, principle operation of MtrMMC-DC-DC and important voltage and current waveforms will be shown. Then, the selection of arm inductor and submodules capacitor will be explained. Furthermore, the semiconductor devices utilization will be validated through insertion of half bridge submodules and semiconductor devices current waveforms respectively. Finally, simulation results will be shown to validate the operation.

II. Principle operation of MTrMMC-DC-DC converter

Fig. 1 shows the MTrMMC-DC-DC converter which consists of two three phase MMCs, primary MMC and secondary MMC, and they are connected by their ac sides through a star connected medium frequency transformer where L_P, L_S, R_P, R_S are the arm inductors and parasitic resistors of arm inductors for both primary and secondary MMCs, respectively. The ideal upper arm voltage of the primary V_{UA} shown in Fig. 2 where ω is the angular frequency and T_d is the time between voltage levels, T_t is the transition time required between 0 to DC link voltage in staircase which reduces the dv/dt stress on the transformer insulation. Considering a single MMC, the upper arm voltage is complementary with the lower arm voltage within the phase and the phases are shifted by $2\pi/3$ rad. The arm voltage is generated using an uneven distribution of duty cycle method where the SMs are assigned in order based on the sorting with a maximum duty cycle $T/2+(N_{SM}-1)T_d$ and reduces by $2T_d$ until it reaches the minimum duty cycle which is $T/2-(N_{SM}-1)T_d$ (N_{SM} is the number of SMs per arm). The SMs capacitor voltage are balanced by assigning the gate signals with the higher net charge to the SMs with the lower capacitor voltage at fundamental frequency as described in [19].

The low voltage rating of semiconductor devices and high number of SMs in HVDC applications makes grouping SMs

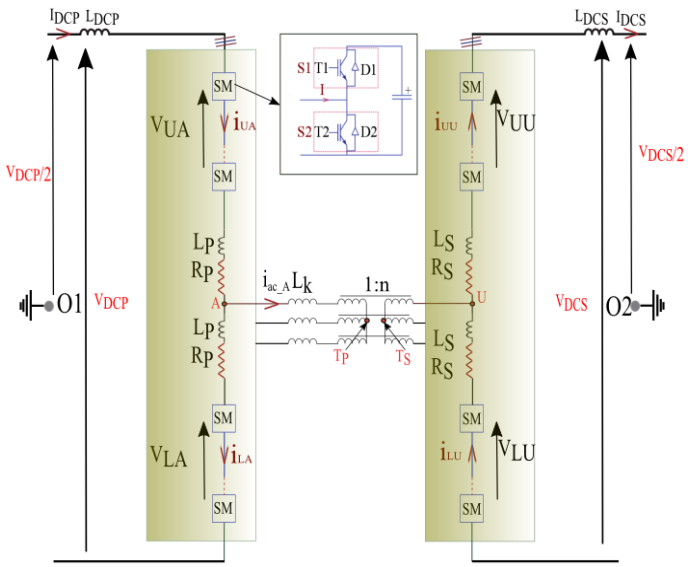

Fig. 1. MMC-DC-DC converter

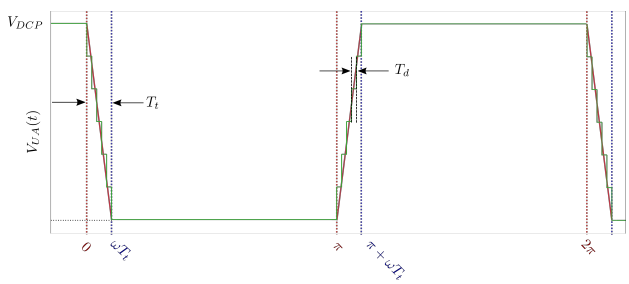

Fig. 2. Phase A primary arm voltage

in each chain-link essential to keep $T_t \leq 0.15\pi$ as shown in Fig. 3 where N_{st} is the number of voltage levels and N_L is the number of SMs per voltage level. The fundamental harmonic of primary phase A voltage, $v_{AO1}(f)$, and primary modulation index, m_p, are shown in equations 1 and 2, respectively, where $\alpha_P = \frac{1}{2}\omega(N_{st}-1)T_d$. Based on the equations 1 and 2, increasing T_t will reduce m_p and this results in higher current rating devices and lower SM energy density for transferring the demanded power. Therefore, the choice of T_t is selected based on the dc link voltage, ac link frequency and voltage steps to limit dv/dt stress on the transformer insulation. The selection of T_t is always a trade-off in HVDC applications where with higher T_t the voltage level is lower and consequently lower dv/dt stress but higher T_t increases the energy storage requirements due to the increase in the SM capacitor value. Moreover, the switching capability of semiconductor devices (IGBTs) determines T_d and 5µs can be chosen as minimum value for T_d when high power IGBTs are used.

$$v_{AO1}(f) = \frac{2V_{DCP}}{\pi}\frac{sin(\alpha_p)}{\alpha_p} \tag{1}$$

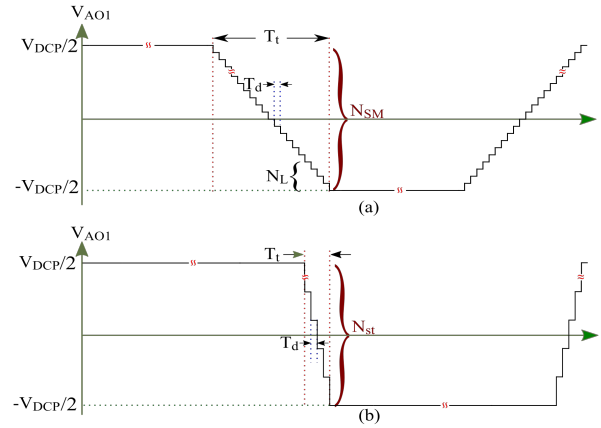

Fig. 3. The effect of grouping SMs on phase voltage with respect to DC link midpoint: (a) phase voltage without grouping SMs (b) phase voltage with grouping SMs

$$m_p = \frac{2v_{AO1}(f)}{V_{DCP}} = \frac{4}{\pi}\frac{sin(\alpha_p)}{\alpha_p} \tag{2}$$

Fig. 4 shows per-phase equivalent circuit of MTrMMC-DC-DC considering zero average power in each chain-link over the fundamental period by applying KVL. The primary transformer voltage, $V_{PTp_\phi P}(t)$, and secondary transformer voltage, $V_{STsp_\phi S}(t)$, are represented in eq. 3 and 4, respectively, where n represents transformer turns ratio, ϕP represents primary phases A, B and C and ϕS represents secondary phases U, V and W.

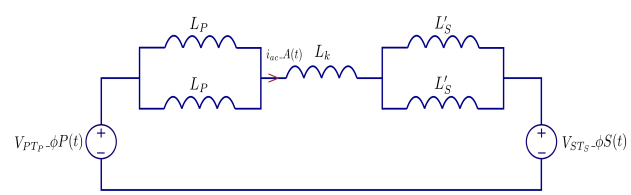

Fig. 4. Per-phase equivalent circuit of MtrMMC-DC-DC

$$V_{PTp_}\phi P(t) = \frac{V_{L\phi P}(t) - V_{U\phi P}(t)}{3} - V_{Tp}$$
$$V_{Tp} = \frac{(V_{LA}(t) - V_{UA}(t)) + (V_{LB}(t) - V_{UB}(t)) + (V_{LC}(t) - V_{UC}(t))}{3} \tag{3}$$

$$V_{STs_}\phi S(t) = n * (\frac{V_{L\phi S}(t) - V_{U\phi S}(t)}{3} - V_{Ts})$$
$$V_{Ts} = \frac{(V_{LU}(t) - V_{UU}(t)) + (V_{LV}(t) - V_{UV}(t)) + (V_{LW}(t) - V_{UW}(t))}{3} \tag{4}$$

Fig. 5 depicts $V_{PTp_A}(t)$ and with a phase shift, φ, which determines the power flow. It also depicts the phase A AC link current which can be analytically expressed using equation 5 where α indicates the time intervals from 0 to π and L_{eq} is determined from equation 6. Table I shows the phase A AC link current expressions for each portion from 0 to π when $\omega T_t < \varphi < \frac{\pi}{3} - \omega T_t$ where $\rho_g = \frac{nV_{DCS}}{V_{DCP}}$ is the dc voltage

gain and considering symmetric current waveform, equation 19 was applied to find the $i_{ac}_A(0)$ which was shown in equation 20. Similar calculation can be performed when φ is allocated at different intervals.

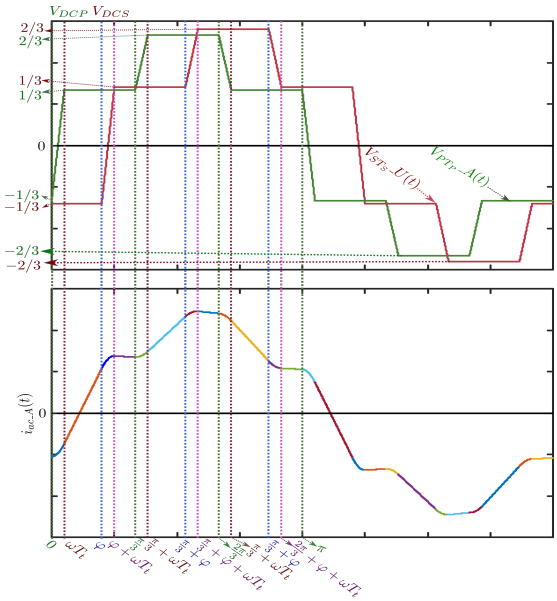

Fig. 5. Ac link voltage and current wave shaping of trapezoidal operation

$$i_{aTp(\alpha)} = i_{aTp0} + \frac{1}{\omega L_{eq}} \int_{\alpha_0}^{\alpha} (V_{aTp(\alpha)} - nV_{uTs(\alpha)}) * d\alpha \tag{5}$$

$$\begin{aligned} L_{eq} &= \frac{L_p}{2} + L_k + \frac{L'_S}{2} \\ L'_S &= \frac{L_S}{n^2} \end{aligned} \tag{6}$$

$$i_{ac}_A(0) = -i_{ac}_A(\pi) \tag{19}$$

$$i_{ac}_A(0) = \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g - 1)\frac{2\pi}{3} + (1-\rho_g)\frac{\omega T_t}{2} - \rho_g\varphi) \tag{20}$$

III. Selection of the Converter Components and Semiconductor Device Utilization

Under trapezoidal operation and apart from T_t all the SMs are inserted for half of the cycle period, $2f_o$, and bypassed for the other half in each arm. When the SMs are inserted the arm of the MTrMMC-DC-DC can be represented as an LC resonant arm. When the SMs are bypassed the arm can be represented as an inductive arm. Considering one of the primary arms the continuous conduction of arm current is achieved by keeping the resonant frequency, f_r, between C_{eqP} which is the primary arm equivalent SMs capacitance and L_P below the half of the cycle period, $fr \leq \frac{2f_o}{1.5}$, where the resonant frequency, f_r, of series LC circuit is shown in equation 21. Considering unity ρ_g and the ac link current profiles segment $\varphi \leq \alpha \leq \varphi + \omega T_t$ is important for calculating the size of SMs capacitor where dv/dt of transformer voltage is maximum. The expression 22 shows the size of the arm equivalent SMs' capacitance, C_{eqP}, at phase shift $\omega T_t \leq \alpha \leq \varphi + \omega T_t$ where δ_{pp} is the per unit peak to peak voltage ripple across the SM capacitor. The SM's capacitance $C_{SM} = C_{eqP}N_{SM}$ where $N_{SM} = V_{DC}/V_{SM}$, and V_{SM} is the nominal SM capacitor voltage.

TABLE I
$i_{ac}_A(\alpha)$ PROFILE FOR HALF FUNDAMENTAL CYCLE WHEN $\omega T_t < \varphi < \frac{\pi}{3} - \omega T_t$

α	$i_{ac}_A(\alpha)$	
$0 \leq \alpha \leq \omega T_t$	$i_{ac}_A(0) + \frac{V_{DCP}}{3\omega L_{eq}}(\frac{\alpha^2}{\omega T_t} + (\rho_g - 1)\alpha)$	(7)
$\omega T_t \leq \alpha \leq \varphi$	$i_{ac}_A(\omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g + 1)(\alpha - \omega T_t))$	(8)
$\varphi \leq \alpha \leq \varphi + \omega T_t$	$i_{ac}_A(\varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((\rho_g + 1)(\alpha - \varphi) - \frac{\rho_g}{\omega T_t}(\alpha - \varphi)^2)$	(9)
$\varphi + \omega T_t \leq \alpha \leq \frac{\pi}{3}$	$i_{ac}_A(\varphi + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\alpha - \varphi - \omega T_t))$	(10)
$\frac{\pi}{3} \leq \alpha \leq \frac{\pi}{3} + \omega T_t$	$i_{ac}_A(\frac{\pi}{3}) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\alpha - \frac{\pi}{3}) + \frac{1}{2\omega T_t}(\alpha - \frac{\pi}{3})^2)$	(11)
$\frac{\pi}{3} + \omega T_t \leq \alpha \leq \frac{\pi}{3} + \varphi$	$i_{ac}_A(\frac{\pi}{3} + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((2 - \rho_g)(\alpha - \frac{\pi}{3} - \omega T_t))$	(12)
$\frac{\pi}{3} + \varphi \leq \alpha \leq \frac{\pi}{3} + \varphi + \omega T_t$	$i_{ac}_A(\frac{\pi}{3} + \varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((2 - \rho_g)(\alpha - \frac{\pi}{3} - \varphi) - \frac{\rho_g}{2\omega T_t}(\alpha - \frac{\pi}{3} - \varphi)^2)$	(13)
$\frac{\pi}{3} + \varphi + \omega T_t \leq \alpha \leq \frac{2\pi}{3}$	$i_{ac}_A(\frac{\pi}{3} + \varphi + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((2 - 2\rho_g)(\alpha - \frac{\pi}{3} - \varphi - \omega T_t))$	(14)
$\frac{2\pi}{3} \leq \alpha \leq \frac{2\pi}{3} + \omega T_t$	$i_{ac}_A(\frac{2\pi}{3}) + \frac{V_{DCP}}{3\omega L_{eq}}((2 - 2\rho_g)(\alpha - \frac{2\pi}{3}) - \frac{1}{2\omega T_t}(\alpha - \frac{2\pi}{3})^2)$	(15)
$\frac{2\pi}{3} + \omega T_t \leq \alpha \leq \frac{2\pi}{3} + \varphi$	$i_{ac}_A(\frac{2\pi}{3} + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - 2\rho_g)(\alpha - \frac{2\pi}{3} - \omega T_t))$	(16)
$\frac{2\pi}{3} + \varphi \leq \alpha \leq \frac{2\pi}{3} + \varphi + \omega T_t$	$i_{ac}_A(\frac{2\pi}{3} + \varphi) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - 2\rho_g)(\alpha - \frac{2\pi}{3} - \varphi) - \frac{\rho_g}{2\omega T_t}(\alpha - \frac{2\pi}{3} - \varphi)^2)$	(17)
$\frac{2\pi}{3} + \varphi + \omega T_t \leq \alpha \leq \pi$	$i_{ac}_A(\frac{2\pi}{3} + \varphi + \omega T_t) + \frac{V_{DCP}}{3\omega L_{eq}}((1 - \rho_g)(\alpha - \frac{2\pi}{3} - \varphi - \omega T_t))$	(18)

$$\begin{aligned} C_{eqP} &= \frac{1}{\omega V_{DCP}\delta_{pp}} \int_{\alpha=\varphi}^{\alpha=(\omega T_t+\varphi)} (\frac{I_{DCP}}{3} + \frac{i_{ac}(t)}{2}) d\alpha \\ &= \frac{T_t(14\pi\varphi - 2\pi\omega T_t - \omega^2 T_t^2 - 6\varphi^2)}{36 L_{eq}\delta_{pp}\omega\pi} \end{aligned} \tag{22}$$

By selecting $fr \leq \frac{2f_o}{1.5}$ the TrMCC-DC-DC will operate with continuous current in the arms. In addition, by knowing the C_{eq}, the arm inductor can be determined. Fig. 6 shows the ideal current and voltage of the upper arm of phase A with IGBT utilization and similar to conventional MMC the arm current comprises dc current and ac current. Considering the half bridge SM shown in Fig. 1 and when all SMs are bypassed (0 to $\pi - T_t$) transistor, T2, is conducting and during

transition period, T_t, transistor, T2, and diode, D1, are sharing the arm current. In the half of the period where the SMs are all inserted the device D1 is ON when the arm current is positive and transistor T1 is ON when the arm current is negative. Under this operation both switches, S1 and S2, are conducting continuously. Moreover, transistor, T1, is soft switching at zero current since the current goes through the diode of the SM and this is an additional advantage of this proposed trapezoidal operation in terms of switching loss considerations. The continuous conduction of current in the arms and the trapezoidal voltage waveforms make the device current rating reduces by approximately 25% in comparison to other operations since in MtrMMC-DC-DC, the devices peak current is $\frac{I_{DCx}}{3} + \frac{\hat{i}_{ac}}{2}$ where $\hat{i}_{ac}$ is the peak AC current and additionally other low order odd harmonics of current contribute in power transfer. However, in TrMMC-DC-DC operation, the devices peak current is the same as peak AC current and ideally in sinusoidal MMC-DC-DC operation only fundamental component of current contributes in power transfer.

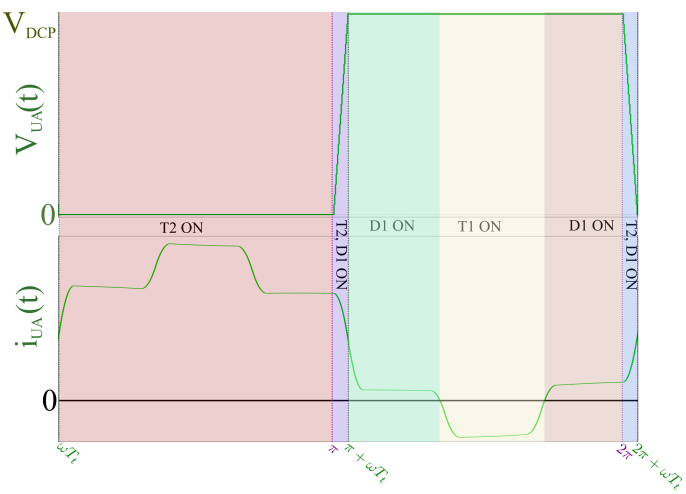

Fig. 6. phase A upper arm voltage and current waveforms with devices utilization

IV. Simulation Results

An 800MW system with a 10% series inductance assumption, 400kV primary and secondary dc link voltage was developed in PLECS to validate the proposed trapezoidal operation of MMC-DC-DC converter. Table II shows the parameters of the converter circuit where 10% peak to peak ripple across SMs capacitor voltage, $\delta_{pp} = 10\%$, is considered. Fig. 7 shows the instantaneous waveform of the upper chain-link voltage of phase A, $V_{UA}(t)$, lower chain-link voltage of phase A, $V_{LA}(t)$, primary DC current, $I_{DCP}(t)$, AC link current, $i_{ac}(t)$, upper arm current of phase A, $i_{UA}(t)$, lower arm current of phase A, $i_{LA}(t)$, sum of upper SMs' capacitor voltage per group (level), $V_{CgP_U}(t)$, and sum of lower SMs' capacitor voltage per group (level), $V_{CgP_L}(t)$, respectively. Fig. 8 shows the results during transient conditions when the power demand was changed from 400MW to 800MW. The

TABLE II
Circuit Parameters

Parameters	Value
$V_{DCP} = V_{DCS}$	400kV
Rated power, P_r	800MW
L_k 10%	8.6mH
$L_p = L_s$	28.45mH
V_{SM}	2kV
N_{SM} *Per Chain-Link*	200
N_{st}	20
$N_{LP} = N_{LS}$	10
$T_{dP} = T_{dS}$	15µs
$C_{SMP} = C_{SMS}$	1.6 mF
$C_{gP} = C_{gS}$	0.16 mF
φ	0.13π
$\frac{fr}{fo}$	1.334
δ_{pp}	10%
f_o	250 Hz

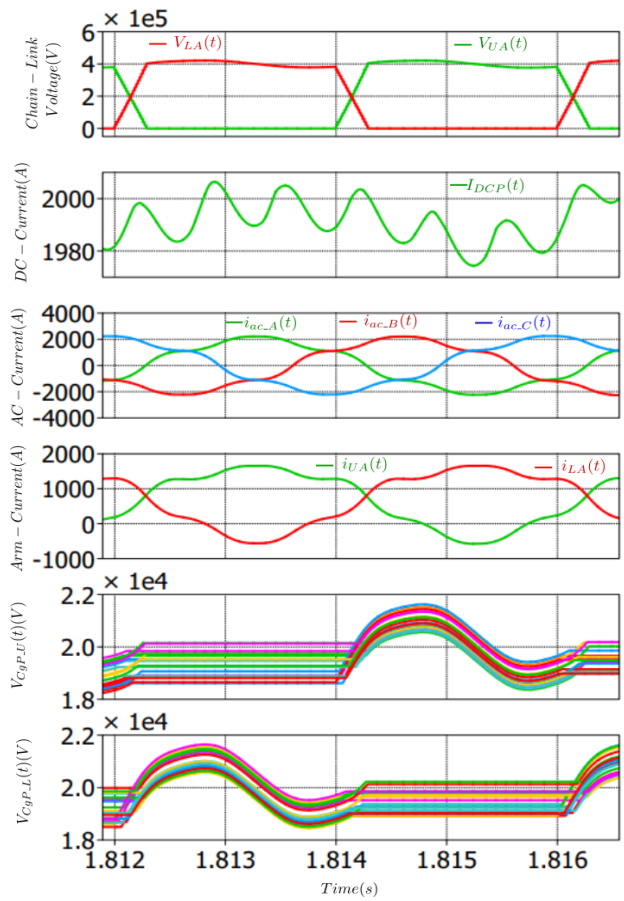

Fig. 7. MTrMMC-DC-DC waveforms

results validates the modified trapezoidal operation and the analytical parameters' design.

V. Conclusion

This paper introduced a modified trapezoidal operation of MMC-DC-DC converter for HVDC interconnection with better semiconductor devices utilization and lower semiconductor devices' current rating in addition to the reduction in energy

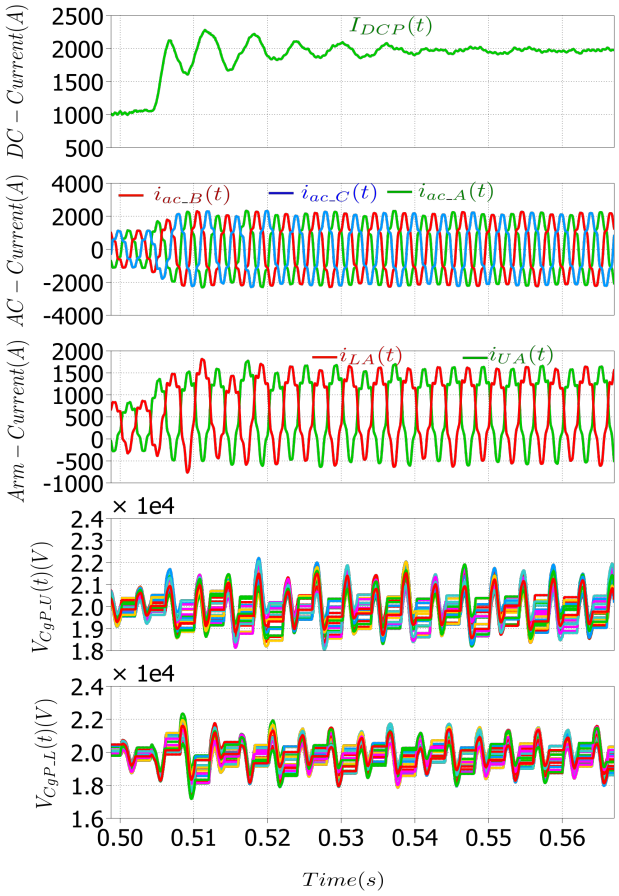

Fig. 8. MTrMMC-DC-DC waveforms with energy control, current and fast power flow control

storage requirements. Intensive operation analysis was shown where based on resonant frequency between the equivalent capacitance of the arm and the corresponding arm inductance the circuit parameters' were designed. This resonance makes the current conduct continuously in the arm and as a result both switches in half bridge SMs will be utilized and devices are needed with lower current rating which means lower silicon area. Additionally, the zero current soft switching of one of the switches is naturally achieved and the sorting the SMs at the fundamental frequency reduces the switching losses of the converter. The 800MW simulation results in PLECS software support the effectiveness of the proposed trapezoidal operation of MMC-DC-DC converter.

VI. Dedication

This paper is dedicated to the memory of our fellow researcher, friend and co-author, Dr. Alessandro Costabeber. Alessandro was instrumental in the development of the operation. He sadly died June 2020 before the work could be completed.

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