Chipped PWM Strategy with SMPS for Noise Mitigation in PSDM-based Systems

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***Abstract*—Power/signal dual modulation (PSDM) is a promising integrated communication solution for intelligent switched-mode power supply (SMPS) systems. A common strategy is to utilize input/output switching ripples as information carriers, which transmit along common power bus. As the switching harmonics peaks are located in the same frequency band with communication signals, they may lead serious noise interference. To deal with this issue, random PWM is a proper solution, as it scatters the spectrum of switching harmonic peaks to a much wider and flatter one. This paper proposes a novel chipped PWM strategy to shape the switching harmonics to semi-Gaussian white noise. It breaks the periodicity of PWM sequence and releases more control freedom of the gate signal. Conventional PWM strategy is not used, but independent chips of high voltage level state and low voltage level state are introduced. They are combined in a pseudo random way, and the numbers of "on" and "off" chips in each pseudo random encoding interval are constant to ensure a desired equivalent duty-cycle. Therefore, switching harmonic suppression is achieved for improved communication performance with PSDM. Simulation and experimental results are presented to validate the proposed strategy.**

Keywords—Switched-mode power supply (SMPS), Random PWM, Power/signal dual modulation (PSDM), Pseudo random encoding

I. Introduction

Switched mode power supplies (SMPSs) have been widely adopted due to its high efficiency, flexible control, and high accuracy [1]. They play a vital role in connecting renewable power generators, power grids, load, and energy storage devices, forming a power electronics system. In order to achieve distributed, reliable, efficient, and intelligent power control and management, communications among SMPSs are indispensable. Power and signal dual modulation (PSDM) with SMPSs is a promising technique for integrated and reliable communication [2]. It has great advantages of simple structure and low cost [3]. In this scheme, information is modulated to the power switching carrier, carried by input/output switching ripples, and then transmitted along the common power bus [4]-[6].

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Although high frequency switching operation of SMPSs has the benefits of flexible control, providing the possibility to integrate signal modulations, it unavoidably creates the harmonics emission problems [7]. It brings serious noises in communication band, which is the main noise in communication. For the conventional PWM strategy, there are switching harmonics peaks located at the switching frequency f_s, as well as $3f_s$, $5f_s$, $\cdots$ in the spectrum, making the communication noise extremely serious.

To suppress the switching harmonics noises, random PWM technique is a promising solution. Compared with other strategies like orthogonal signal modulation [8] and signal frequency shifting [9], random PWM mitigates the harmonics peaks at source.

Back to 1969, Clarke et al introduced spread spectrum method to SMPS, and proposed random PWM strategy for switching harmonics mitigation [10]. Further, various random PWM strategies have been proposed, e.g. randomized pulse position modulation (RPPM), randomized pulse width modulation (RPWM), randomized carrier frequency modulation with fixed duty ratio (RCFMFD), randomized carrier frequency modulation with variable duty ratio (RCFMVD), randomized duty ratio and an RPPM with fixed carrier frequency (RDRPPMFCF), randomized carrier frequency and a RPPM with fixed duty ratio (RCFRPPMFD), and randomized carrier frequency and a randomized duty ratio with RPPM (RRRM) [11]-[17]. They differ from each other in four degrees of switching frequency, pulse position, pulse width, and duty cycle in PWM process. In general, the improved random strategies and increased random degrees are helpful in increasing dispersion of switching harmonics in the spectrum [18].

Among them, RPPM can be further divided into several subclasses. For example, [19] proposed a random lead-lag modulation, in which the pulse position generated at the beginning of the switching interval is randomly modulated. [20] proposed a random phase shift modulation. In this scheme, the phase shift time in positive half-cycle, and the time in the negative half cycle are randomized, while the switching frequency is kept constant. [11] presented a random displacement of the pulse center modulation, in which the pulse in the center of the switching interval is shifted randomly. However, the existing researches are mainly focused on the harmonics suppressions for EMI mitigation, but the influence to the PSDM-based communication is never studied.

In fact, both the power spectrum density and the shape of spectrum of the noise have great impact on the PSDM-based communication performance. Specifically, according to Shannon theory, higher power spectrum density of noise leads to lower channel capacity with the spectrum shape keeps the same. On the other hand, if the power spectrum keeps the same, the Gaussian white noise indicates the highest channel capacity. Random PWM can mitigate the switching harmonics peaks and reduce the power spectrum density within the communication band. As a result, it is a prospective technique to increase the channel capacity and enhance the communication performance in PSDM-based systems.

Due to the potential advantages of random PWM in noise mitigation, this paper proposes a novel chipped PWM strategy to suppress the switching harmonic peaks and alleviate noise problems in communication band in PSDM-based systems. It is adopted by all the SMPSs not sending signals at the moment. In this scheme, the high voltage level ("on") state and low voltage level ("off") state with constant duration times (called a "chip") are combined in a pseudorandom way as the gate signal, which enhances control flexibility and releases more control freedoms. Considering the switching losses, the equivalent duty cycle should be constant, which is determined by power control loop. Therefore, "on" state chips and "off" state chips are combined in a pseudo random way, and the total number of each are determined by power control loop. Compared with existing random PWM strategy, the proposed strategy releases more control freedoms and supports more flexible encoding strategies.

This paper is organized as follows: section II presents the basic principle of the proposed chipped PWM strategy, and section III gives design details with a buck/boost converter. Section IV shows the simulation and experimental validations, and section V is the conclusion.

II. PRINCIPLE OF CHIPPED PWM STRATEGY

In conventional PWM strategy, periodical square wave sequence is adopted as the gate signal, which is generated by comparing the output reference with a periodical triangle/sawtooth wave sequence, as shown in Fig. 1. In stable state, the duty-cycle keeps constant, and thus the "on" and "off" state alternate in a constant frequency. In this scheme, only one control freedom, i.e. duty ratio, is used. In most existing random PWM strategies, some key parameters are adjusted randomly in each switching cycle, as shown in Fig. 2, i.e. switching interval T_{s}, pulse width W_{s}, pulse position P_{s}, and the duty ratio $\frac{W_{\mathrm{s}}}{T_{\mathrm{s}}}$. One or more random degrees are introduced in different methods, leading to different harmonic spectrums. In the proposed chipped PWM method, more narrow chips are divided in time domain, and each chip has a constant state of either high or low, as shown in Fig. 3. The high voltage level chip corresponds to the "on" state of the switch, while the low voltage level chip corresponds to the "off" state of the switch. The "on" and "off" states are randomly distributed, so that the harmonics are spread to a wide bandwidth, as shown in Fig. 4. As a result, the spikes noise interference to the communication signals along the common power bus can be eliminated, and the communication performance can be improved. To optimize the performance, the harmonics spectrum should approach Gaussian white noise as close as possible.

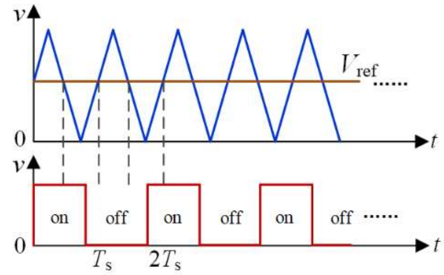


Fig.1 Principle of conventional PWM strategy.

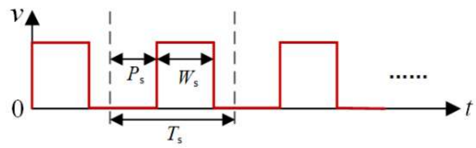


Fig.2 Principle of some existing random PWM strategies.

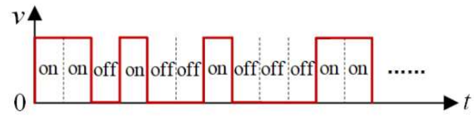


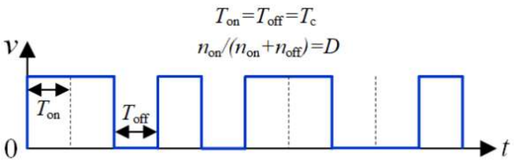
Fig. 3 Principle of the proposed chipped PWM strategy.

According to Shannon theory, the channel capacity of a communication system with Gaussian white noise only is derived as:

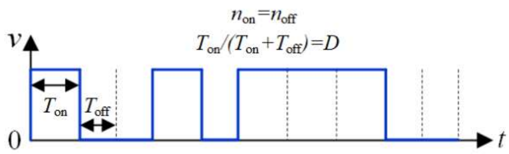
$$C_{\mathrm{WGN}} = W \log(1 + \frac{P}{N}) \tag{1}$$

in which W is the bandwidth, P is the power of signal, and N is the power of noise. If there are other types of noises, while the total noise power keeps constant, the noise spectrum will be uneven, then channel capacity will be less than C_{WGN}. Therefore, it is theoretically approved that the channel with Gaussian white noise has the highest channel capacity than those with other types of noises while the total noise power keeps the same. The proposed chipped PWM strategy provides rich encoding freedoms of "on" and "off" chips, and they can be pseudo randomly encoded approaching the Gaussian white noise distribution to maximize the channel capacity.

In order to achieve stable and required value of output power of the SMPS, the equivalent duty ratio is determined by the power control module, and in stable state, the equivalent duty ratio is a constant D. For this purpose, there are two possible solutions: constant chip length encoding and constant chip probability encoding. For the first one, the probabilities of chips "on" and "off" are determined by the duty ratio, while the chip length of them are the same, as shown in Fig. 4(a). It requires a changeable encoding rule, of which the probability of "on" and "off" should be adjusted according to the feedback of power loop in real time. Besides, the control precision is limited by the length of pseudo random sequence. For the second one, the length of chip "on" and "off" are determined by the duty ratio, while the probability of them are the same, as shown in Fig. 4(b). The encoding rule can always keep the same with different power feedback, and the probability of "on" and "off" should be the same. Also, the power control precision is much higher than the first one. As a result, constant chip probability encoding is adopted.



(a)



(b)

Fig. 4 Two operation modes of chipped PWM strategy. (a) Constant chip length. (b) Constant chip probability.

In the proposed chipped PWM scheme, the chip length is carefully selected, which is closely related to the power conversion performance and power harmonics distributions. If the chip length is too small, frequent switching losses may cause serious heating problem. Besides, the nonideal rising/falling edges also limits the minimum chip length. If the chip length is too large, it will deteriorate the input/output power quality.

The sampling period selection for closed loop power control is another key issue in the proposed chipped PWM design. In order to achieve fixed frequency sampling, the concept of encoding period is introduced, in which the equivalent duty ratio is kept constant according to the power loop command. Therefore, in each encoding interval, there is the following relationship:

$$d_{\mathrm{equ}} = \frac{n_{\mathrm{on}} \cdot T_{\mathrm{on}}}{n_{\mathrm{on}} \cdot T_{\mathrm{on}} + n_{\mathrm{off}} \cdot T_{\mathrm{off}}} \tag{2}$$

in which n_{on} and n_{off} are the total number of "on" states and "off" states in each coding interval, while T_{on} and T_{off} are the chip length of "on" state and "off" state. In stable state, the charging and discharging of the output capacitor in each encoding interval is balanced. Therefore, in this scheme, fixed frequency sampling can be adopted and no output voltage vibrations will be introduced. The current sampling and control obeys similar rule.

A pseudo random encoding mechanism is employed to achieved switching harmonics spectrum dispersion, and it should satisfies the following constrains: 1) the length of the pseudo random sequence should be constant so that constant frequency sampling can be adopted; 2) the number of "on" chips and "off" chips are the same in each sequence; 3) the encoding period is much lower than switching frequency to avoid impulsive interferences in communication band. With these constraints, *M* sequence is a proper choice. It is generated by an *n*-stage nonlinear feedback shift register, shown in Fig. 5, and the generated sequence length is 2^n. In *M* sequence, the number of "0"s and "1"s are the same, which satisfies the requirement of constant probability solution in chipped PWM.

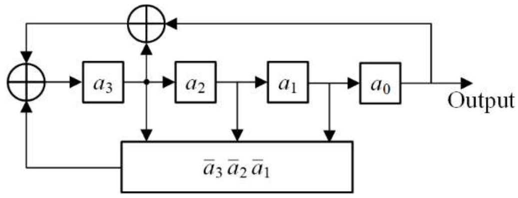


Fig. 5 Generation of *M* sequence by the nonlinear feedback shift register (4-stage as an example).

Among the runs of "1"s and of "0"s in each encoding interval, $\frac{1}{2^k}$ are of length k $(1 \leq k \leq n-2)$, and 2 are of length n [21]. Therefore, with the increase of the sequence length, the switching ripple's amplitude tends to be larger in time domain. To achieve the tradeoff between the input/output power quality in both time domain and frequency domain, the sequence length should be carefully selected.

III. Design of Chipped PWM Strategy

In this section, the chipped PWM design based on a buck/boost converter is presented in detail.

In this condition, 4-stage *M* sequences with length $2^4 = 16$ are adopted. According to the characteristics of *M* sequence, there are totally 16 sequences with length 16, as listed in Table I. To further disperse the spectrum, the 16 *M* sequences are randomly shifted.

TABLE I. All the 4-Stage *M* Sequence

0,0,0,1,1,1,1,0,1,1,0,0,1,0,1,0	0,0,0,0,1,1,1,1,0,1,0,0,1,0,1,1
1,1,1,0,0,0,0,1,0,0,1,1,0,1,0,1	0,0,0,0,1,0,1,0,0,1,1,0,1,1,1,1
0,0,0,0,1,0,1,1,0,0,1,1,1,1,0,1	0,0,0,0,1,0,1,1,1,1,0,0,1,1,0,1
0,0,0,0,1,1,0,0,1,0,1,1,1,1,0,1	0,0,0,0,1,1,0,1,0,1,1,1,1,0,0,1
0,0,0,0,1,1,1,1,0,0,1,0,1,1,0,1	0,0,0,0,1,1,1,1,0,1,0,1,1,0,0,1
0,0,0,0,1,0,0,1,1,1,1,0,1,0,1,1	0,0,0,0,1,0,1,0,0,1,1,1,1,0,1,1
0,0,0,0,1,0,1,1,0,1,0,0,1,1,1,1	0,0,0,0,1,0,1,1,1,1,0,1,0,0,1,1
0,0,0,0,1,1,0,1,0,0,1,0,1,1,1,1	0,0,0,0,1,1,0,1,1,1,1,0,0,1,0,1

According to the runs feature of *M* sequence, there are totally 8 times of state switching in every 4-stage sequence, and an example is shown in Fig. 6, which equals 4 switching periods in conventional PWM mode. Therefore, the equivalent switching frequency is derived as:

$$f_{s\_eq} = \frac{1}{4T_{\mathrm{chip}}} \tag{3}$$

in which T_{chip} is the chip length.

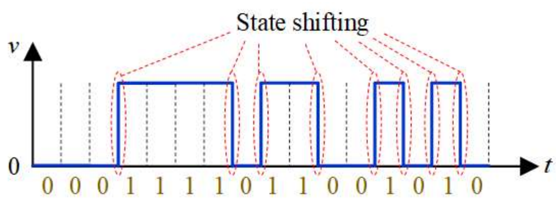
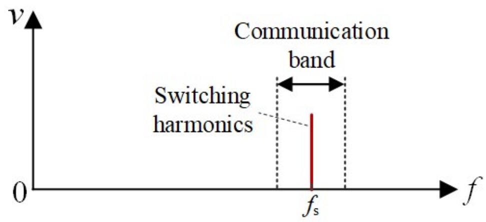


Fig. 6 4-stage *M* sequence

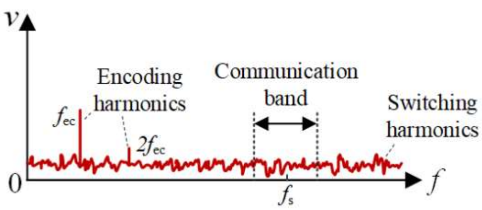
As 4-stage *M* sequences are adopted, there will be encoding harmonics peaks in the encoding frequency, which is

$$f_{\mathrm{ec}}=\frac{1}{16T_{\mathrm{chip}}} \quad (4)$$

Different from the switching harmonics peak of conventional PWM strategy, which is located in communication band, shown in Fig. 7(a), f_{ec} is much lower than $f_{\mathrm{s\_eq}}$, and thus it is beyond the communication band, as shown in Fig.7(b). Besides, f_{ec} can be flexibly adjusted by the length of *M* sequence according to practical application requirements. Scattered harmonics can be easily filtered without distorting communication signals as they are beyond the communication band.



(a)



(b)

Fig. 7 Output power harmonics spectrum. (a) With conventional PWM strategy. (b) With chipped PWM strategy.

To sum up, with chipped PWM, the switching harmonics peaks in spectrum are dispersed to a wide range, which is semi-Gaussian white noise. The periodical pseudo random encoding will lead to encoding harmonics peaks in the spectrum, but they are quite far away from communication band. Therefore, the noise in the channel in communication band is greatly suppressed, and the communication performance can be well improved.

IV. Simulation and Experimental Result

Simulations and experiments are carried out to verify the feasibility and effectiveness of the proposed method. The prototype structure is designed as shown in Fig. 8. Two buck/boost converters are adopted with output port connected in parallel. Some key parameters are listed in Table II, and 4-stage *M* sequences are adopted as shown in Table I.

First of all, only buck/boost converter #1 is operating, and chipped PWM strategy is adopted. According to (3), the equivalent switching frequency is $f_{\mathrm{s\_eq}}=125\ \mathrm{kHz}$. Fig. 9 shows the output voltage ripple waveform. “On” and “off” chips are pseudo randomly arranged, as shown in green waveform.

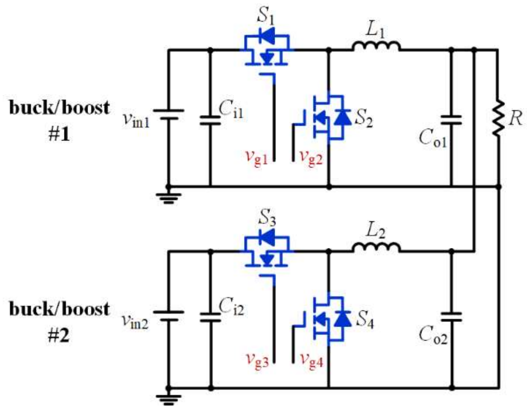


Fig. 8 Prototype structure.

TABLE II. Key Parameters of the Prototype

Parameters	Symbol	Value
Input voltage	V_{i}	48 V
Output voltage	V_{o}	24 V
Chip length	T_{c}	2 μs
Encoding period	T_{ec}	32 μs
Inductor	L	100 μH
Input capacitor	C_{i}	1000 μF
Output capacitor	C_{o}	1000 μF
Feedback control sampling frequency	f_{s}	31.25 kHz

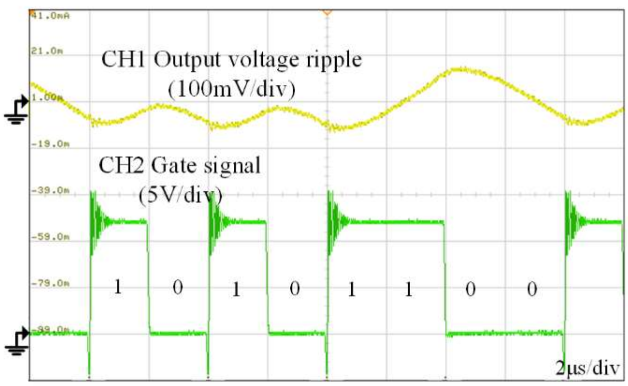


Fig. 9 Waveform with chipped PWM strategy.

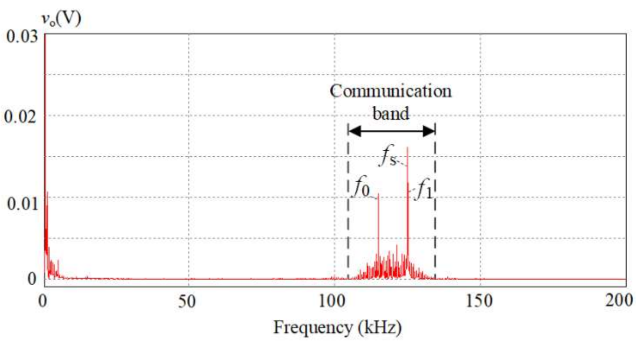


Fig. 10 Output voltage spectrum with conventional PWM adopted by buck/boost #1 and PSDM adopted by buck/boost #2.

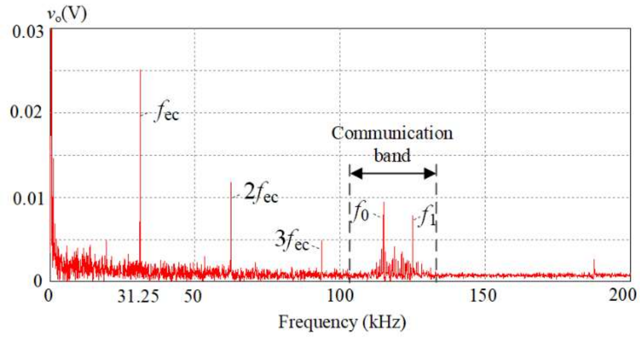


Fig. 11 Output voltage spectrum with chipped PWM adopted by buck/boost #1 and PSDM adopted by buck/boost #2.

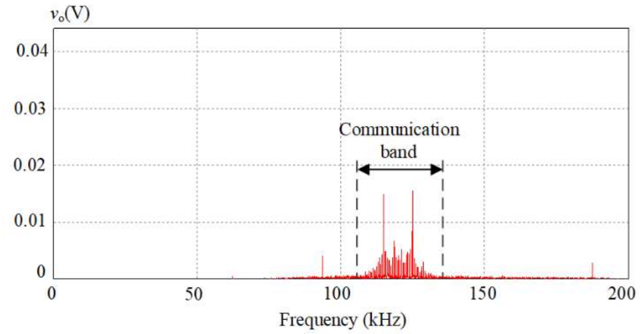


Fig. 12 Conditioned signal in the receiver with chipped PWM adopted by buck/boost #1 and PSDM adopted by buck/boost #2.

Then both buck/boost converters #1 and #2 are operating, and #2 operates in PSDM mode with binary frequency shift keying (FSK) modulation. Therefore, two switching frequencies 125 kHz and 115 kHz are adopted, representing data "1" and "0" respectively, as shown in Fig. 10 and 11. In the conventional PWM strategy with fixed switching frequency $f_s = 125$ kHz employed by buck/boost converter #1, there is a switching harmonic peak located in f_s in the output voltage spectrum, as shown in Fig. 10. It is highly overlapped with communication spectrum, and thus causes serious noise interference. With chipped PWM adopted by buck/boost converter #1, the switching harmonics peaks are dispersed to a wide range, with characteristics like Gaussian white noise, as shown in Fig. 11. Encoding frequency harmonics of 31.25 kHz is out of communication band. Fig. 12 shows the spectrum in the receiver after signal conditioning. It can be seen that the encoding harmonics peaks are greatly suppressed by filters in the receiver.

In sum, with chipped PWM strategy, the noise environment in communication band is greatly improved. Switching harmonics peaks are mitigated to semi-Gaussian white noise, and the power spectrum density in communication band is also reduced. As a result, it can greatly alleviate the serious noise interference problem and improve channel capacity in PSDM-based systems.

V. Conclusions

This paper proposes a chipped PWM strategy for switching harmonics mitigation. It is mainly designed for the PSDM-based systems, in which communication is achieved using power switching ripples. Therefore, in these systems, communication signals are in switching frequency band, and switching harmonics from other SMPSs are the main noises. The proposed strategy can mitigate the switching harmonics peaks at source, and thus greatly improve the channel noise environment. It employs pseudo random combination of "on" and "off" chips for a semi-Gaussian white noise distribution of switching harmonics. In this scheme, there will be no switching harmonics peaks from normal operated SMPSs in communication band. For optimization, there is still some work to be done in the future. First, the pseudo random encoding strategies can be further improved, so that better harmonics spectrum can be achieved to enhance the channel capacity, and corresponding strategies can be developed for specific applications. Besides, the influence of encoding strategies to power conversion, e.g. EMI, needs more in-depth research.

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