A New Input-Parallel-Output-Series Three-Phase Hybrid Rectifier for Heavy-Duty Electric Vehicle Chargers

Qiang, Rui; Wu, Yang; Soeiro, Thiago Batista; Granello, Pierpaolo; Qin, Zian; Bauer, Pavol

DOI
10.1109/IECON49645.2022.9968988

Publication date
2022

Document Version
Final published version

Published in
IECON 2022 - 48th Annual Conference of the IEEE Industrial Electronics Society

IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society | 978-1-6654-8025-3/22/$31.00 ©2022 IEEE | DOI: 10.1109/IECON49645.2022.9968988

A New Input-Parallel-Output-Series Three-Phase Hybrid Rectifier for Heavy-Duty Electric Vehicle Chargers

1st Rui Qiang
DCE&S
Delft University of Technology
Delft, The Netherlands
R. Qiang@student.tudelft.nl

2nd Yang Wu
DCE&S
Delft University of Technology
Delft, The Netherlands
Y.Wu-6@tudelft.nl

3rd Thiago Batista Soeiro
Power Management and Distribution Section
European Space Agency
Noordwijk, The Netherlands
Thiago.BatistaSoeiro@esa.int

4th Pierpaolo Granello
Astronautical, Electrical and Energetic Engineering
Sapienza University of Rome
Rome, Italy
pierpaolo.granello@uniroma1.it

5th Zian Qin
DCE&S
Delft University of Technology
Delft, The Netherlands
Z.Qin-2@tudelft.nl

6th Pavol Bauer
DCE&S
Delft University of Technology
Delft, The Netherlands
P.Bauer@tudelft.nl

***Abstract*—This paper proposes a solution to the circuit topology of heavy-duty electric vehicle (HDEV) chargers. In light of the original hybrid rectifier, a new unidirectional Input-Parallel-Output-Series (IPOS) three-phase hybrid rectifier is proposed and analyzed. The IPOS topology is advantageous at ultra-high power rating to interface the next-generation HDEV batteries which require a high and wide output voltage range of 800∼1500 V with available 600/1200V commercial semiconductors. Moreover, the proposed topology is efficient, cost-effective, and scalable with the grid input current harmonic components in compliance with the IEEE-519 standard. The benefits of the IPOS topology are supported by circuit derivation, control strategy, analytical modelling, simulation, and experimental verification.**

***Index Terms*—fast charging, hybrid rectifier, partial power processing, power factor correction, AC–DC converter**

I. Introduction

A trend of electrifying heavy-duty vehicles and developing ultra-fast chargers has emerged for the next phase of the global electrification of transport. In applications such as the charging of HDEV batteries, the power rating of the chargers can reach an ultra-high level (>1 MW). In 2018, CharIN initiated the 'Megawatt Charging System' project to meet the market demand for charging E-trucks and E-buses [1]. It is evident that the power rating of EV chargers will continue to increase in the future, welcoming more suitable circuit topologies.

In the conventional two-stage charger topology, the components have to be rated for Full Power Processing (FPP), which imposes limitations on the system efficiency and power density and is less desirable in high-power applications. Furthermore, to provide a high output voltage (>1000 V) to interface the next-generation HDEV batteries, less available and more expensive semiconductor devices of higher voltage ratings, e.g. 1700 V are required, which limits the design space.

Much research effort has been spent on improving the efficiency, power density, and effective cost of the power conversion stages of EV chargers. Converters that process only a fraction of the total power and deliver partial output voltage with the majority of the power processed by a close-to-unity efficient secondary path, are addressed as Partial Power Processing (PPP) converters. The IPOS PPP configuration is shown in Fig. 2(b). The output voltage of the IPOS PPC is only part of the total output voltage. Accordingly, the PPP contributes to higher overall system efficiency and power density compared to an FPP system [2].

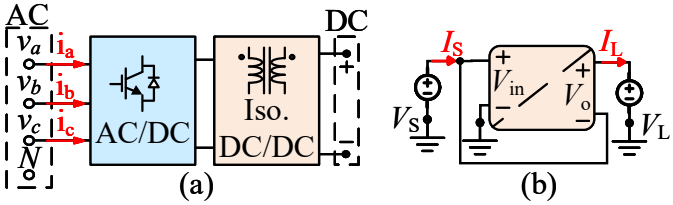

Fig. 2: (a) Conventional charger topology (b) PPP IPOS

The hybrid rectifier denotes a parallel connection of two or more rectifier stages (cf. [Fig. 1(b)]). Hybrid rectifiers innately incorporate the PPP characteristic by processing the majority of the active power through a more efficient line-commutated rectifier, and the minority of active power through a less efficient self-commutated rectifier which compensates for the reactive power, offering higher system efficiency, a unity power factor, and a sinusoidal grid current.

In light of the concepts of the PPP and the hybrid rectifier, this paper proposes a PPP IPOS three-phase hybrid rectifier which is derived from the IPOP topology in [3] (cf. [Fig. 1(a)]). The main difference between the proposed topology and the IPOP hybrid rectifiers discussed in [3], [4] is that the DC-links are connected in series, enabling the system to deliver a

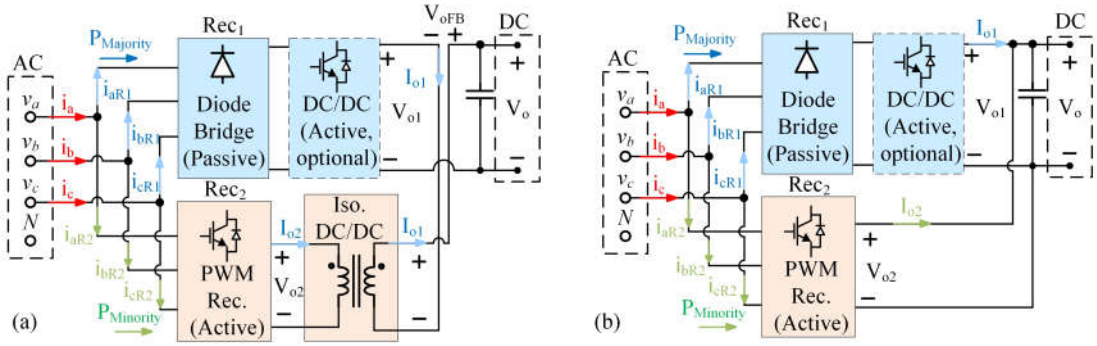

Fig. 1: Hybrid rectifier power flow: (a) IPOS hybrid rectifier. (b) IPOP hybrid rectifier.

high and wide total output voltage range of 800∼1500 V. It is worth noting that semiconductors with higher voltage rating, e.g. 1700 V, can be avoided in the proposed topology because of the serial connection, bringing more design choices and a lower cost on semiconductors. The grid currents are regulated by two rectifier stages, adding up to a sinusoidal waveform.

This paper is structured as follows. The topology derivation of the IPOS hybrid rectifier, theoretical analysis, the control strategy, and the converter parameter design are introduced in Section II. The simulation and analytical loss modelling are presented in Section III. The experimental verification is presented in Section IV. The prime of this paper and the future work are concluded in Section V.

II. Proposed IPOS Hybrid Rectifier Topology

A. Proposed Topology Derivation

The hybrid rectifier can be treated as a black box of two rectifier stages with topology selection based on the application. General requirements placed on a three-phase PFC rectifier system in [5] should be fufiled. In the application of HDEV chargers, specific requirements are listed as follows.

- Scalable to process ultra-high power (>1 MW);
- A high and wide output voltage (800∼1500 V);
- Unidirectional power flow;
- Highly efficient and cost-effective;

In the IPOP topology, the DC-link voltage of each rectifier stage is equal to the total output voltage due to the parallel connection. Thus, a high output voltage (> 1000 V) will require an upscale of voltage ratings from 1200/600 V to 1700/1200 V to safely handle the voltage stress. Consequently, the design space is limited by higher costs and fewer available component options at the required power/voltage rating. The system efficiency will also be compromised because of the high voltage stress on the components.

This limitation brings to the essence of this paper, which is to connect the output DC-links of each converter stage in series (cf. [Fig. 1(a)]). In the IPOS topology, the total output voltage (V_o) is the addition of the DC-link voltage of the Boost PFC rectifier (V_o1) and the isolated DC-DC converter (V_oFB). Notably, the average output current of Rec.1 equals that of the isolated converter, and the total output current I_o. Therefore, the power-sharing of each converter stage is determined by the proportion of the average DC-link voltage in the total output voltage as Eq. 1. α_series addresses the power-sharing ratio on the Rec. 2 plus the isolated DC-DC converter path for the IPOS topology. By altering the DC-DC output voltage V_o1 and V_oFB, the power shared on each path can be changed accordingly. Note that an isolated DC-DC converter is required at the DC-link output to prevent the circulating current between two rectifier stages. The reference DC-link voltage of the PWM rectifier (V_o2) does not influence the power-sharing ratio. The power processed by two rectifier stages are defined as (P_o1, P_o2) respectively. α is an important property since it is closely related to the system efficiency and the grid current $\mathrm{THD_i}$.

$$\alpha_\mathrm{series} = \frac{P_\mathrm{o2}}{P_\mathrm{o}} \approx \frac{P_\mathrm{oFB}}{P_\mathrm{o}} = \frac{I_\mathrm{oFB}V_\mathrm{oFB}}{I_\mathrm{o}V_\mathrm{o}} = \frac{V_\mathrm{oFB}}{V_\mathrm{o}} \tag{1}$$

A suitable combination of topologies can be selected for the IPOS hybrid rectifier based on the above-mentioned requirements. The DC-link voltage of the line-commutated rectifier is typically higher than the peak value of the three-phase line-to-line voltage ($V_\mathrm{ll,pk}$), which requires a Boost-type PFC rectifier with DC-link voltage and current regulation. For the self-commutated rectifier, a unidirectional T-type rectifier is preferred for its low $\mathrm{THD_i}$ and component stress. The Phase-Shifted Full-Bridge (PSFB) converter is selected as the isolated DC-DC stage for its high efficiency, wide voltage gain range, and simple control. Readers are referred to a more detailed topology derivation in [6].

B. Control Strategy

A classic feedback control is implemented to regulate the DC-link voltage and grid current of the IPOS hybrid rectifier (cf. [Fig. 3]). The Boost PFC rectifier, the T-type rectifier, and the PSFB converter are controlled separately.

1) Voltage control loop: The DC-link voltage of each stage needs to be controlled separately since its proportion in the total output voltage determines the power processed by each stage. The DC-link voltage of the Boost PFC is set to be $(1-\alpha)\cdot V_\mathrm{o}$ with a maximum value of 960 (1200×0.8) V, constrained by the maximum blocking voltage of the 1200 V semiconductor. The DC-link voltage of the T-type rectifier is set to a constant 650 V. The desirable voltage gain of the PSFB

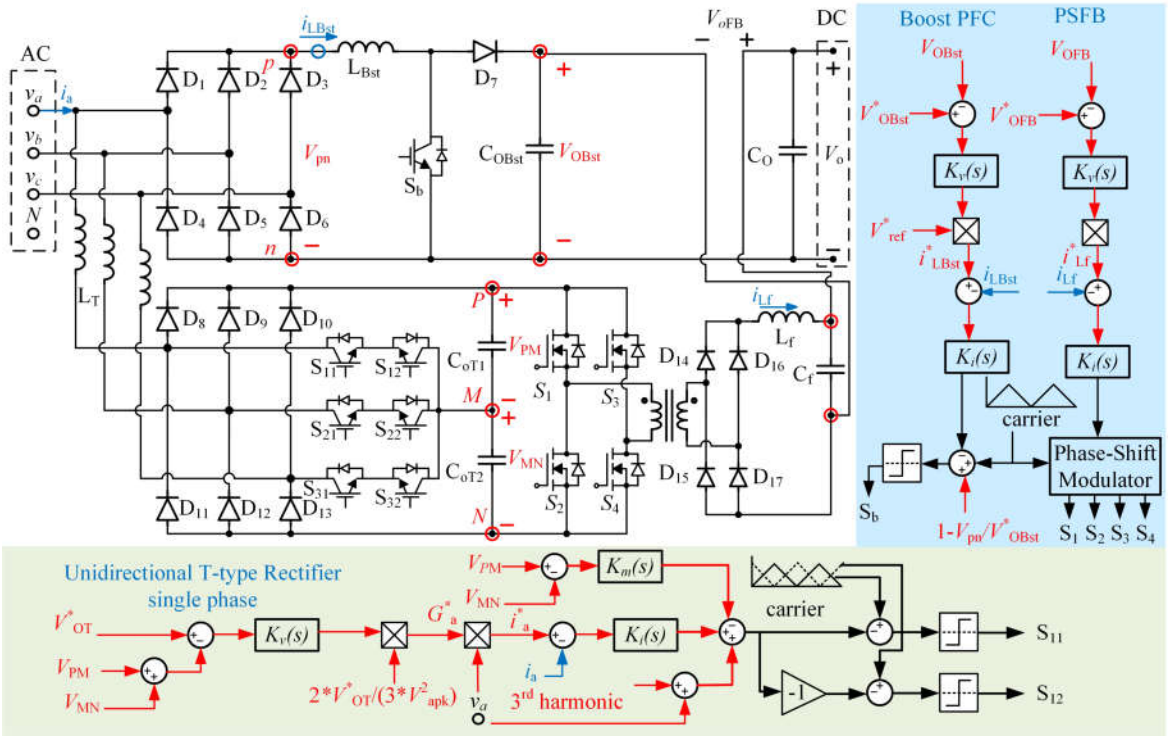

Fig. 3: Proposed hybrid rectifier topology and the control scheme

is determined by the phase shift between the switches on the leading leg and the lagging leg generated by the phase-shift modulator. By altering the DC-link voltage reference value of the DC-DC stage, the desirable power sharing ratio can be achieved. Moreover, the total output voltage, which is the addition of the DC-link voltage of the Boost PFC rectifier and the PSFB converter, can achieve a high and wide range.

2) Current control loop: The grid current regulation is achieved by the current feedback control. For the Boost PFC rectifier, the output of the voltage compensator is multiplied with a voltage reference signal v^*_{ref} obtained from fragments of the grid voltage to generate the current reference i^*_{LBst} ([cf. Fig. 4 and Table. I]) [3]. The inductor current i_{LBst} is then sensed and compared to i^*_{LBst}, with the error sent to the current compensator $K_{\text{i}}(s)$. The output of $K_{\text{i}}(s)$ is added by a feed-forward signal, which is the preset duty-cycle derived from the voltage gain of a Boost converter regarding the six-pulse output voltage of the three-phase diode bridge as the input, and a reference DC-link voltage as the output. The PWM modulator generates the gate signal of the Boost switch. As a result, the inductor current and the input current of the passive diode bridge can be imposed.

Singal phase Sinusoidal Pulse Width Modulation (SPWM) is applied for the current control of the T-type rectifier. Similar to the Boost PFC control, the output of the voltage compensator $K_{\text{v}}(s)$ is multiplied by a gain to derive the line frequency transconductance G^*_{a}, which is then multiplied by the sensed sinusoidal grid voltage v_{a} to generate a sinusoidal line current reference signal i^*_{a}. The sensed grid current i_{a} is compared to the reference current and the error is sent to a current compensator $K_{\text{i}}(s)$. The output of $K_{\text{i}}(s)$ is then superimposed on a feedforward grid voltage signal v_{a} which presets the duty cycle of the SPWM operation [3]. Incorporating a voltage balance control of the two DC-link capacitor voltages V_{PM} and V_{MN} through another compensator $K_{\text{m}}(s)$, the gate signals are generated to control the bidirectional switches. This control scheme enables the T-type rectifier to generate a phase current waveform in compensation for the imposed current on the passive three-phase diode bridge to form a sinusoidal grid current ([cf. Fig. 4(c)]).

TABLE I: Generation of current reference signal [3]

Interval	v_{ref}	Interval	v_{ref}	Interval	v_{ref}
0°-30°	v_{a}	120°-150°	v_{b}	240°-270°	v_{c}
30°-60°	$-v_{\text{b}}$	150°-180°	$-v_{\text{c}}$	270°-300°	$-v_{\text{a}}$
60°-90°	$-v_{\text{c}}$	180°-210°	$-v_{\text{a}}$	300°-330°	$-v_{\text{b}}$
90°-120°	v_{a}	210°-240°	v_{b}	330°-360°	v_{c}

3) Constraints of the unidirectional power flow: The unidirectional power flow of the T-type rectifier imposes constraints on the current modulation and the power-sharing ratio. Readers are referred to a detailed derivation in [6]. As a result, minimum power of $23\% \cdot P_{\text{o}}$ needs to be processed by the T-type rectifier to achieve effective PFC. If the power processed by the Boost PFC is larger than $1-\alpha_{\text{min}}$, the magnitude of the imposed diode current i_{Da} will be larger than the grid current reference value in certain time intervals. The T-type will have to provide an input current i_{Ta} with an opposite sign such that

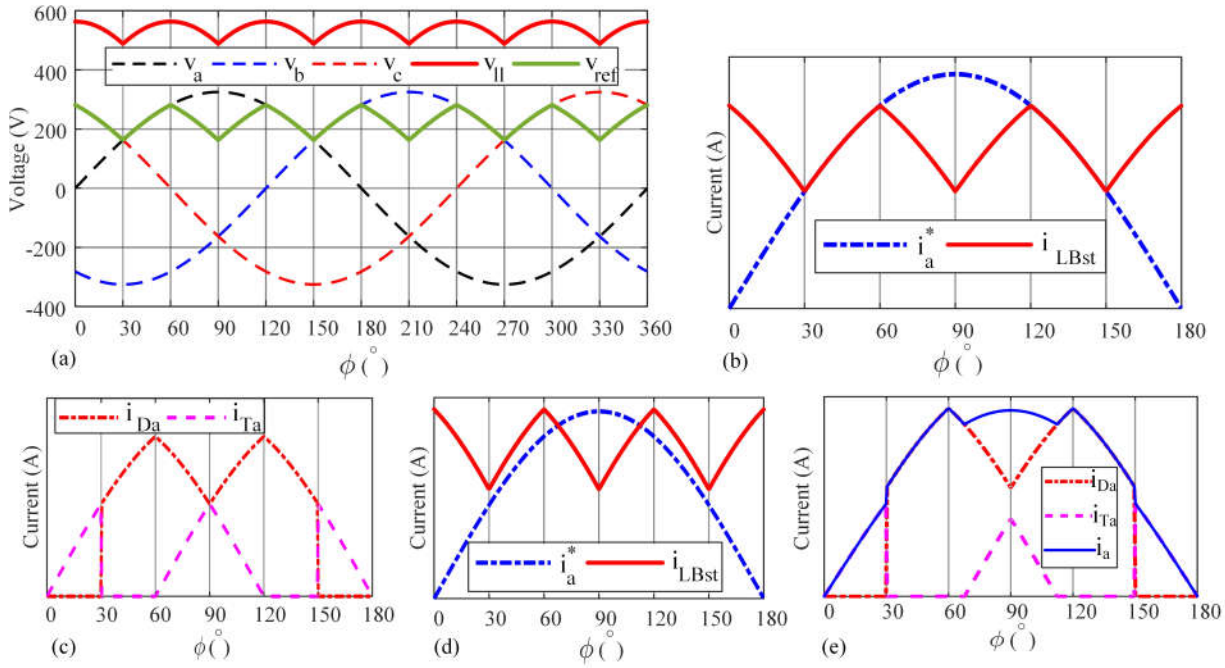

Fig. 4: Analytical current waveforms: (a) Generation of current reference signal. (b) Mains reference current and Boost inductor current, $\alpha = \alpha_{\text{min}} = 0.23$. (c) Bridge diode current and T-type inductor current, $\alpha = \alpha_{\text{min}} = 0.23$. (d) Bridge diode current and T-type inductor current, $\alpha < \alpha_{\text{min}}$. (e) Bridge diode, mains, and T-type inductor current, $\alpha < \alpha_{\text{min}}$.

the addition of these two currents can be sinusoidal (cf. [Fig 4(d) and (e)]). However, due to the unidirectional power flow, this can no be achieved. Therefore, the current modulation is no longer valid in these time intervals, deteriorating the grid current THD_i and the PF.

It is worth noting that the power-sharing is still determined by the DC-link voltage proportion even with distorted grid current. The power-sharing ratio is only the constraint of an effective PFC operation. Instead, if a bidirectional PWM rectifier is applied for Rec.2, the line-commutated Rec.1 can process 100% of the output power P_o. The PWM rectifier will only process reactive power as a shunt filter [3].

C. Converter Parameter Design

Readers are referred to [6] for the parameter designs of the passive components in each converter stage. Note that due to the power-sharing scheme, the corresponding equations may differ from the original ones.

III. Simulation And Modelling Results

A. Simulation results

The system specifications are listed in Table. II. The power rating is selected to be 50 kW where an abundance of available semiconductor devices can be selected for the analytical loss modelling. The power rating and DC-link voltage range of each stage are determined by their maximum processed power.

The simulation results at V_o=1200 V are shown in Figs. 5 and 6. The results are obtained under two power-sharing ratio to test the PFC control. It can be observed that the DC-link voltage of each stage can be stabilized at their reference value, delivering a total 1200 V output voltage regardless of the power-sharing. For the current modulation, the T-type rectifier is able to compensate for the current shape of the imposed diode bridge when $\alpha \geq \alpha_{\text{min}}$, forming a close-to-sinusoidal grid current (cf. [Fig. 6(a)]). The grid input current total demand distortion (TDD) is $1.97\% < 5\%$ with its individual harmonic component in compliance with the IEEE-519 standard, implying that no added filtering stages are required (cf. [Fig. 6(b)]). Nevertheless, protection circuits, Electromagnetic Interference (EMI) filters, and LCL filters

TABLE II: System specifications

RMS Input mains voltage $v_{\text{a,b,c}}$ (V)	230
Mains frequency f_m (Hz)	50
System power rating P_o (W)	50k
Boost switching frequency $f_{\text{sw,Bst}}$ (Hz)	5k
T-type switching frequency $f_{\text{sw,T}}$ (Hz)	20k
PSFB switching frequency $f_{\text{sw,fb}}$ (Hz)	20k
Total DC-link voltage V_o (V)	1200
Boost DC-link voltage $V_{\text{o,Bst}}$ (V)	924 (1200×0.77)
T-type DC-link voltage $V_{\text{o,T}}$ (V)	650
PSFB DC-link voltage $V_{\text{o,fb}}$ (V)	276 (1200×0.23)
Boost DC inductor L_{Bst} (mH)	2.5
T-type filter inductor L_T (mH)	0.3
PSFB filter inductor L_f (mH)	0.33
PSFB transformer leakage inductor L_{lkg} (μH)	30
Boost DC-link capacitor C_{oBst} (μF)	2350
T-type DC-link capacitor C_{oT} (μF)	2000
PSFB DC-link capacitor C_f (μF)	47
PSFB turns ratio n	1

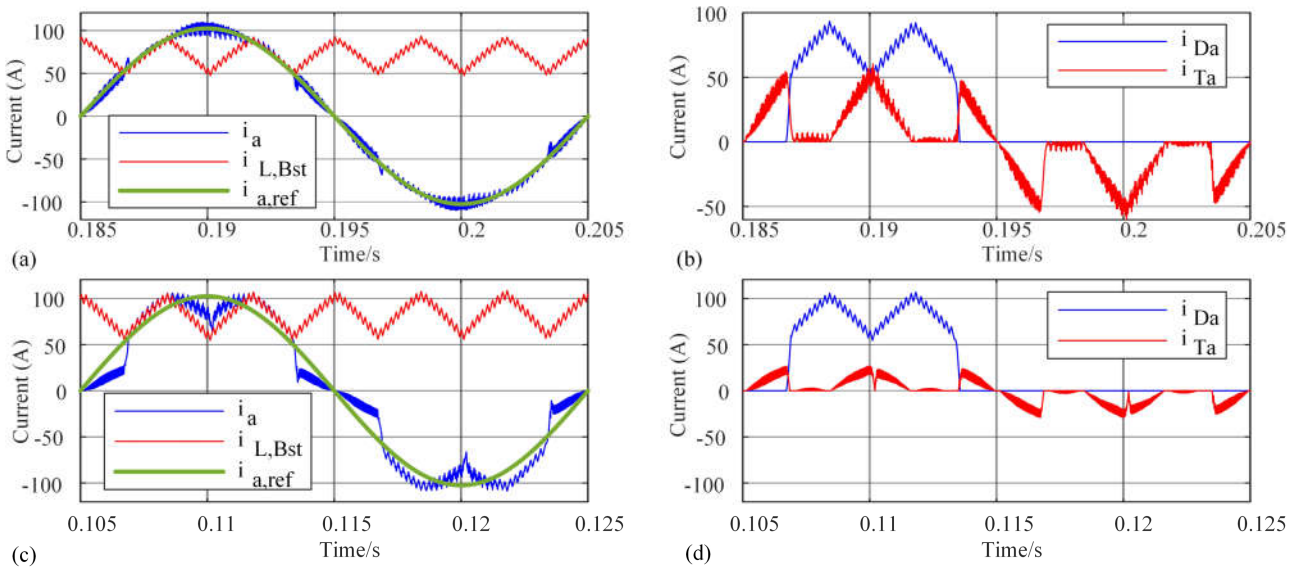

Fig. 5: Simulation current waveforms: (a) grid and Boost inductor currents, $\alpha = \alpha_{\text{min}}$. (b) Bridge diode and T-type inductor currents, $\alpha = \alpha_{\text{min}}$. (c) grid and Boost inductor currents, $\alpha < \alpha_{\text{min}}$. (d) Bridge diode and T-type inductor currents, $\alpha < \alpha_{\text{min}}$.

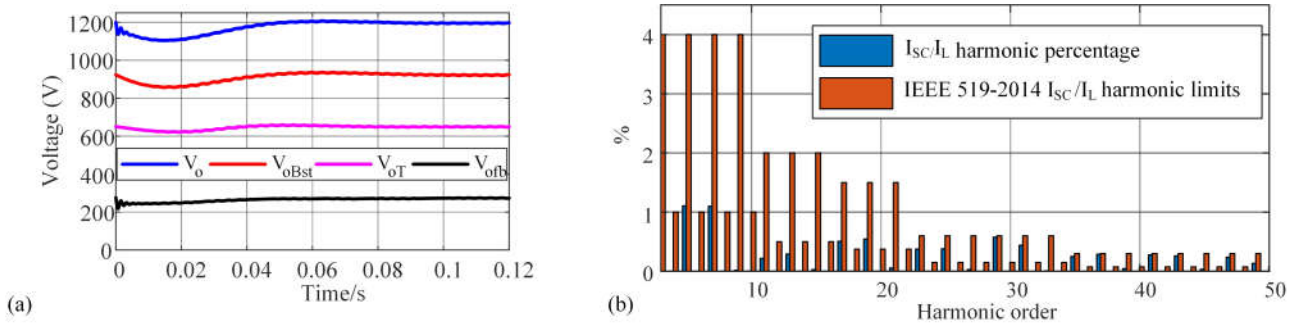

Fig. 6: Simulation results: (a) DC-link voltages. (b) grid current harmonic component, $\alpha = \alpha_{\text{min}}$

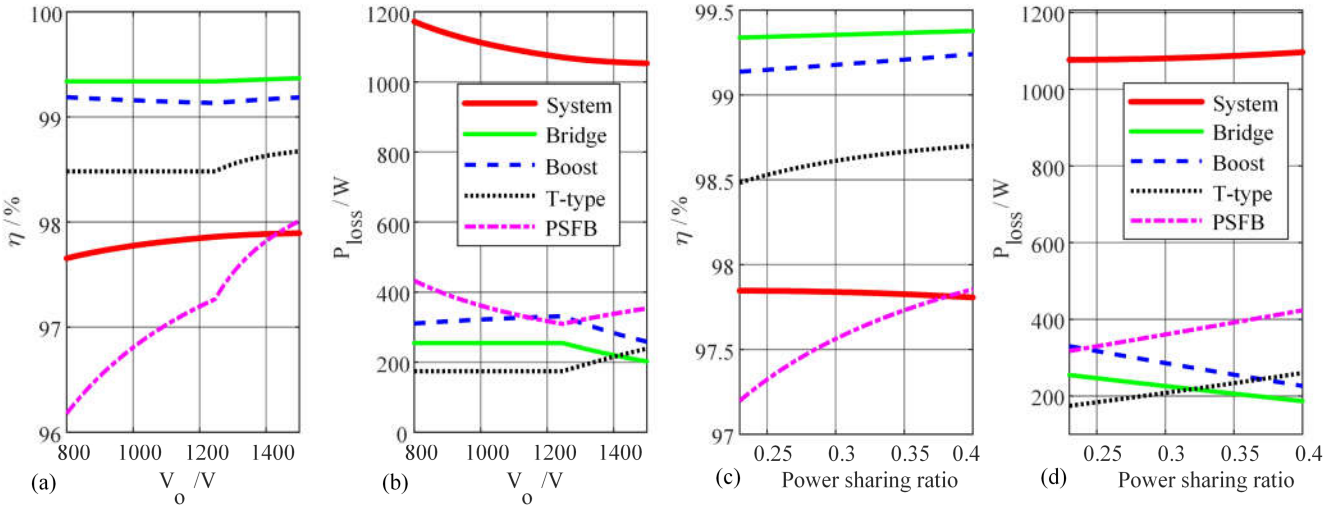

Fig. 7: System efficiency modelling: (a) System efficiency vs. load voltage. (b) System losses vs. load voltage. (c) System efficiency vs. α when $V_{\text{o}} = 1200$ V. (d) System losses vs. α when $V_{\text{o}} = 1200$ V.

are necessary to guarantee an effective PFC under various load conditions for industrial applications. When the power-sharing ratio $\alpha < \alpha_{\min}$, the system loses the unity power factor operation, injecting distorted currents into the grid, which is consistent with the analysis in II-B.

B. Analytical loss modelling results

The loss modelling of the system and each stage are performed under various power-sharing ratio $\alpha = 0.23 \sim 0.4$ and load condition (V_o = 800∼1500 V) using the method in [7] (cf. [Fig. 7(a) and 7(b)]). The system can achieve a peak efficiency of 97.89% under the system specifications in Table. II. It can be observed that the system efficiency declines with the increase of the power-sharing on the T-type rectifier plus the PSFB. Notably, the diode bridge and the Boost stage are highly efficient ($> 99\%$) while the T-type rectifier and the PSFB are less efficient, which is consistent with the analysis in Section II-A.

It can be observed that the system efficiency rises as the load voltage rises. When the output voltage varies from 800∼1246 V (i.e., the maximum blocking voltage of the Boost IGBT, 1200×0.8/0.77), the power-sharing can be maintained as $\alpha_{\min}$ to achieve an optimal system efficiency. The discontinuity at the transition is caused by the change in α. The further increase in the load voltage from 1246∼1500 V can only be provided by the PSFB, rendering the α to increase from 0.23 to 0.36.

IV. Experimental Verification

Experimental verification was performed to attest active PFC control applied in the Boost PFC rectifier. The system specifications are listed in Table. III. The test setup is shown in Fig. 8. The Boost stage is implemented by a phase leg of a 2-level inverter in a rectifier configuration.

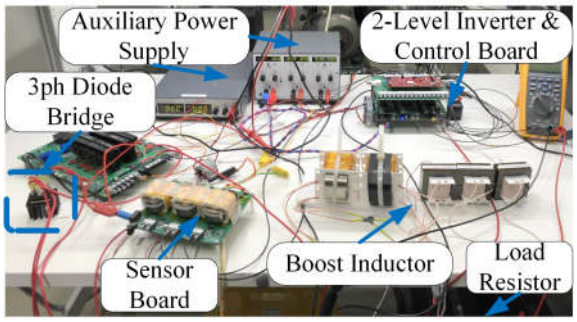

Fig. 8: Experiment setup

TABLE III: Experimental specifications

RMS input line voltage $v_{a,b,c}$ (V)	230
Line frequency f_m (Hz)	50
Power rating P_o (W)	1.2k
Boost switching frequency $f_{sw,Bst}$ (Hz)	36k
Boost DC-link voltage $V_{o,Bst}$ (V)	616 (800×0.77)
Boost DC inductor L_{Bst} (mH)	4.7
Boost DC-link capacitor C_{oBst} (μF)	360

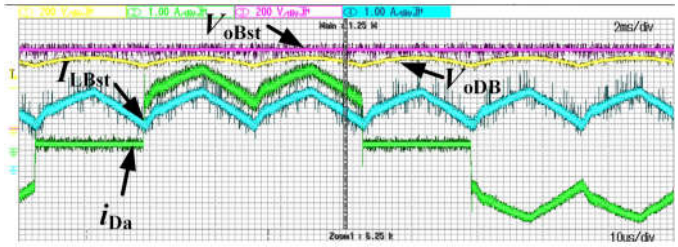

Fig. 9: Experimental results: PFC closed-loop control

The PFC was implemented by the TI2000 DSP to generate the current reference and command the switches. The results are shown in Fig. 9. The DC-link voltage can be stabilized at its reference value. The inductor current is shaped to be the reference waveform in phase with the line voltage.

The results attest the effectiveness of the PFC control scheme in the Boost PFC rectifier, offering desirable DC-link voltage and AC current modulation. Due to the limited resources and time, tests on the T-type rectifier and the IPOS system integration will be carried out in future work.

V. Conclusion And The Future Work

This paper proposed an Input-Parallel-Output-Series (IPOS) hybrid rectifier topology which is able to deliver a high and wide output voltage of 800∼1500 V with 600/1200 V semiconductors. The PPP characteristic yields a high system efficiency under various power-sharing and load conditions without hindering an effective voltage/current regulation and is thus suitable for applications such as ultra-high-power DC-type fast chargers. The feasibility and reasonableness of this solution are verified using a combination of a Boost PFC rectifier, a T-type rectifier, and a PSFB converter by simulation, analytical loss modelling, and experimental verification.

In future work, experimental validation of the whole system shall be carried out. A comparison of the conventional charger solution and the IPOS solution shall be performed analytically. More advantageous combinations of topologies and control schemes shall be explored for the proposed IPOS topology.

References

[1] IEA, "Global ev outlook 2022 – analysis," May 2022. Available at https://www.iea.org/reports/global-ev-outlook-2022.

[2] P. Granello, T. B. Soeiro, N. H. Van der Blij, and P. Bauer, "Revisiting the partial power processing concept: Case study of a 5 kw 99.11 flyback converter-based battery charger," *IEEE Transactions on Transportation Electrification*, pp. 1–1, 2022.

[3] T. B. Soeiro and J. W. Kolar, "Analysis of high-efficiency three-phase two- and three-level unidirectional hybrid rectifiers," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 3589–3601, 2013.

[4] R. Alves, C. Font, and I. Barbi, "A novel unidirectional hybrid three-phase rectifier system employing boost topology," in *2005 IEEE 36th Power Electronics Specialists Conference*, pp. 487–493, 2005.

[5] J. W. Kolar and T. Friedli, "The essence of three-phase pfc rectifier systems—part i," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, 2013.

[6] R. Qiang, "A new input-parallel-output-series three-phase hybrid rectifier for heavy-duty electric vehicle chargers," 2022. Available at http://resolver.tudelft.nl/uuid:6cd95db6-bc4b-4523-99fa-ef2d6695fcc6.

[7] J. Xu, T. B. Soeiro, Y. Wang, F. Gao, H. Tang, and P. Bauer, "A hybrid modulation featuring two-phase clamped discontinuous pwm and zero voltage switching for 99Vehicular Technology, vol. 71, no. 2, pp. 1454–1465, 2022.