

Synchronization Detection in Networks of Coupled Oscillators for Pattern Recognition

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Abstract—Coupled oscillator-based networks are an attractive approach for implementing hardware neural networks based on emerging nanotechnologies. However, the readout of the state of a coupled oscillator network is a difficult challenge in hardware implementations, as it necessitates complex signal processing to evaluate the degree of synchronization between oscillators, possibly more complicated than the coupled oscillator network itself. In this work, we focus on a coupled oscillator network particularly adapted to emerging technologies, and evaluate two schemes for reading synchronization patterns that can be readily implemented with basic CMOS circuits. Through simulation of a simple generic coupled oscillator network, we compare the operation of these readout techniques with a previously proposed full statistics evaluation scheme. Our approaches provide results nearly identical to the mathematical method, but also show better resilience to moderate noise, which is a major concern for hardware implementations. These results open the door to widespread realization of hardware coupled oscillator-based neural systems.

Index Terms—Associative memory; Synchronization; Oscillator network; Classification; Recognition; Neuromorphic

I. INTRODUCTION

The interest for neuro-inspired computing architectures is currently rising considerably, due to the inefficiency of the von Neumann architecture for the treatment of cognitive tasks like recognition or classification of massive amounts of data [1]–[4]. Both academic and industrial groups are focusing efforts on developing efficient physical implementations of artificial neural network architectures, emulating neuronal and synaptic behavior by the means of complex CMOS circuits [5], [6], or relying on the physical properties of emergent technologies, such as spintronics [7], [8], oxide devices [9]–[11] or phase change devices [12].

Inspired by the importance of temporal patterns of activity in neural assemblies in the brain achieving cognitive functions [13], [14], an alternative cognitive architecture consists of building networks of coupled oscillators. The rich dynamics of coupled oscillators can be leveraged to operate classification and recognition tasks [15]–[20], based on the emergence of synchronization patterns among the oscillators of the network. Beyond theoretical studies, experimental implementations of cognitive networks of oscillators have been proposed based on numerous technologies such as CMOS differential oscillators [21], CMOS ring oscillators [22]–[24], or laser oscillators [25]. Additionally, emerging nanotechnologies provide nanometer-scaled oscillators that are exception-

ally compact, have easily tunable frequencies, can be very fast, and show synchronization capabilities that may be used for oscillator-based computing. Examples include spin-torque nano-oscillators [19], [26], [27] or oxide-based relaxation oscillators [28]–[31].

Most of these proposals are based on Hopfield's model, where the construction of the cognitive capabilities of the network (learning) happens by tuning the connections between each pair of oscillators [15], [16]. With emerging nanotechnologies, controlling oscillator coupling with high accuracy can be a difficult challenge. As a consequence, other schemes for computing with coupled oscillators, where the network has fixed connections that do not need to be controlled perfectly, and oscillators have adjustable natural frequencies, are especially attractive as they would face less difficulties with hardware implementation [19], [23], [32], and map well to emerging technologies [26], [28].

In particular, in [32], Vassilieva *et al.* propose a weakly coupled oscillator network for pattern recognition where the coupling strengths between oscillators do not need to be tuned, and the cognitive operations are performed by only changing the natural frequencies of the oscillators. This network is also relatively resilient to oscillator phase noise, a major concern of oscillators based on nanotechnologies. Unfortunately, the readout of such a network remains a challenge from a hardware implementation perspective. It involves the detection of synchronization patterns, and requires the evaluation of synchronization between each pair of oscillators. Achieving this readout with fast, possibly noisy oscillators in real time might even be more complicated than the pattern recognition itself.

Therefore, in this study, we propose and investigate simple, easy to implement schemes for the evaluation of the degree of synchronization between pairs of oscillators, in the context of the oscillator-based recognition architecture of [32]. First, we describe the weakly coupled oscillator network architecture following the proposal of [32] and introduce three protocols for the evaluation of the degree of synchronization between each pair of oscillators. Then, we present and compare the recognition capabilities of the oscillator network obtained when using each readout protocol, in the case of a network of noiseless oscillators as well as in a more realistic case of noisy oscillators. We conclude on the potential for large scale integration of each protocol.

II. DESCRIPTION OF THE CONSIDERED SYSTEM

A. An Oscillator Network for Pattern Recognition

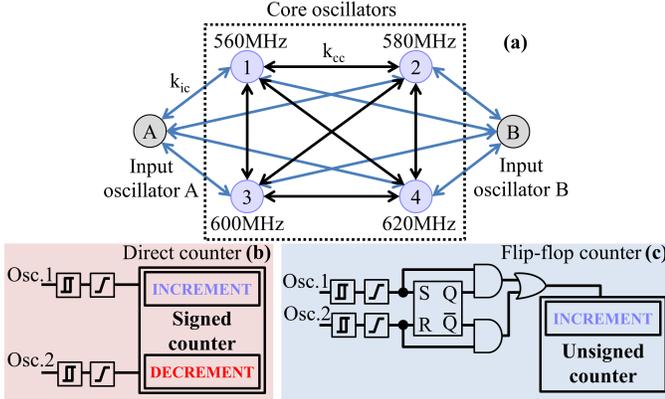


Fig. 1. (a) Illustration of an oscillator network architecture for pattern recognition operation, showing core oscillators, input oscillators, and the corresponding couplings. (b,c) Illustration of proposed schemes for evaluating the degree of synchronization between pairs of oscillators: (b) direct counter evaluation technique, (c) flip-flop counter evaluation technique.

As proposed in [32], we use a network of weakly coupled oscillators for pattern recognition. The considered network is based on a set of oscillators whose natural frequencies are controlled and set by external means (voltage, current, etc.). For the purpose of our demonstration, and as illustrated in Fig. 1(a), the core of the architecture is a small network of four coupled oscillators labeled $\{1,2,3,4\}$. This network is connected to two input oscillators $\{A,B\}$. Such an architecture is able to classify analog patterns $\{s_A, s_B\}$ coded as input oscillators' natural frequencies $\{f_0^{(A)}, f_0^{(B)}\}$ by associating them to different synchronization patterns within the core network. Indeed, the combined influence of the input oscillators induces computation among the core oscillators, by bringing their complex dynamics to converge to given synchronization states. The coupling strengths, together with the natural frequencies of the oscillators, can be tuned by learning algorithms in order to shape the response of the network and classify a desired set of patterns [32].

All the oscillators are modeled using the Kuramoto equation:

$$\dot{\varphi}_n = 2\pi f_0^{(n)} + 2\pi \sum_{m \neq n} k_{mn} \sin(\varphi_m - \varphi_n) + \eta \quad (1)$$

where φ_n is the phase of oscillator n , $f_0^{(n)}$ is its natural frequency and the k_{mn} matrix defines the coupling between the oscillators of the network. η is a Gaussian random noise term with a standard deviation defined by $\sqrt{2\pi \cdot \text{FWHM}/dt}$ so that isolated oscillators' power spectra have a Full-Width at Half Maximum FWHM. These stochastic differential equations were simulated using the Milstein method [33] with a timestep of $100ps$.

To build the recognition network, each core oscillator is coupled to all the others, while input oscillators are coupled to core oscillators only. In this study, we focus on a simple

case where the input-core coupling strengths and the core-core coupling strengths are uniform and defined by k_{ic} and k_{cc} respectively. All couplings are considered bidirectional ($k_{nm} = k_{mn}$). The natural frequencies of the core oscillators are assumed to be equally distributed. Unless otherwise stated, we assume that $k_{ic} = 12 \text{ MHz}$, $k_{cc} = 4 \text{ MHz}$ and the natural frequencies of the core oscillators are set to $\{560, 580, 600, 620\} \text{ MHz}$.

B. Schemes for Evaluating Synchronization Patterns

The readout process of such an architecture involves pairwise synchronization detection between core oscillators, and the output is the resulting list of synchronized pairs. In weak coupling conditions and especially in the presence of phase noise, synchronization between oscillators in its strictest definition is hardly achieved, as perfect phase-locking seldom occurs. Thus, a weaker definition of synchronization is needed and should be based on a measure of the degree of synchronization between two signals. For instance, statistical methods such as the variance measure introduced in [32] can be used to define quasi-synchronization between a pair of oscillators $\{n,m\}$:

$$\text{Var}_\tau(\sin(\varphi_n - \varphi_m)) < \epsilon_v \quad (2)$$

where the variance is evaluated during a limited time τ . A threshold $\epsilon_v \in [0;0.5]$ is chosen to discriminate quasi-synchronized pairs from non-synchronized pairs, $\epsilon_v = 0$ corresponding to a perfect synchronization requirement. This definition was shown to allow the detection of a rich set of synchronization patterns in weakly coupled networks [32]. However, the hardware implementation of such a detection scheme would involve a combination of complex circuits, or an external computing unit: it is not a reasonable readout technique for an efficient physical implementation.

Here, we propose two other quasi-synchronization detection schemes based on operational principles compatible with an easy CMOS implementation and compare their performances with the variance-based method. The oscillator signals are digitized using Schmitt triggers, intended to increase the noise resilience of the readout, after which a rising edge detection is performed to obtain a single pulse per period of the signals.

A first synchronization evaluation approach that is further called "direct counter" is presented in Fig. 1(b). This technique aims at evaluating the difference ΔN_τ between the number of periods of the two signals during a given amount of time τ . The counting is achieved by incrementing or decrementing a counter at each rising edge of the respective signals. The result is then compared to a threshold ϵ_d , and the two oscillators are considered synchronized if $|\Delta N_\tau| < \epsilon_d$.

A second scheme that is further called "flip-flop counter" is presented in Fig. 1(c). This technique exploits the fact that if two signals are synchronized, their rising edges should alternate. A counter is then incremented each time two consecutive rising edges of the same signal are not separated by a rising edge of the second. Again, after the evaluation time τ , the two oscillators are considered synchronized if the final value of the counter is strictly lower than a given threshold ϵ_f .

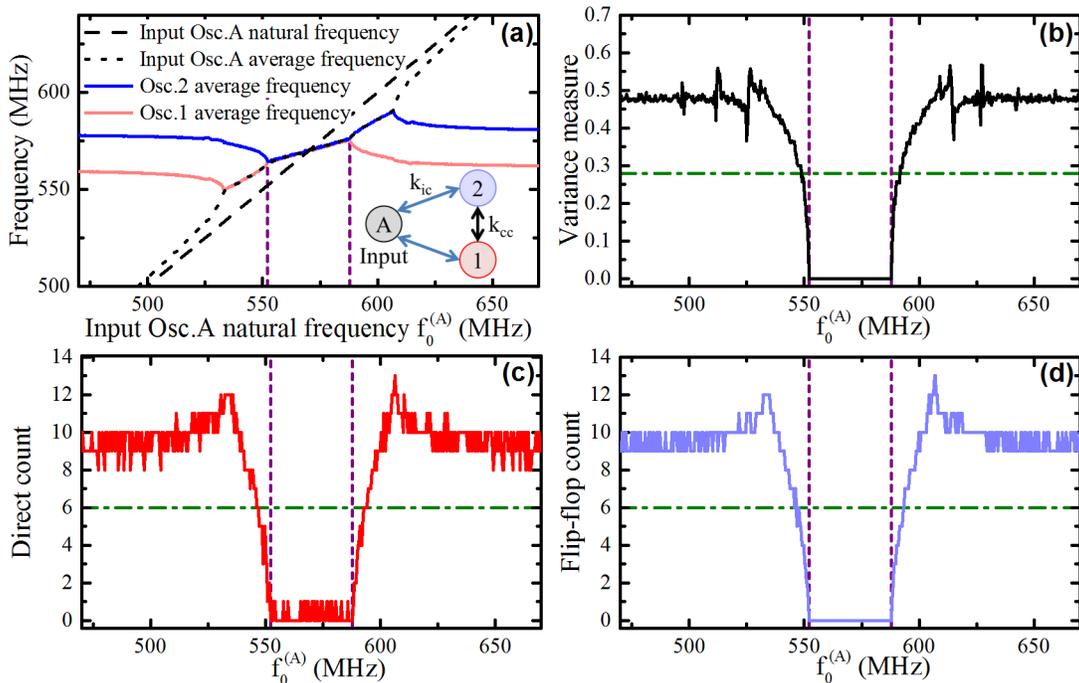


Fig. 2. Simulations in a simplified, noiseless situation with two core oscillators with fixed natural frequencies $\{f_0^{(1)}, f_0^{(2)}\} = \{560, 580\}$ MHz, and one input oscillator whose natural frequency $f_0^{(A)}$ is varied. (a) Average frequencies of the three oscillators as a function of $f_0^{(A)}$. The quasi-synchronization of the two core oscillators is evaluated using the three readout schemes, and their outputs are plotted as a function of $f_0^{(A)}$ for (b) variance measure, (c) direct counter, and (d) flip-flop counter schemes. Vertical purple dotted lines indicate the range of perfect synchronization between oscillators 1 and 2. Horizontal green dotted lines correspond to selected thresholds under which oscillators are declared quasi-synchronized.

Because they use only limited information from the signals, the two counter-based schemes differ conceptually from the variance measure which depends on the full time dependence of the phase difference between the two oscillators. We also highlight the major difference between the two counter-based schemes: while the direct counter method measures an average frequency difference during the total evaluation time, the flip-flop counter takes into account and sums up every detected local desynchronization event. Yet, the physical implementation of the flip-flop counter would require less components, mainly because of the simpler, unsigned counter it uses.

C. Equivalence of the Detection Schemes

To compare the synchronization evaluation schemes, we first investigate the simplified case of a single input oscillator $\{A\}$ and two core oscillators $\{1, 2\}$, as illustrated in Fig. 2(a). Core oscillators' natural frequencies are set to $\{f_0^{(1)}, f_0^{(2)}\} = \{560, 580\}$ MHz and the input oscillator's natural frequency $f_0^{(A)}$ is swept from 470 to 670 MHz. Fig. 2(a) captures the synchronization phenomenon between the three oscillators by showing the evolution of their average frequencies. While the coupling between core oscillators $\{1, 2\}$ is initially too weak for them to synchronize, they are eventually brought to synchronization when the input oscillator's natural frequency lies in a limited range.

For every simulation, the oscillator network dynamics are computed for $1\mu s$. After a $0.5\mu s$ cool-down time to wait for the convergence of the network dynamics, the three detection

schemes are evaluated during $\tau = 0.5\mu s$ between core oscillators $\{1, 2\}$. Their outputs are plotted in Figs. 2(b,c,d) before the thresholding operation.

The three curves appear extremely similar. It is surprising to note that, while variance measure and counter approaches use different basic principles, the obtained curves can actually almost be superimposed. All exhibit a very distinct dip to a zero-value when the two core oscillators are synchronized, and a high plateau value when the oscillators are desynchronized. In the intermediate range, where the oscillators are quasi-synchronized, the outputs show a progressive increase, allowing to define thresholds that will discriminate whether the oscillators are quasi-synchronized or not.

From these curves, we choose equivalent thresholds for the three detection schemes: $\epsilon_v = 0.28$ for the variance measure scheme, $\epsilon_d = 6$ for the direct counter scheme, and $\epsilon_f = 6$ for the flip-flop counter scheme. In the following we use these threshold values if not stated otherwise.

III. PATTERN RECOGNITION AND COMPARISON OF THE READOUT SCHEMES

We now evaluate the three readout schemes on the full coupled oscillator network of Fig. 1(a), introduced in section II-A.

A. Readout Maps in the Absence of Noise

Figs. 3(a,b,c) present the readout maps of the synchronization patterns in the core network, as a function of the input oscillators' natural frequencies $\{f_0^{(A)}, f_0^{(B)}\}$ in the case of

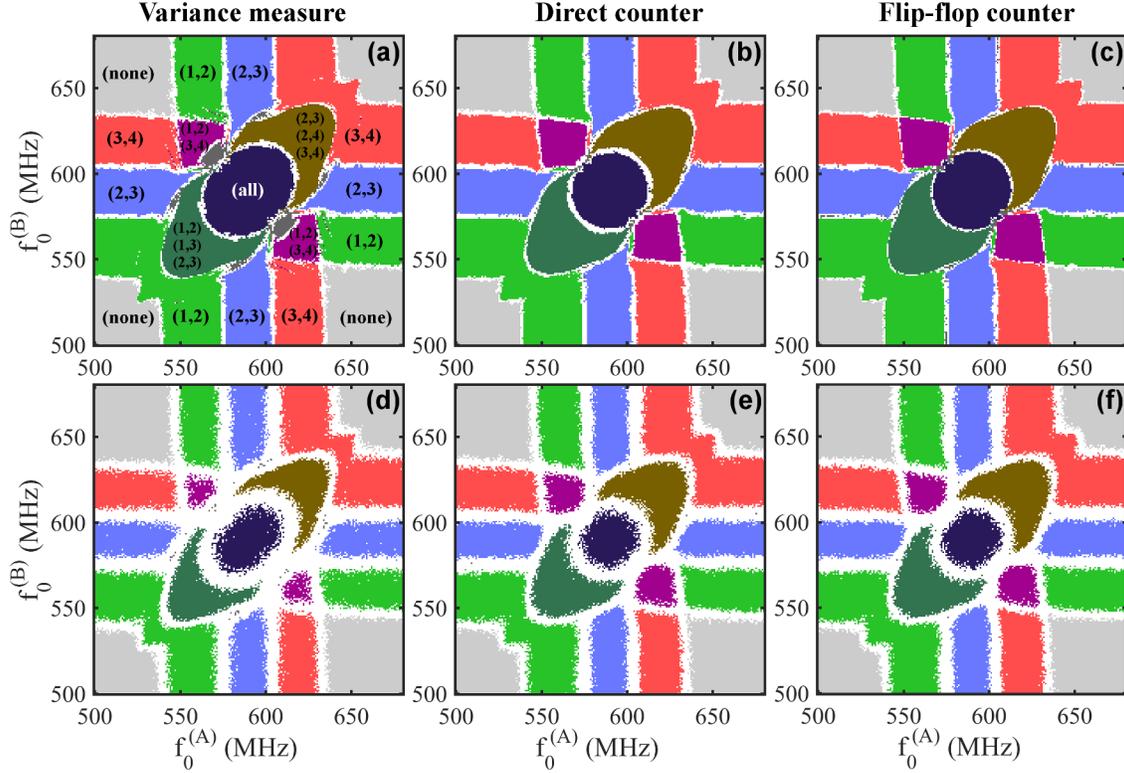


Fig. 3. Readout maps showing the distribution of synchronization patterns among core oscillators as a function of the two input oscillators' natural frequencies $f_0^{(A)}$, $f_0^{(B)}$, as detected by the three readout protocols. Each color is associated to a single synchronization pattern, as specified on Fig.(a). The (a,b,c) maps are obtained in a situation with noiseless oscillators, (d,e,f) maps are obtained for oscillators with phase noise corresponding to FWHM=1 MHz. Readout maps are evaluated respectively using: (a,d) the variance measure scheme, (b,e) direct counter scheme, and (c,f) flip-flop counter scheme.

noiseless oscillators ($\eta = 0$). They are obtained using the variance measure, direct counter and flip-flop counter detection schemes respectively.

For each point in this map, the oscillator network dynamics are simulated for $1\mu s$. After a $0.5\mu s$ cool-down time to wait for the convergence of the network dynamics, the three detection schemes are performed on each of the six pairs of core oscillators during $\tau = 0.5\mu s$, and the results are compared to their respective thresholds. For each simulation, an output list of synchronized pairs is then given by each readout scheme. To account for the robustness of the readout results to initial conditions, each point on the map is simulated ten times with random initial phases. If the ten simulations do not result in the same output synchronization pattern, the point is discarded as "inconsistent" and left blank on the map. If the ten simulations yield identical results, the point is then colored on the map according to the output pattern.

Producing these 200×200 -point maps, to allow precise assessment of the coupled oscillator network behavior, comes at a high computational cost as it requires $200 \times 200 \times 10 = 400,000$ independent simulations per map. For optimal efficiency, the simulations were performed on a nVidia Tesla K20 GPU, using the Cuda Thrust C++ library.

In this noiseless example, the three evaluation schemes yield rich output maps, with large and well-defined regions associated to different synchronization patterns. The boundary

regions (blank) where no repeatable readout is obtained are relatively small. These results show the efficient recognition capability of the oscillator network, as already pointed out in [32]. Indeed, it spontaneously discriminates inputs through the establishment of synchronization patterns in its core. Additionally, it is remarkable that all of the introduced synchronization detection schemes are operational and lead to highly similar readout maps.

The capabilities of the oscillator network associated with each readout scheme are evaluated through the number of classes of patterns the architecture is able to discriminate, *i.e.* the number of regions with different readouts that appear on the map. In this counting, we choose to ignore isolated points, as well as porous regions where consecutive points do not consistently yield the same output. To do so, a filter is applied on the readout maps, as illustrated on Fig. 4, that only keeps regions which yield identical outputs in an at least 3 MHz radius area. This ensures that the counted classes are represented by large and continuous regions that are tolerant to small input variations.

In the case of both counter-based readouts, eight patterns are discriminated, each one being associated to a different synchronization pattern. Meanwhile, a ninth output pattern appears for the variance-based readout.

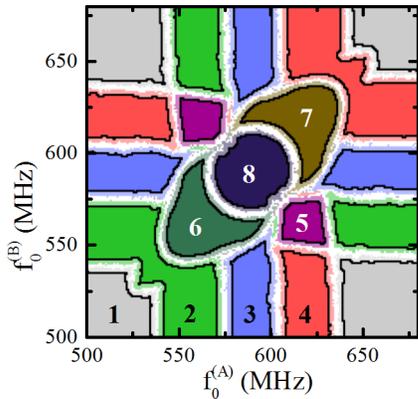


Fig. 4. Effect of the filter applied to the readout maps for counting discriminated patterns. This is illustrated in the case of the readout map obtained for a noiseless network and the flip-flop counter detection scheme (see Fig. 3(c)). Saturated regions delimited by a black line are considered robust and kept by the filter, pale areas are ignored. The numbers on the map index the eight unique discriminated patterns.

B. Readout Maps in the Presence of Noise

When considering hardware implementations, especially based on nanotechnology such as proposed in [19], [26]–[29], [31], the consequences of the phase noise of the oscillators, which can significantly perturb the network dynamics, needs to be considered. To account for it, we reproduced the simulations of the network dynamics as well as the three readout schemes including a non zero noise corresponding to oscillators’ FWHM = 1 MHz.

We show in Fig. 3(d,e,f) the readout maps obtained for the noisy oscillator network. Again, for all three detection schemes, the three maps remain very similar. Compared to the noiseless network, the class regions are sensibly reduced, and the blank (inconsistent) regions are getting wider, as could be expected. Indeed, as the noise increases, the repeatability of the readouts becomes an increasing issue. It notably has an impact on the readout map obtained through the variance-based scheme. As one can see in Fig. 3(d), the ninth synchronization pattern is no longer observed, and the purple region has become particularly porous.

C. Testing Detection Schemes Against Different Network Parameters

Modifying the coupling strengths between oscillators in the network changes the distribution of synchronization patterns, and also has an influence on the relative phase dynamics between coupled oscillators, and subsequently on the synchronization readout. To compare the detection schemes in the case of other network configurations, we repeated the simulations of noisy networks with varying input-core coupling strengths k_{ic} and core-core coupling strengths k_{cc} . Fig. 5(a) shows the number of discriminated classes of inputs when $k_{cc} = 4$ MHz is kept constant and k_{ic} is varied. Fig. 5(b) shows the number of discriminated classes of inputs when $k_{ic} = 12$ MHz is kept constant and k_{cc} is varied.

The two counter-based readout schemes provide quasi-identical results. Both plots show that optimal coupling

strengths, for which a maximum number of classes can be discriminated, fall in the same range for the three readout schemes. However, the counter-based schemes lead to the discrimination of a higher number of classes than the variance-based one in large ranges of coupling strengths. These observations suggest that the counter-based definitions of quasi-synchronization might be more robust than the variance-based one. We discuss and interpret this idea in the next section.

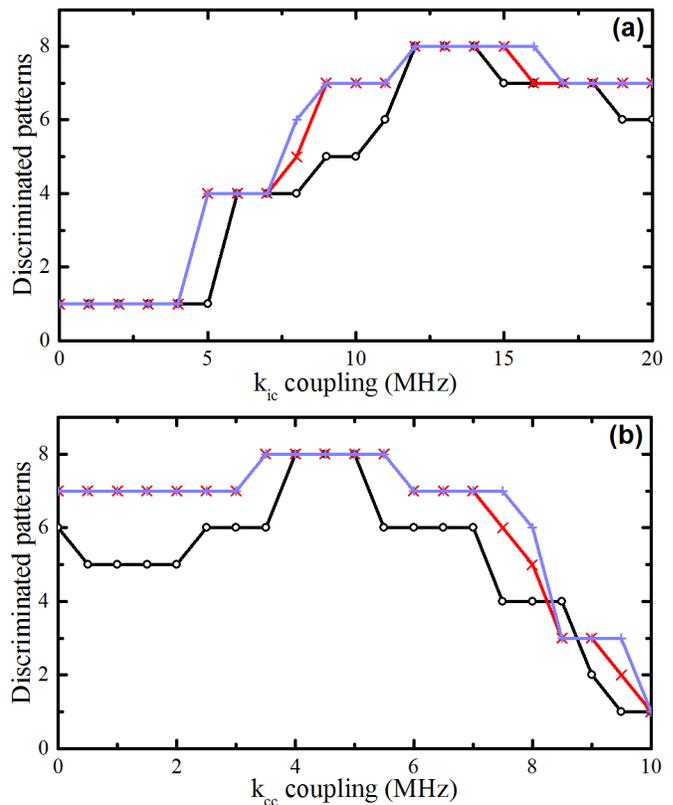


Fig. 5. Number of discriminated patterns within the core network as a function of (a) input-core k_{ic} coupling and (b) core-core k_{cc} coupling as evaluated using the three detection schemes. Simulations performed with FWHM = 1 MHz.

IV. SENSITIVITY OF THE READOUT SCHEMES TO NOISE AND PARAMETERS

In this section, we perform an in-depth evaluation and comparison of these schemes, and discuss their applicability for a final hardware system.

A. Resilience to Noise of the Readout Schemes

To assess the relative influence of phase noise on the three readout schemes, we repeat the simulations of the noisy network with increasing noise levels and plot the evolution of the number of classes discriminated by each readout method in Fig. 6. The three schemes show different resiliences to noise.

For low noise levels, the variance-based scheme shows the lowest resilience, as it is the first detection scheme that stops being able to discriminate eight classes. Indeed, the variance measure is strongly affected by fluctuations appearing in the

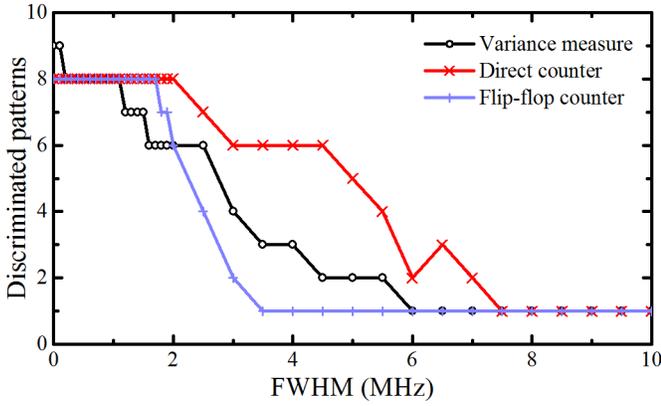


Fig. 6. Number of discriminated patterns as a function of oscillators' FWHM, as evaluated using the three detection schemes.

phase difference dynamics. Moreover, an identical number of phase-slip events can have dramatically different consequences depending on the synchronization recovery duration. Therefore, when looking at the outputs before thresholding, we observe an increasing spreading of the results for the ten repeated simulations with increasing phase noise. This induces spurious detections of synchronization or desynchronization producing many inconsistent points, which leads to the disappearance of some classes in the readout map.

The two counter-based schemes keep their ability to discriminate eight patterns for higher noise levels, even beyond 2 MHz for the direct counter scheme. They evaluate the exact number of desynchronization events and are not sensitive to their dynamics. However, the flip-flop counter scheme appears to fail very rapidly when the FWHM of the oscillators goes above 2 MHz, even faster than the variance-based scheme. In the flip-flop counter detection method, every desynchronization event, *i.e.* phase slip between the two signals, is detected and counted. As the noise level increases, many spurious desynchronization events get detected, which eventually leads the counter to go above the threshold. Only strong synchronizations are then detected. This observation suggests that the threshold level should be raised to adapt to high phase noise oscillator networks.

Because it simply evaluates an average frequency difference between the two noisy signals, the direct counter scheme is the one showing the best resilience to noise. It is still able to discriminate six classes of inputs for oscillators with FWHMs up to 4.5 MHz, when other readout methods only discriminate one or two classes.

B. Influence of the Choice of the Threshold

We have seen that in the presence of noise, the three readout methods may suffer difficulties to detect quasi-synchronization. In these conditions, the initial choice of the thresholds, in an oversimplified case and for a noiseless network, should be reconsidered. We now analyze the impact of the choice of the threshold on the number of recognized patterns. Fig. 7(a,b) shows the total number of discriminated classes for the FWHM = 1 MHz (solid lines) and for the

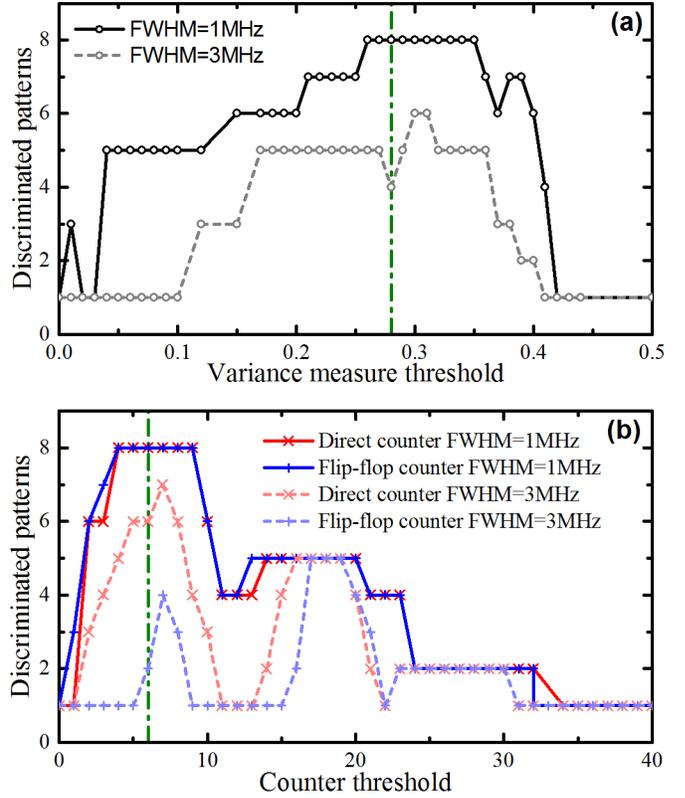


Fig. 7. Number of discriminated patterns, (a) as a function of the threshold ϵ_v when using the variance measure technique, (b) as a function of the counter threshold when using the direct counter and flip-flop counter techniques. The FWHM of the oscillators is set to 1 MHz (solid lines) and 3 MHz (dotted lines). Vertical green dotted lines indicate the thresholds that were chosen in section III-A and used in the simulations to obtain readout maps.

FWHM = 3 MHz (dotted lines) noisy networks as a function of the variance and counter thresholds.

In the case of low phase noise (FWHM = 1 MHz), all three readout techniques identify the maximum number of patterns (eight) for a reasonable range of thresholds. When increasing the thresholds, the variance based detection method rapidly fails when the threshold ϵ_v is chosen above 0.4. On the other hand, the thresholds for counter-based methods can be increased even above 20 without failing (five patterns are still detected), much above the maximum counts observed in III-A.

As noticed in section IV-A, when the FWHM of oscillators reaches 3 MHz, the three readout methods detect different numbers of patterns using the thresholds chosen initially: six for the direct counter scheme, four for the variance-based scheme, and only two for the flip-flop counter scheme. The presented plots show that these initial choices are not adapted to the higher noise case, and that other optimal thresholds can be found. The direct counter approach still shows the best resilience to noise as up to seven synchronization patterns can be read, while the variance measure approach is limited to detecting up to six patterns. In the counter-based approaches, the optimal thresholds are close to our initial choices, yet the optimal ranges are substantially reduced. For the flip-flop

counter scheme, the optimal threshold is found around 18, confirming that high noise induces the spurious detection of many desynchronization events.

C. Influence of the Evaluation Time

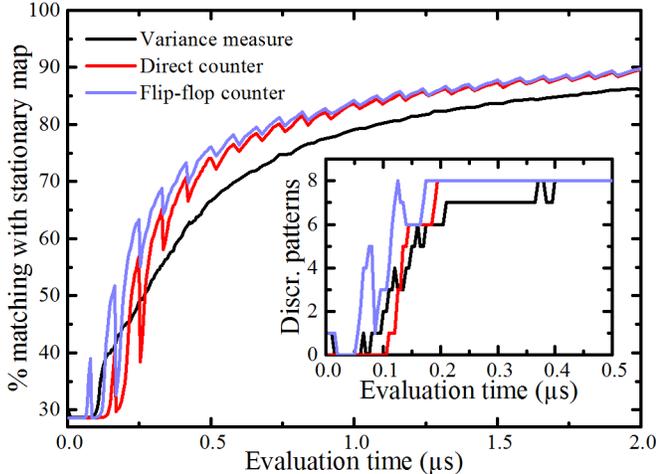


Fig. 8. Matching percentage between the readout map obtained for a limited integration time τ and the readout map obtained for a long $100\mu\text{s}$ integration time, as a function of τ and for the three detection protocols. The inset shows the number of discriminated patterns detected by the three methods as a function of integration time. Simulations are performed with FWHM = 1 MHz.

The synchronization evaluation time τ is an important trade-off for the readout operation, between the speed for recognition and the robustness of the results. Simulations of the recognition networks are performed with varying evaluation time, between 0 and $2\mu\text{s}$. The cool-down time is kept to $0.5\mu\text{s}$, and the FWHM of the oscillators is 1 MHz. The results are compared to the readout obtained in the case of a long evaluation time $\tau = 100\mu\text{s}$ for which the readout is considered stationary and further used as a reference.

In Fig. 8, we plot the percentage of matching points between the obtained readout maps and the reference map, as a function of τ and for each readout scheme. The figure inset also shows the evolution of the detected number of patterns as a function of τ . For equivalence in the case of the counter-based detection schemes, the thresholds are adjusted as τ varies so that $\lfloor \epsilon_{\{d,f\}}/\tau \rfloor$ is kept equal to $12\mu\text{s}^{-1}$.

We observe a fast convergence of the readout maps for evaluation times up to $0.5\mu\text{s}$ above which the convergence starts slowing down. After $2\mu\text{s}$, the counter-based readout schemes reach 90% matching with the reference, while the variance-based scheme lags behind. For the counter-based methods, the maximum number of patterns (eight) is already detected when $\tau > 0.2\mu\text{s}$, while $\tau > 0.4\mu\text{s}$ is needed for the variance measure scheme. In all case, the choice of $\tau = 0.5\mu\text{s}$ then offers a reasonable trade-off as the maximum number of patterns is already discriminated.

V. CONCLUSION

In this work, we have introduced two simple techniques (direct counter and flip-flop counter) for evaluating the output of coupled-oscillator based recognition networks. Both counters-based approaches are simple to implement in hardware, and were compared to a hardware-implausible, more conventional approach (variance measure).

In situations with oscillators with no or low phase noise, the readouts of all three techniques appear very similar. Although variance measure is the most complex, it is not the most robust to noise, and may actually identify less synchronization patterns in some situations with intermediate noise levels and very weak coupling between core oscillators. The variance measure also appears to converge slower than counter-based approaches, hence requiring longer evaluation time for equivalent precision.

When both counter-based protocols show equivalent results, the flip-flop counter is the best choice for hardware implementation, as it relies simply on an unsigned counter. However the flip-flop counter protocol appears to fail at high noise levels, when it detects a lot of spurious desynchronization events. Nonetheless, the direct counter protocol also shows strong resilience to high noise, again better than the variance measure. The choice between these two techniques should therefore be based on the amount of noise.

These results give credibility to the idea of coupled oscillator-based recognition networks, and open the way for their implementation, either with CMOS technology or emerging nanotechnologies.

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REFERENCES

- [1] Yen-Kuang Chen, J. Chhugani, P. Dubey, C. Hughes, Daehyun Kim, S. Kumar, V. Lee, A. Nguyen, and M. Smelyanskiy, “Convergence of Recognition, Mining, and Synthesis Workloads and Its Implications,” *Proceedings of the IEEE*, vol. 96, no. 5, pp. 790–807, May 2008.
- [2] T. Shibata, “Bio Inspired Architectures in the Nanoscale Integration Era,” *ECS Transactions*, vol. 25, no. 7, pp. 49–64, Sep. 2009.
- [3] G. Indiveri and S.-C. Liu, “Memory and information processing in neuromorphic systems,” *Proceedings of the IEEE*, vol. 103, no. 8, pp. 1379–1397.
- [4] D. Querlioz, O. Bichler, A. Vincent, and C. Gamrat, “Bioinspired programming of memory devices for implementing an inference engine,” *Proceedings of the IEEE*, vol. 103, no. 8, pp. 1398–1416.
- [5] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar, and D. S. Modha, “A million spiking-neuron integrated circuit with a scalable communication network and interface,” *Science*, vol. 345, no. 6197, pp. 668–673.

- [6] B. Benjamin, P. Gao, E. McQuinn, S. Choudhary, A. Chandrasekaran, J.-M. Bussat, R. Alvarez-Icaza, J. Arthur, P. Merolla, and K. Boahen, "Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations," *Proceedings of the IEEE*, vol. 102, no. 5, pp. 699–716.
- [7] K. Roy, M. Sharad, D. Fan, and K. Yogendra, "Brain-inspired computing with spin torque devices," in *Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014*, Mar. 2014, pp. 1–6.
- [8] A. F. Vincent, J. Larroque, N. Locatelli, N. B. Romdhane, O. Bichler, C. Gamrat, W. S. Zhao, J. O. Klein, S. Galdin-Retailleau, and D. Querlioz, "Spin-transfer torque magnetic memory as a stochastic memristive synapse for neuromorphic systems," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 2, pp. 166–174, April 2015.
- [9] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Networks*, vol. 23, no. 7, pp. 881–886, Sep. 2010.
- [10] M. Prezioso, F. Merrih-Bayat, B. Hoskins, G. Adam, K. Likharev, and D. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," *Nature*, vol. 521, no. 7550, p. 61, 2015.
- [11] S. Saïghi, C. G. Mayr, T. Serrano-Gotarredona, H. Schmidt, G. Lecerf, J. Tomas, J. Grollier, S. Boyn, A. F. Vincent, D. Querlioz, S. La Barbera, F. Alibart, D. Vuillaume, O. Bichler, C. Gamrat, and B. Linares-Barranco, "Plasticity in memristive devices for spiking neural networks," *Frontiers in Neuroscience*, vol. 9, Mar. 2015.
- [12] M. Bichler, D. Suri, D. Querlioz, D. Vuillaume, B. De Salvo, and C. Gamrat, "Visual pattern extraction using energy-efficient "2-PCM synapse" neuromorphic architecture," *IEEE Transactions on Electron Devices*, vol. 59, pp. 2206–2214, 2012.
- [13] N. Axmacher, F. Mormann, G. Fernández, C. E. Elger, and J. Fell, "Memory formation by neuronal synchronization," *Brain Research Reviews*, vol. 52, no. 1, pp. 170–182, 2006.
- [14] D. Bhowmik and M. Shanahan, "How well do oscillator models capture the behaviour of biological neurons?" in *The 2012 International Joint Conference on Neural Networks (IJCNN)*, Jun. 2012, pp. 1–8.
- [15] J. J. Hopfield, "Neural networks and physical systems with emergent collective computational abilities," *Proceedings of the National Academy of Sciences*, vol. 79, no. 8, pp. 2554–2558, Apr. 1982.
- [16] A. Johannet, L. Personnaz, G. Dreyfus, J.-D. Gascuel, and M. Weinfeld, "Specification and implementation of a digital Hopfield-type associative memory with on-chip training," *IEEE Transactions on Neural Networks*, vol. 3, no. 4, pp. 529–539, 1992.
- [17] F. Hoppensteadt and E. Izhikevich, "Associative memory of weakly connected oscillators," in *International Conference on Neural Networks, 1997*, vol. 2, 1997, pp. 1135–1138 vol.2.
- [18] E. Izhikevich, "Weakly pulse-coupled oscillators, FM interactions, synchronization, and oscillatory associative memory," *IEEE Transactions on Neural Networks*, vol. 10, no. 3, pp. 508–526, 1999.
- [19] D. Nikonov, G. Csaba, W. Porod, T. Shibata, D. Voils, D. Hammerstrom, I. Young, and G. Bourianoff, "Coupled-Oscillator Associative Memory Array Operation for Pattern Recognition," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 1, pp. 85–93, 2015.
- [20] S. P. Levitan, Y. Fang, J. A. Carpenter, C. N. Gnegy, N. S. Janosik, S. Awosika-Olumo, D. M. Chiarulli, G. Csaba, and W. Porod, "Associative processing with coupled oscillators," in *Proceedings of the 2013 International Symposium on Low Power Electronics and Design*, ser. ISLPED '13. IEEE Press, pp. 235–235.
- [21] J. Cosp, J. Madrenas, E. Alarcon, E. Vidal, and G. Villar, "Synchronization of Nonlinear Electronic Oscillators for Neural Computation," *IEEE Transactions on Neural Networks*, vol. 15, no. 5, pp. 1315–1327, Sep. 2004.
- [22] M. A. Sivilotti, M. Emerling, and C. Mead, "A Novel Associative Memory Implemented Using Collective Computation," in *Artificial neural networks: electronic implementations*, N. Morgan, Ed. Piscataway, NJ: IEEE, 1990, pp. 11–21.
- [23] T. Shibata, R. Zhang, S. Levitan, D. Nikonov, and G. Bourianoff, "CMOS supporting circuitries for nano-oscillator-based associative memories," in *2012 13th International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA)*, 2012, pp. 1–5.
- [24] M. Cotter, Y. Fang, S. Levitan, D. Chiarulli, and V. Narayanan, "Computational Architectures Based on Coupled Oscillators," in *2014 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Jul. 2014, pp. 130–135.
- [25] F. C. Hoppensteadt and E. M. Izhikevich, "Synchronization of laser oscillators, associative memory, and optical neurocomputing," *Physical Review E*, vol. 62, no. 3, pp. 4010–4013, Sep. 2000.
- [26] G. Csaba, M. Pufall, D. Nikonov, G. Bourianoff, A. Horvath, T. Roska, and W. Porod, "Spin torque oscillator models for applications in associative memories," in *2012 13th International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA)*, 2012, pp. 1–2.
- [27] D. Fan, S. Maji, K. Yogendra, M. Sharad, and K. Roy, "Injection-locked spin hall-induced coupled-oscillators for energy efficient associative computing," *Nanotechnology, IEEE Transactions on*, vol. 14, no. 6, pp. 1083–1093, Nov 2015.
- [28] S. Datta, N. Shukla, M. Cotter, A. Parihar, and A. Raychowdhury, "Neuro inspired computing with coupled relaxation oscillators," in *2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC)*, Jun. 2014, pp. 1–6.
- [29] N. Shukla, A. Parihar, M. Cotter, M. Barth, X. Li, N. Chandramoorthy, H. Paik, D. Schlom, V. Narayanan, A. Raychowdhury, and S. Datta, "Pairwise coupled hybrid vanadium dioxide-MOSFET (HVFET) oscillators for non-boolean associative computing," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, 2014, pp. 28.7.1–28.7.4.
- [30] A. Parihar, N. Shukla, S. Datta, and A. Raychowdhury, "Exploiting synchronization properties of correlated electron devices in a non-boolean computing fabric for template matching," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no. 4, pp. 450–459, 2014.
- [31] A. Sharma, J. Bain, and J. Weldon, "Phase Coupling and Control of Oxide-based Oscillators for Neuromorphic Computing," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. PP, no. 99, pp. 1–1, 2015.
- [32] E. Vassilieva, G. Pinto, J. Acacio de Barros, and P. Suppes, "Learning Pattern Recognition Through Quasi-Synchronization of Phase Oscillators," *IEEE Transactions on Neural Networks*, vol. 22, no. 1, pp. 84–95, Jan. 2011.
- [33] G. Milshtejn, "Approximate integration of stochastic differential equations," *Theory of Probability & Its Applications*, vol. 19, no. 3, pp. 557–562.