An Accelerated Analog Neuromorphic Hardware System Emulating NMDA- and Calcium-Based Non-Linear Dendrites

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Abstract—This paper presents an extension of the BrainScaleS accelerated analog neuromorphic hardware model. The scalable neuromorphic architecture is extended by the support for multicompartment models and non-linear dendrites. These features are part of a 65 nm prototype Application Specific Integrated Circuit (ASIC). It allows to emulate different spike types observed in cortical pyramidal neurons: NMDA plateau potentials, calcium and sodium spikes. By replicating some of the structures of these cells, they can be configured to perform coincidence detection within a single neuron. Built-in plasticity mechanisms can modify not only the synaptic weights, but also the dendritic synaptic composition to efficiently train large multi-compartment neurons. Transistor-level simulations demonstrate the functionality of the analog implementation and illustrate analogies to biological measurements.

I. INTRODUCTION

The biological nervous system is a main source of inspiration in the quest for future computing. A prominent example is deep learning, a computing scheme based on multi-layer Perceptron models [1], which is currently in the focus of academia as well as industry [2]. The neuron models used in these machine learning applications are heavily simplified compared to the biological example. The fact that such a simple copy of the basic architecture of the nervous system is already capable of impressive results encourages many scientists that even more powerful computing devices might be built by looking more closely at nature's principles. The hope is that even without a full understanding of the operation of the brain, studying its architecture leads to new inspirations for the development of novel computing systems [3].

Testing such concepts is mostly done with numerical simulations, often using standardized software packages [4], [5]. These tools allow a step up in complexity from the Perceptron model by using spike-based neuron models. Spike-based models cover a wide range of complexities, ranging from the basic Integrate-and-Fire models up to Hodgkin-Huxley-like models incorporating a multitude of different ion-channel kinetics [6].

It has been shown by several research groups that prominent concepts used with Perceptron models, for example sampling based approaches [7], [8] or deep-learning using backpropagation [9], can be transferred successfully to spiking models [10]. Comparing typical benchmark problems, many spike-based implementations reach similar scores as their ratebased examples [11], but they execute orders of magnitude slower on the commonly used High Performance Computing (HPC) platforms [12].

It gets even worse if the training methods are constrained to biologically plausible mechanisms, which requires that at short timescales all information exchange is done by spikes only. This forbids for example the implementation of back-propagation as it is currently used in the standard deep-learning software packages [13]. Luckily, first ideas how to circumvent these problems have been reported lately [14], where the network learns not only its objective but also the correct mapping of the error information from the output backwards to the upstream synapses.

Recent findings in biology [15] have inspired novel models [3], [16] which include the three-dimensional structure of the neuron. The dendritic tree is no longer treated as a compartmentalized cable-equation [17], but as a complex non-linear structure which allows multi-layer information processing and coincidence detection within a single neuron [18].

Including all these details into numeric simulations strongly enhances the performance problems already surfacing with spiking neuron models. The work in this paper presents an alternative approach to the numerical modeling of multicompartmental, non-linear dendrites, using physical-modelbased neuromorphic hardware [19]. It builds upon the Brain-ScaleS accelerated analog neuromorphic system [20] in conjunction with the built-in hybrid plasticity extension developed for the BrainScaleS 2 system [21]. It expands these concepts by incorporating novel circuits to mimic non-linear dendritic behavior, including an emulation of N-Methyl-D-Aspartat (NMDA) and calcium channels [22].

In [23] a neuromorphic chip is presented that also contains NMDA emulation circuitry and has adapted many of the features of the BrainScaleS system, but implementing them in the real-time domain using sub-threshold point neurons, in contrast to the accelerated emulation used in the circuits presented in this publication. Some authors have reported neuromorphic circuits incorporating aspects of NMDA-R behavior to achieve a certain functionality, for example [24] and [25]. In contrast to those, our approach is not targeted at a single functional model, but aims to be a universal experimental platform. The presented implementation is also



Fig. 1. Basic structure of the HICANN chip. Left: Micro-photograph of a first generation HICANN chip. The synapses are organized in two blocks with the neurons in the center. Each block has 128 independent pre-synaptic input circuits, each capable of relaying 64 different pre-synaptic neurons, adding up to a total of 16k different pre-synaptic neurons. A single input is symbolically depicted by the red arrow. Right: conceptual drawing of the neuron compartment circuits and their associated synapses. The individual compartments are connected to each other by switches to assemble the neurons (A) and between adjacent compartments in the upper and lower block (B).

inherently scalable in the framework of the BrainScaleS system. Neuromorphic hardware concepts based on non-linear dendrites have also been previously reported [26] [27], demonstrating the viability of the concept for pattern classification.

This paper will present an extension of the BrainScaleS Adaptive-Exponential Integrate-and-Fire (AdEx) neuron model [28] that allows the replication of coincidence detection between basal and apical dendritic segments similar to those observed in experiments [29]. The circuits are fully plastic and can be tuned during the experiment according to plasticity rules executed by the local plasticity processing unit [30], while still performing the network emulation at an acceleration factor of 10^3 . A first prototype chip has been sent to manufacturing at the time of this writing.

The remaining sections of the paper are organized as follows: Section II gives an introduction to the BrainScaleS 2 accelerated analog neural network hardware implementation, Section III describes the theory as well as the circuit implementation of the multi-compartment extensions. Section IV shows simulation results demonstrating the presented circuits' capabilities. Section V discusses the built-in plasticity and possible learning algorithms. The paper closes with Section VI, presenting our conclusions and outlook.

II. ACCELERATED ANALOG NEUROMORPHIC HARDWARE

The presented multi-compartment circuits are part of a larger research project which aims to develop the second generation BrainScaleS neuromorphic hardware as part of the European Human Brain Project (HBP) [31]. The basic neuromorphic building block of every BrainScaleS system is the High Input Count Analog Neural Network (HICANN) chip. It contains the neuron and synapse circuits as well as a digital communication



Fig. 2. Conceptual drawing of the synaptic input with its associated column of synapses (rotated by 90 degrees to fit the layout of the figure), the enlargement shows a block diagram of the synapse circuit. The part of the synapse implementing the pre-post connection is shaded in green.

network. While the first generation is implemented in 180 nm standard Complementary Metal-Oxide-Semiconductor (CMOS) technology, the second generation uses a smaller 65 nm feature size, which enables, among others, the inclusion of a Plasticity Processing Unit (PPU) to implement hybrid plasticity [21].

Fig. 1 shows the basic structure of the BrainScaleS neuromorphic ASIC. The micro-photograph is the current version of the BrainScaleS chip and serves only as an illustration, since the basic structure of the second generation BrainScaleS ASIC, which is the version referred to in this paper, will be very similar. The synapses are arranged in a two-dimensional array. All synapses in a column share their output, while two adjacent rows share the same group of pre-synaptic input signals. There are 512 rows all-together, each group of two is connected to 64 pre-synaptic neurons by the means of the digital communication network. The inputs to the upper and lower block are independent from each other. Each block can receive events from a maximum of 8192 different pre-synaptic neurons.

To be able to create neurons of different sizes, each column of synapses together with the neuron compartment circuits in the center of the chip has an adjustable membrane capacitance which can be connected to the neighboring compartment circuit by an electronic switch¹. A second set of switches allows to connect adjacent neuron compartments in the upper and lower block, doubling the number of available pre-synaptic inputs to the neuron. The maximum number of pre-synaptic neurons that can project to a single neuron is 16k. The pre-synaptic neurons can be located on the same or on remote chips, either on the same or different silicon wafers [32].

Fig. 2 illustrates the synaptic input of the neuron with its associated synapses as well as the temporal relationship of the related signals. It shows that a column of synapses (rotated

¹All switches are built from standard CMOS transmission gates.



Fig. 3. One PPU instance each is located a the outer edge of the upper and lower synapse block.

in the figure to fit the page format) is connected to the two *dendritic input lines* of the neuron compartment, labeled A and B. The enlargement in the lower half of Fig. 2 depicts the different functional blocks within each synapse. At its core is a 6 bit memory storing the current weight of the synapse. A weight of zero means there is effectively no connection between the pre- and post-synaptic neurons, but the correlation between pre- and post-synaptic events is still being monitored².

The neuron compartment circuit emulates the different ion channels. The voltage on the membrane capacitance reflects the momentary membrane voltage of the compartment [33]. The conductances and capacitances are scaled such that all time constants are a factor of 1000 shorter compared to biology. Hence the addition *accelerated* in the designation of the BrainScaleS model.

A time-multiplexed scheme is used to allow the high number of inputs per row. The communication network delivers presynaptic events with a maximum rate of 125 MHz. Each row of synapses receives pre-synaptic events from up to 64 different pre-synaptic neurons through said network. The synapses receive the events via one shared input bus per row, transmitting a 6 bit pre-synaptic address to identify the pre-synaptic neuron. Each synapse stores a 6 bit pre-synaptic address that is compared to the address presented on the input bus each time a pre-synaptic event is transmitted. In case of an address match, the synapse uses a pulse of a precise duration of 4 ns to sink current from the dendritic input of the neuron compartment circuit it is connected to. The amplitude of the current pulse is proportional to the weight stored in a separate 6 bit memory within the synapse [21]. Depending on a row-wise configuration setting, the synapses use one of two available dendritic inputs, named A and B in Fig. 2. This allows each neuron compartment to accommodate two different synaptic time constants and reversal potentials. The capacitance of the dendritic input line acts as an integrator of all synaptic current pulses. An adjustable resistor recharges the dendritic line capacitance continuously, thereby setting



Fig. 4. Different kinds of spikes in a cortical pyramidal neuron. Figure taken from [34].

the synaptic time constant. Due to the acceleration factor the synaptic time constant is typically about $2 \mu s$, approximately three orders of magnitude slower than the synaptic current pulses.

By storing not only their weight, but also part of their presynaptic neuron address, the content of the synapse memories defines the local network topology. To program these memories, a custom Single Instruction Multiple Data (SIMD) microprocessor (PPU) is connected to the synapse array at the opposite edge of the compartment circuits. Fig. 3 illustrates this arrangement. It is described in detail in [21].

III. MULTI-COMPARTMENT NEURONS

III-A. Conceptual Background

The accelerated analog neuron model presented in Section II can be used to emulate point-neuron-based network models with a biologically realistic fan-in of more than 10k pre-synaptic neurons. To use a physical model with such a high number of inputs one has to consider the linear character of the synaptic input in the point neuron model. Identical synapses generate the same post-synaptic potentials (PSPs), thus having the same potential contribution to the firing of the soma. A contribution which decreases with the total number of synapses, since in the BrainScaleS physical model increasing the size of the neuron automatically decreases the PSP of a single synapse. This is caused by the growth of the membrane capacitance due to the larger number of neural compartment circuits connected together.

²This will be covered in detail in Section V.

Therefore, the more synapses a neuron has, the more presynaptic action potentials must arrive in synchrony to reliably relay an input pattern. On the other hand it is desirable to use sparse coding in neural networks [35], [36]. The energy consumption in the BrainScaleS physical model is directly linked to the sparseness of the neural code used.

Arguments against the simple linear addition of all synaptic inputs can also be found in biology. It has been observed that many neo-cortical cells are subject to a dense background firing from thousands of synapses as well as that microscopic sources of true noise are present at each synapse [37].

Recent findings have shed some light on different non-linear mechanisms within the dendritic tree of the neuron [38], most notably the capability of the dendritic membrane to generate different spike types in distinct parts of the dendritic tree of a neuron. These properties provide a possible solution to the problem outlined above. A hypothesis reviewed in [34]: "Clustering of synaptic inputs in space (and time) improves the chances for reaching the dendritic threshold for firing a regenerative (amplified) response and provides the opportunity for faster and more frequent cooperation among synaptic contacts involved in the same computational task." Therein the authors furthermore elaborate: "Instead of thousands of synaptic inputs, the pyramidal cell requires only a *correct* set of < 50active synaptic contacts to trigger a regenerative dendritic response (e.g. NMDA/plateau potential)". Fig. 4, taken from [34], summarizes the three kinds of spikes one can observe within a cortical pyramidal neuron.

NMDA-receptors are typically located in the thin, distal parts of the tuft, oblique and basal dendrites. They are responsible for NMDA spikes (*B*1). Since they are usually co-located with sodium channels, the resulting waveforms resemble the NMDA plateau potential (PP) shown in Fig. 4A. Triggered by a sufficiently localized synaptic input of approximately 10 to 50 pre-synaptic action potentials [39], it strongly increases the membrane conductance for a period ranging from several tens to hundreds of milliseconds. Due to the fact that NMDA channels are glutamate receptors with voltage dependent magnesium blocks, the NMDA PP is a strongly non-linear function of the pre-synaptic input. If the dendritic membrane stays below its threshold, only a sub-threshold PSP is observed.

The presented in-silico emulation has been guided by these observations. Because the design of our physical modeling system already incorporates the interconnection of compartments to implement a scalable number of synapses per neuron it was a natural step to include an extension that incorporates dendritic structures with active components. In the subsequent sections we focus on pyramidal neurons becuase of their supposed role in cortical information processing, as discussed for example in [29].

III-B. Implementation

The implementation of the multi-compartment concepts introduced in Section III-A into the BrainScaleS 2 neuron requires two additional features for the existing neuron circuit [40]: an emulation of the effect of the NMDA and calcium



Fig. 5. Left: Operation principle of the compartmental ion channel circuit (exemplarily configured as NMDA circuit). Right: Transistor-level simulation of an NMDA PP.

ion channels as well as controllable inter-compartmental conductances. The previous neuron implementations of our research group, beginning with the Spikey neuron [19], and including our previous multi-compartment chip [41], are only capable of emulating a sodium-like spike. This is done by continuously comparing the membrane voltage against an adjustable threshold voltage. If the threshold voltage is crossed, a spike is generated and the membrane is connected to the reset potential by a very high conductance. This condition is held for an adjustable amount of time to generate the refractory period of the neuron. After the refractory time has passed, the connection to the reset is released and the membrane is controlled by the interplay of synaptic input and leakage potentials again.

Fig. 5 illustrates the operational principle of the ion channel circuit. It is based on a unified emulation circuit for the three different neuronal spike types listed in Fig. 4. The ion channel circuit uses two adjustable settings for its reversal potential as well as its conductance. The active setting is controlled by a voltage comparator (Comp), which continuously compares the membrane voltage against an adjustable threshold. If the threshold voltage is crossed, the ion channel circuit switches to the alternate setting. The output signal of the comparator passes through a mono-flop (MF) which ensures that the ion channel circuit switches to its alternate setting for a defined period of time. In the presented implementation this time interval is controlled by a digital counter, allowing a wide dynamic range from sub-milliseconds to several hundreds of milliseconds in biological time. The ion-channel itself is built from an operational transconductance amplifier (OTA) circuit, emulating the channel conductance. Electronic switches connect one of the two electrical parameter sets to the OTA. The parameters are part of the analog parameter storage memory associated with the neuron compartment circuits [42]. This memory holds 24 analog parameters for each individual neuron compartment. In addition to parameter tuning, the values stored in the analog memory are also used to compensate process and fixed-pattern variations.

In Fig. 5 the circuit is configured for the emulation of NMDA channels: the threshold is set to the gating voltage of the NMDA receptor ($V_{\text{th_NMDA}}$), the ion channel emulation is switched from the leakage setting (g_{leak} and V_{leak}) to the setting for an NMDA PP (g_{NMDA} and V_{NMDA}). The right half of the figure shows a transistor-level simulation of this circuit,



Fig. 6. Multi-compartment extension to the BrainScaleS neuron circuits. The additional parts are shaded.

demonstrating the effect of the voltage-gated NMDA channel on the membrane voltage: as soon as multiple PSPs pile up and reach the NMDA threshold, the conductance mode is switched and the NMDA conductance pulls the membrane quickly up to the NMDA reversal potential $V_{\rm NMDA}$ where it stays until $\tau_{\rm NMDA}$ has passed and the ion channel emulation switches back to the leakage parameters, pulling the membrane back to the compartment's leakage potential $V_{\rm leak}$.

By changing the values of the threshold as well as the two parameter sets for the ion channel and the time constant of the mono-flop other kinds of spikes can be emulated as well. For example, in the sodium case the threshold equates to the firing threshold and the time constant to the refractory time. Instead of using the NMDA parameters the ion channel circuit is set to maximum conductance and the reversal potential to the reset voltage. This will be shown in more detail in Section IV.

In the current revision of the BrainScaleS 2 chip, each neuron compartment circuit contains one instance of the functional unit described above. Therefore each compartment can now be configured to generate either NMDA, calcium or sodium spikes. All three spikes also generate digital signals that can be routed as events to other parts of the system, which are typically but not exclusively the pre-synaptic inputs of unrelated neurons. Thus, they also take part in the coincidence detection mechanisms used for plasticity (see Section V). Since all parameters are freely adjustable within the available ranges, settings which do not resemble biological examples can be realized as well. If no voltage-gated ion channels are required, the circuit can be disabled.

The presented models are still simplistic and do not take into account some of the known features of their biological examples. For example, the glutamate concentration at the distal dendrite modulates the length of the NMDA PP [15]. Also, the channel emulation is only voltage gated while the real NMDA-R molecule is a glutamate receptor with a voltage dependent magnesium block.

The second extension is an additional interconnect to create larger neurons from a set of neuron compartments. The



Fig. 7. A: Illustration of the equivalent pyramidal neuron model in accordance to [18]. The different compartments are discerned by their spike mechanism: NMDA, calicum (Ca) or sodium spikes (Na). B: Example configuration to implement the multi-compartment structure shown in A. The configuration of each compartment is depicted by its coloring as well as by the name of the spike type they produce (NMDA: red, Ca: blue, Na: black).

shaded part in Fig. 6 shows the necessary components: an adjustable conductance per neuron compartment and some switches. The new shared line represents the somatic membrane. Each neuron compartment can be connected to it via an adjustable conductance which represents the conductance between the distal dendrite and the soma. Usually, not all neuron compartments within a neuron block (see Fig. 1) are supposed to be part of the same neuron. Therefore, there are switches built into the somatic line at regular distances (every four compartments in Fig. 6) which allow its separation into different neurons. The somatic membrane by itself does not contain any active circuits, neither does it have an associated membrane capacitance. It acquires this functionality by a connection to a neuron compartment which is configured to have an infinite conductance between its compartmental membrane and the somatic membrane. To achieve the effect of this infinite conductance, or zero resistance, a bypass switch exists in parallel to each adjustable conductance.

Including said extensions into the basic neuron block structure illustrated in Fig. 1, the neuron can now be configured to emulate non-linear, multi-compartment neurons. By including calcium spikes it is possible to emulate more complex neurons, like for example layer 5 pyramidal neurons [18]. Fig. 7A illustrates this concept: the basic structure of a pyramidal neuron is replicated using the presented circuits. The individual compartments are connected by the adjustable intercompartment conductances introduced in Fig. 6, depicted by resistor symbols. The neuron model consists of a set of distal tuft and basal dendrites containing NMDA receptors, giving them the ability to create NMDA PPs if the NMDA threshold is reached. All basal distal dendrites are connected to the soma, which is configured to generate sodium spikes to emulate the axon hillhock. The distal tuft dendrites converge at a separate junction, emulating the apical dendrite. The apical dendrite connects to the soma via a compartment configured for calcium spike generation. This allows the electronic neuron model to detect coincidences between its basal and distal input, similar to the measurements of laver 5 pyramidal neurons reported in [29]. Section IV provides simulation results illustrating this mechanism.

Fig. 7B depicts the same configuration of the neuron compartment circuits, but shown as they are arranged in the physical layout of the chip (see Fig. 1). Both neuron blocks, the upper and the lower, are used. The somatic line in the upper block emulates the apical dendrite, the one in the lower block the soma. The lower left compartment is configured to generate sodium spikes. Therefore, the bypass switch for the resistor connecting it to the somatic line is closed. Its membrane capacitance becomes the somatic capacitance of the neuron. If the voltage on this capacitance crosses the sodium threshold programmed into the compartment, the neuron will fire a spike and the soma capacitance will be pulled down to the reset potential. The NMDA compartments (marked red in Fig. 7B) in the lower block the distal tuft dendrites, the ones in the upper block the distal tuft dendrites.

Two compartments, one in the upper and one in the lower block, are used to connect the apical dendrite with the soma (shown in blue). This is accomplished by closing the vertical switch between them. This directly connects both their membrane capacitances and both calcium spike mechanisms share the same membrane voltage, which is isolated from the soma as well as the apical dendrite by an adjustable conductance each. The calcium spike generation can use either one or both of the spike mechanisms in the two compartments, which provides additional possibilities for better approximating the correct calcium waveform by combining multiple time constants and conductances. The possible neuron models are not limited to the pyramidal neuron example. For instance, it is also possible to create a branch in the apical dendrite, or to have several distinct dendrites.

IV. RESULTS

This section provides results from circuit simulations of the neuron and its multi-compartment extensions. The simulation setup includes four neuron compartments with the corresponding multi-compartment circuits and eight synapses for each compartment. Only the part of the system that is essential to the new multi-compartment functionality is simulated at transistor level to reduce computation time. The simulated circuits match those of the prototype ASIC. The Spectre simulator³ is used with device characterization data provided by $TSMC^4$ for the simulations.

A behavioral model is implemented for the mono-flop which triggers the start of the refractory period and the alternate conductance mode (Fig. 5) when it receives a signal from the spike comparator. In the chip, the digital configuration is stored in local Static Random Access Memory (SRAM) while the analog parameter memory provides currents and voltages to the respective circuits. In simulation, the SRAM is implemented at transistor level and each cell is initialized to the required value for the corresponding neuron setup. The analog parameter memory is simulated as a behavioral model which consists of the output stage for current and an effective ideal capacitance and resistor for voltage parameters [42].

The chip design provides the possibility to stimulate one neuron by external current in addition to spiking input that reaches the compartments via the synapse circuits. In the simulation, current and voltage signals are provided to implement these inputs to the neurons and synapses as the ideal version of the input that is seen by the circuits during operation. In particular, the pre-synaptic enable signal and neuron address (Fig. 2) are provided to each synapse to initiate synaptic events while the current stimulus is injected into a shared input line. One neuron at a time is configured to receive input from this line.

Voltage readout for an arbitrary compartment is possible via a dedicated read-out path in the chip design. This path is not included in the simulation to reduce simulation time and the signals that are shown are recorded directly from the corresponding capacitors in the circuit.

Fig. 8A shows the basic functionality of a multi-compartment configuration. One compartment receives two inputs of different strength. The exponential term of the AdEx implementation is enabled for the compartment which receives the input. This term generates a current onto the membrane that increases as an exponential function of the membrane potential itself. It acts as a soft threshold [28] in addition to the explicit firing threshold in each compartment (Fig. 5). The second input is sufficiently strong to cause the membrane voltage of the stimulated compartment to exceed the threshold of the exponential term in that compartment and induce a spike and reset. The reset is configured to have a short refractory period and a low reset voltage, which corresponds to typical point-neuron models with Na spikes, e.g. the AdEx model [43]. The neighboring compartment is passively pulled up via the inter-compartment conductance. The upswing of the membrane voltage during an action potential is not captured in the implemented circuit as is usual for low-dimensional spiking neuron models (cf. [44]), which is particularly beneficial for a hardware implementation as it allows for a better utilization of the available voltage range for the neural sub-threshold dynamics.

³Cadence Design Systems, Inc., San Jose, CA, USA

⁴Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan



Fig. 8. Simulation of multi-compartment functionality: A: A single compartment (solid line) is stimulated by synaptic input and a current pulse. The current pulse is sufficient to trigger the exponential current in the compartment. Consequently, the firing threshold is reached and the compartment is pulled to the reset voltage which is configured to be below 0.6 V. The neighboring compartment is connected using an adjustable conductance (Fig. 6) and its membrane voltage (dashed line) passively follows the active compartment. B: Demonstration of the configurability of the reset circuit (Fig. 5). The reset duration and voltage can be modified to implement an up-state of precise length (solid lines). The neighboring compartments are pulled up via the passive conductance (dashed lines). Three distinct simulations for refractory periods of 70 µs, 9 µs and 30 µs are shown. C: Detection of coincidence over long timescales. Top: Synaptic input into the soma compartment (solid line) only induces spikes when the neighboring compartment (dashed line) has entered a high state. Center: input spikes to dendritic compartment (red, top) and soma (blue, bottom). Bottom: spike emission for dendritic (top) and soma (bottom) compartments. Bottom right: configuration of compartment interconnection for this simulation. Biologically inspired use case: D: Figure taken from [29]. The response of a layer 5 pyramidal neuron to separate and correlated dendritic and somatic stimulus is shown. The traces show the membrane voltage at the Na-spike initiation zone (blue), the Ca-spike initiation zone (black) and the dendrites (red). E-G: Simulation of circuit configuration that is inspired by the reference in D. Only the stimuli differ in the simulations in E-G; the circuit configuration is identical. The amplitude of the current stimulus is 1.5 µA. E: Spike input into the NMDA compartment (green, bottom) is chosen as not to cause firing in any compartment. An attenuated version of the post-synaptic potential is seen in the Ca and Na compartments. F: Current stimulus into the Na compartment which is adjusted to initiate a single spike. The pictogram shows the switch and resistor configuration to which the simulations in E-G will correspond in the final chip. G: Both inputs combined suffice to cause firing in the Ca and NMDA compartments. This, in turn, induces a burst in the Na compartment. Note that the time scale is milliseconds for the biological reference (D) and microseconds for the circuit simulation (E-G) due to the accelerated nature of the neuromorphic device (Section II). The circuit and stimulus parameters in all simulations were chosen such as to reproduce the desired spiking behavior. There is no procedural parameter mapping from a given reference for circuit or stimulus parameters. The relative timing of the stimulus in E-G is chosen such that the current input into the soma compartment arrives first, as in D. The time scales are not translated quantitatively.

The refractory time, reset voltage and threshold can be configured individually for each compartment (Fig. 8B), which is central to the implementation of active dendrites (Section III). Here, the reset potential is set above the threshold and the reset duration is set to three values between $9 \,\mu s$ and $70 \,\mu s$. Since the reset conductance is configured to be greater than the leak conductance, this setting effectively serves as an additional positive input current to the neighboring compartment, which is being pulled up passively.

A demonstration of directed coincidence detection is shown in Fig. 8C. Two compartments, one with a Na-like (short reset) and one with an NMDA-like (plateau potential) configuration, are connected by a conductance and each compartment is stimulated by distinct synaptic input. The circuit parameters are adjusted in such a way that the Na compartment emits spikes for single synaptic inputs during the high state of the NMDA compartment, but does not when the NMDA compartment is in its inactive state.

The features described above (Fig. 8A-C) are used to implement a functional behavior which is similar to that of layer 5 pyramidal neurons (Fig. 8D) described in [29]. Therein its author hypothesizes that pyramidal neurons in the cortex act as coincidence detectors for their basal and apical inputs. This proposed mechanism employs the active nature of Ca and NMDA spikes (Fig. 4) to allow a non-linear interaction of synaptic input to opposite poles of the neuron. Fig. 8D shows how a dendritic stimulus leads to a marginal effect at the soma, while a somatic stimulus leads to a single action potential. Both inputs combined trigger a burst. This functionality is emulated using the active components in the presented circuits (Fig. 8E). Synaptic input to the NMDA compartment induces a PSP which propagates to the other compartments and is attenuated along the way. Current stimulus into the Na compartment (Fig. 8F) is set to cause a single spike. When both inputs are applied

simultaneously the voltage in both dendritic compartments crosses the respective threshold, pulling up the membrane voltage in the Na compartment and causing a burst (Fig. 8G).

This demonstrates how the presented physical implementation is configured in analogy to a biological use case, emulating the dendritic structure by a series of connected compartments and using the introduced extensions of the BrainScaleS neuron model (Section III) to emulate the active nature of the Ca and NMDA spikes in the biological reference. The simulation shows that using this structural analogy one can parameterize the circuit to achieve a functional analogy, in this case the implementation of a non-linear coincidence detection for inputs into different locations of a single neuron.

V. PLASTICITY

In Section III the basic concept of the BrainScaleS accelerated analog neuromorphic network chips has been presented, omitting one important aspect: plasticity. Similar to other neuromorphic devices, e.g. [45], [46], correlation measurement between pre- and post-synaptic events is used to implement learning. In Fig. 2 and Fig. 3 two key structures implementing plasticity⁵ are shown: the correlation sensor within each synapse and the PPU at the edge of each synapse array. The correlation sensor measures the exponentially weighted temporal difference of each pre-post and post-pre spike pair⁶ and stores it locally in each synapse. The PPU can read back these causal and anti-causal correlation data as well as the current weights and addresses of the synapses. It executes a software-defined algorithm to determine new weights and possibly new addresses. It can also update all parameters of a configured neuron circuit like Fig. 7, e.g. modify NMDA plateau durations, calcium threshold voltages or reset conductances. A detailed description of how these circuits interact to implement a flexible hybrid plasticity concept can be found in [21].

Measuring correlation between pre- and post-synaptic events is frequently used to implement local learning in neuromorphic hardware [45] [46] based on the strengthening of causal connections, i.e. synapses that were active in the time frame before the firing of the post-synaptic event. In large neurons with linear dendrites, this becomes increasingly difficult because of the diminishing effect a single synapses has on the firing of the post-synaptic event. The non-linear model using NMDA PPs may provide better signatures for plasticity. Only about 10 to 50 synapses located on a common distal dendrite are needed to evoke a plateau potential [39]. Therefore, replacing the NMDA event as the post-synaptic event for plasticity provides a clear learning signal even with thousands of synapses connected to the neuron. The presented hardware model allows to use all spike types as post-synaptic signals for plasticity, including NMDA for the synaptic columns configures as distal dendrites.

Grouping synapses onto distal dendrites with non-linear, active mechanisms solves the problem of the single synaptic



Fig. 9. Illustration of structural plasticity. Part of the pre-synaptic address memories in the synapses are changed by the PPU (left: yellow numbers). Synapses recording a high correlation are kept (right: bold numbers). Synapses with insufficient correlation are changed to a different pre-synaptic neuron (right: yellow numbers). In the lower left an established synaptic connection has been replaced (right: italic yellow) by a random new one.

event drowning in the overall synaptic input of the cell, but creates a new one: which synapses should be grouped on a dendrite? The presented neuromorphic hardware realizes an efficient platform for testing algorithms using the combination of local correlation measurement and the possibility to quickly change the pre-synaptic input of a dendrite. This implements a hardware analogy to the kind of structural plasticity created by the growth of axons and dendrites and the formation of axonal boutons and dendritic spines [48] [49].

Fig. 9 visualizes the basic concept. It presents an example where each row of synapses gets input from a group of neurons with similar, related information, e.g. part of an upstream layer or a subset of neighboring neurons within the layer. The PPU assigns random addresses to the synapses of such a row (rows two and three in the example). While the network emulation is continuously operating the synapses in each column measure the correlation between the NMDA PPs and their input. The PPU monitors these correlation measurements and tags synapses with high correlation results to be established as working synapses, i.e. assigns them a non-zero weight (bold numbers) while it reassigns new random pre-synaptic input to the synapses showing weak correlation numbers. In addition, it can also reassign previously established synapses if their weight has fallen below a threshold, i.e. if their correlation has weakened over time.

Although a similar net result could be achieved by starting with a fully connected network and pruning unused connections by Spike-timing dependent plasticity (STDP), a much larger number of synapses would be needed initially and a subsequent re-mapping of the remaining non-zero synapses onto the hardware would be necessary to realize any benefit form the pruning.

It is possible to route the post-synaptic firing signal of one compartment, for example the soma, to synapses of different compartments. This allows to implement the functional analogy of back-propagating action potentials from the soma to the dendrites. In a supervised learning scenario this may be used to relate different kinds of teacher signals that modulate

⁵We are restricting this chapter to the multi-compartment related aspects of long-term plasticity. The BrainScaleS chips also implement short-term synaptic plasticity [47].

⁶The correlation sensor implements a nearest-neighbors scheme.

somatic firing with the synaptic composition of the neuron. Similar models to implement biologically plausible backpropagation learning schemes have been proposed [16]. Due to the acceleration factor of 1000 the chip can test a multitude of possible synaptic configurations per dendrite while still being faster than biological real time.

VI. OUTLOOK

This paper presents extensions to the BrainScaleS 2 neuron model for non-linear dendrites and structured neurons using multiple compartments. The purpose of these extensions is not the emulation of the full three-dimensional structure of the neuron [50] but its reduction to a minimal electronic model which captures the essential features of such a multi-compartment structure with active, non-linear dendrites. We think that the non-linearity created by the different kinds of spikes in combination with a flexible multi-compartment structure will significantly extend the capability of the BrainScaleS 2 system to help investigate the intersection between biologically inspired hypotheses of information processing [29], machine-learning derived approaches [16] and the efficient implementation of these kinds of processing in dedicated hardware systems.

The ability of a single neuron to act as a coincidence detector and the availability of somatic spike information at distal dendrites is expected to facilitate the mapping of established machine learning approaches to large-scale spiking systems. Future computing based on neuromorphic hardware might also benefit from the presented level of biological realism, since it could help in creating efficient local learning strategies derived from the biological example. Most likely, if these strategies are identified and proven, the neuromophic systems could be simplified again. Not all of the biological features implemented in the presented model will be needed for each application.

The fully parallel and accelerated nature of the system supports a fast investigation of spiking systems with highly different time scales of neural and plasticity dynamics. Due to its analog implementation it will keep the advantages of neuromorphic hardware like low power-consumption and robustness against localized defects. Since it is spike based and continuous time it might be useful for studying spatio-temporal problems.

The multi-compartment extensions will not change the powerconsumption of the HICANN chip significantly. The energy needed per synaptic transmission depends strongly on network topology and activity and is of the order of magnitude of 10 pJ. The area used by the extensions is less than $200 \,\mu\text{m}^2$ per neuron compartment. This is approximately 0.5% of the total area used by neuron and synapse circuits.

The introduced extensions of the BrainScaleS neuron model capture essential features of complex biological structures. Although we do not yet fully understand the purpose and the function of the biological details we are optimistic that the presented models will allow insight into the functional possibilities of multi-layered networks built from multi-compartment neurons possessing non-linear active dendrites. By evaluating the behavior of such networks using a multitude of possible plasticity schemes, we expect to gain insight into which features are relevant for functional performance. Future hardware generations might utilize these insights for systems that incorporate novel nano-electronic components.

The presented circuits have all been implemented in silicon using a 65 nm low-power CMOS technology and are currently being manufactured. As soon as funding allows they will be integrated in the wafer-based BrainScaleS 2 system which will then combine the speed of accelerated neuromorphic hardware with the substantial network size achievable by wafer-scale integration. The presented circuits and concepts should also be transferable to smaller process geometries.

In the meantime, a single chip implementation will soon be available to all interested researchers as an experimental platform for ideas inspired by biology and machine learning and to prepare the ground for future, non-Turing computing substrates.

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VIII. AUTHOR CONTRIBUTION

J.S. created the concept, designed the circuits and wrote and edited the manuscript except for Section IV, L.K. conceived the simulations jointly with P.M, performed the simulations and prepared the results, P.M. wrote Section IV and edited the manuscript and K.M. gave conceptual advice.

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