Multi-GPU SNN Simulation with Static Load Balancing

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Abstract—We present a SNN simulator which scales to millions of neurons, billions of synapses, and 8 GPUs. This is made possible by 1) a novel, cache-aware spike transmission algorithm 2) a model parallel multi-GPU distribution scheme and 3) a static, yet very effective load balancing strategy. The simulator further features an easy to use API and the ability to create custom models. We compare the proposed simulator against two state of the art ones on a series of benchmarks using three well-established models. We find that our simulator is faster, consumes less memory, and scales linearly with the number of GPUs.

Index Terms—SNN, AI, Deep Learning, simulation, multi-GPU, parallel, distributed, HPC, GPGPU, CUDA

I. Introduction

Spiking Neural Networks (SNNs), first formalized in 1997 [1], have experienced a renaissance in recent years due to the rise in popularity of Deep Learning and the widespread availability of GPGPU hardware. While we are still waiting for the breakthrough that will let SNNs overtake 2nd generation ANNs, the research community remains highly active, working to improve performance, biological fidelity, support for complex models and topologies, and user friendliness. Our own prior work [2] surpassed the state of the art on a couple of these criteria.

We believe that SNN simulation is fundamental to SNN design: faster simulation means faster iteration and thus quicker progress for the field as a whole. Not only speed is important, but so is size, especially considering that we are currently limited to simulating a modest 1% of a rat's visual cortex [3]. While gains are still to be made from algorithmic and data-structural improvements, we must solve multi-GPU (and eventually multi-node) scaling. Towards this goal we present a SNN simulator called "Spice" (/spark/) which scales to millions of neurons, billions of synapses, and 8 GPUs. This is made possible by three key contributions:

- A novel, cache-aware spike transmission algorithm allows linear scaling with network size in the face of millions of neurons that do not fit into cache.
- Our parallelization scheme distributes both computations and storage across multiple GPUs.
- A simple neuron partitioning strategy achieves perfect load balancing in practice albeit being completely static.

The result is a SNN simulator that makes it possible to run ten different experiments of 100K iterations on a 24B-synapse

¹We use "GPU" to refer to an entire GPU PCIe board throughout the paper.

model spanning 8 GPUs in the same time it takes competing simulators to create a single network.

II. RELATED WORK

As noted by Tuckwell [4], early attempts to mathematically model the function of biological neurons can be traced all the way back to the beginning of the 20th century [5]. Research on efficiently simulating SNNs has a long history [6], [7] and is still showing ever-increasing interest [2], [8]–[12]. It covers areas such as improving the biological fidelity [13] and numerical stability of methods [12] and employing hardware acceleration [14], [15] on such diverse platforms as VLSI [6], FPGA [15], and even super-computers [16]. Additionally, there have been theoretical advances such as the quantification of the difference between two spike trains [17], the exact solution of differential equations that model membrane dynamics [18], and an approach on implementing back propagation on SNNs [19].

A. Simulator classifications

Several useful classifications of SNN simulators can be defined based on their key traits. One classification regards whether the simulator aims to model the exact behavior of biological neurons [13], [20]–[25], or is just based on the general principle of spiking neurons.

Another classification regards the customizability of the simulators. Simulators that allow the user to specify neuron (and synapse) models with custom behavior can be referred to as general [2], [3], [26]–[30], in contrast to ones that only simulate fixed types of neurons [13], [21], [25], [31].

The distinction between event- and time-driven simulation arises in the software architecture of the simulator: Time-driven simulators [2], [3], [18], [31]–[33] quantize time into fixed deltas and advance the entire network state in lock-step. In contrast, event-driven simulators [7], [18], [27], [32], [34], [35] intentionally leave neurons in varying, past states until it is required by the simulation to advance them, usually because of incoming spikes. Typically, time-driven simulators are simpler and more efficient per element but very small deltas can become prohibitively slow. Event-driven simulators offer arbitrary time resolution and can potentially make up for their lower per-element performance by being able to skip ahead in time. Falling somewhere in between are so-called hybrid approaches [36], [37].

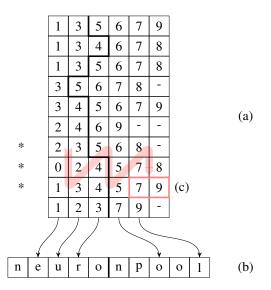


Fig. 1. We store our network's topology in a padded adjacency list (a). Each row stores a neuron's neighbor IDs (b). The synapse pool (not depicted) has the same size as the adjacency list with an implicit 1:1 mapping between the two. CUDA warps (c, here chosen to be 2 threads wide) deliver spikes (*) in a column-wise fashion, keeping recipients close together and improving cache coherency. The thick black line illustrates how the network would be split in two with a pivot of "4".

Lastly, simulators can also be classified according to the employed hardware platform. Common targets include regular CPUs [10], [27], [32], [34], [35], [38], [39], GPUs [2], [3], [8], [9], [11], [14], [15], [22], [25], [28]–[31], [36], [37], [40]–[42] (with some works notably combining CPU and GPU computations [14], [36], [37], [42]), as well as custom/specialized hardware [6], [15], [16], [20], [21], [43]. There is a clear trend in recent works to increasingly adopt specialized hardware, especially GPUs.

The simulator presented here is of the general-purpose, time-driven, GPU-accelerated variety.

B. Parallel Simulators

Works that aim to harvest the computational resources of multiple GPUs have been presented as early as 2010 [42]. The simulator in [42] is notable for its spike synchronization algorithm, pioneering the use of multiple GPUs as well as utilizing the available CPU. Beyond that it is of no use as its network topology and models were hard-coded. Also noteworthy is the work by Kunkel et al. [16] which inspired our parallelization scheme and load balancing strategy. In [16] the authors took the famous NEST simulator [38] and scaled it to a supercomputer comprising some 100 000 cores with decent results. Nowadays though it is outperformed by a single GPU by a factor of $100 \times$ (compare Fig. 5 "Brunel+" with Kunkel et al. [16, Fig. 9]).

As immediate competitors we choose two very recent works, closely related to ours: BSim [11] and NeuronGPU [44]. Both simulators are time-driven, GPU-accelerated, and general (to varying degrees), allowing the implementation of the same models in all three simulators,

and therefore a direct comparison. A comparison with event-driven simulators does not make much sense since each design pursues distinct goals entailing different trade-offs. BSim is the only other current, published state of the art simulator with multi-GPU support, so a comparison with it is mandatory. NeuronGPU stands out in that it is more focused on accuracy over performance, featuring double precision arithmetic and Runge-Kutta integration. It is interesting to see which performance trade-offs this design choice implies in practice.

III. METHOD

For self-containment, we recap the basic data structures and algorithms employed by Spice [2] (Sections III-A & III-B). We then discuss in depth the proposed spike transmission algorithm and its parallelization (Sections III-C–III-F).

A. Data Structures and Algorithms

Neurons and synapses are stored as a struct of arrays (SoA) which is necessary to enable memory coalescing on GPUs and can dramatically improve achieved memory bandwidth compared to an array of structs (AoS) layout [45]. The user specifies their neuron and synapse formats by inheriting from neuron and synapse base classes, for example:

via template meta programming. All neurons are stored in a single, global SoA (Fig. 1b) which is as big as the largest neuron model times the total number of neurons. This wastes a few megabytes of memory in exchange for simpler addressing and code. The same holds true for synapses.

The network's topology is stored in a single, padded adjacency list (Fig. 1a). This wastes a few percent of memory in exchange for simpler and faster code as it requires no offset table and allows us to align rows to 128-byte boundaries which leads to a few percent faster memory accesses. Each row's entries are sorted to improve cache coherency. We allocate a synapse pool the size of the adjacency list with an implicit 1:1 mapping between the two (adj[i,j] corresponds to synapses[i,j]).

Neuron- and synapse dynamics are specified by implementing callbacks such as <code>onUpdate()</code> and <code>onReceiveSpike()</code> which are invoked by the framework on every simulation step. As a result of updating neurons, some of them may spike. Their IDs are inserted into one of delay many spike arrays so they may be delivered on the appropriate simulation step in the future.

B. Adjacency List Construction

The network's topology is specified through a descriptor of the form $\{\{range1, range2, p\}, ...\}$ which means: "connect all neurons in range1 with all neurons in range2 with probability p" (and so on). The out-degree of neurons in range1 follows a binomial distribution, which can be approximated by a normal

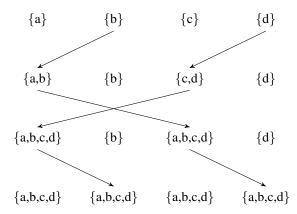


Fig. 2. Our spike synchronization algorithm. Depicted are 4 GPUs with their respective spike sets $\{a\}$, $\{b\}$, $\{c\}$, and $\{d\}$. The goal is for all GPUs to end up with the union of these sets. We hierarchically gather and then distribute the spikes again. Each arrow represents a cudaMemcpy() call. Whenever 2 GPUs end up with half of all the spikes (2nd row, 1st and 3rd GPU), we perform a full duplex sync (crossing arrows) which saves one iteration compared to a strictly hierarchical approach. So long as GPUs are equipped with two copy-engines, all memory transfers between two rows take place concurrently with respect to each other and the ongoing simulation.

distribution with mean $\mu = |range2| * p$ and variance $\sigma^2 = |range2| * p * (1-p)$. We compute the mean and variance for all neurons, summing them if a neuron is contained in multiple ranges. We then estimate the width of the adjacency list as

$$max\left(\mu_i + 3\sqrt{\sigma_i^2}\right),$$

which allows us to pre-allocate it. The layout description is then uploaded to the GPU where it is expanded and from it, the adjacency list is populated.

C. Spike Transmission

Spikes are transmitted by selecting the appropriate spike array S based on the current simulation step and delay. For each spike in S, the corresponding row in the adjacency list is selected (Fig. 1*) and the spike is delivered to all neighbors in said row by invoking the aforementioned onReceiveSpike() callback. This is done by launching $|S|*width(adj) \div 32$ CUDA warps where warp i is responsible for delivering spike $i \mod |S|$ to neighbors $|i \div |S|| * 32$ through $\lfloor i \div |S| \rfloor * 32 + 31$ of neuron $S_{i \mod |S|}$, i.e. columnwise (the neuron is advanced first, then its neighbors, Fig. 1c). Recall that the entries of each row are sorted. By traversing the adjacency list in a column-wise fashion the recipient neurons are statistically expected to be close together, improving our cache hit rate when writing to the global neuron pool. This allows us to scale linearly even when dealing with millions of neurons that do not fit into cache (see Section IV-B). We chose a warp because it is the smallest computational unit that still achieves full memory bandwidth.

D. Parallelization

Our design allows us to split the network across multiple GPUs with per-neuron granularity. Load balancing, the act of

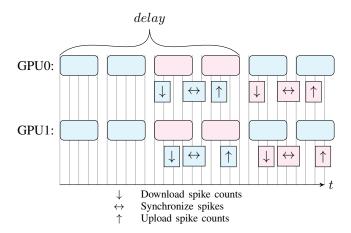


Fig. 3. Timeline of a dual-GPU simulation loop with delay = 4. The top row of each GPU's timeline depicts kernel invocations (simulation steps), the bottom row depicts memory transfers (spike synchronizations). We group the simulation into batches of delay many simulation steps. As soon as half the batch has completed on all GPUs, we download spike counts (required for address calculations), synchronize the spikes (according to Fig. 2), and upload the new, total spike counts. Simulation steps and spike transfers of the same color depend on each other's completion.

deciding which neurons should be assigned to which GPU, will be discussed later. For now let us assume we are given a partition and see how the neuron, synapse, and adjacency data are physically distributed. We remind ourselves that a network, in its entirety, is defined by the neuron pool, synapse pool, adjacency list, and user callbacks. In order to split such a network into, say, two slices given a pivot one would:

- 1) Split the neuron pool into ranges [start, pivot) and [pivot, end).
- 2) Split each row of the adjacency list along the pivot (via binary search).
- 3) Split the synapse pool in sync with the adjacency list. This is illustrated by the thick black line in Fig. 1. Callbacks need not be modified. They will simply be invoked on the new subsets of the original neuron and synapse pools. This split can be performed implicitly during network construction simply by modifying the topology descriptor:

$$\{range1, range2, p\}$$
 would turn into $\{range1, range2 \cap [start, pivot), p\}$ on GPU_0 and $\{range1, range2 \cap [pivot, end), p\}$ on GPU_1

Since the network never needs to be instantiated as a whole, the maximum network size grows linearly in the number of GPUs.

It is noted that each half of the original network forms a network in its very own right. It can be simulated on a dedicated GPU independently from the other half and without knowledge of any other GPUs in the system. Each GPU is responsible for delivering *all* spikes to *its* neurons via *its* synapses (similarly to [16]). Therefore, the only data that need to be exchanged between GPUs are spikes.

E. Spike Synchronization

Each GPU simulates its network slice in isolation and without knowledge of any other GPUs. A supervisor synchronizes spikes between GPUs using the hierarchical algorithm described in [46, pp. 9–18] (see Fig. 2). The synchronization is performed with a series of cudaMemcpy () calls so they may overlap with kernel executions, the importance of which will become apparent shortly. Rather than synchronizing spikes after every simulation step, we take advantage of the fact that delay many steps can be executed in a batch: any spikes produced inside one batch will not arrive until the next one (known as "Timestep Grouping" [31]). We divide batches into two halves with $\lfloor delay \div 2 \rfloor$ and $\lceil delay \div 2 \rceil$ many steps respectively. After the first half completes we asynchronously initiate spike synchronization which then runs concurrently with the second half (Fig. 3). This has two advantages:

- It is faster: By grouping spikes from multiple simulation steps together we cut down on the total number of memory transfers.
- 2) We maximize the probability that spike synchronization completes before the next batch begins (which is when the spikes will be needed).

If the simulation step and delay are long enough, we can hence completely hide any overhead introduced by spike synchronization. If, additionally, we can achieve perfect load balancing (all GPUs completing the batch simultaneously), the simulation will scale linearly with the number of GPUs.

F. Load Balancing

The goal of load balancing is to distribute the simulation load across GPUs as evenly as possible so as to avoid the system stalling for a long-running GPU. Ideally, all GPUs would complete every batch at the same time. In our case this means partitioning the neuron pool according to the above criteria. The partitioning of the adjacency list and synapse pool is determined by that of the neuron pool since a GPU must always store the incoming edges to all of its neurons.

PipeDream [47], which in large part solved multi-GPU backpropagation for conventional ANNs, opts for profiling: Before training, the cost of each layer is measured and layers are then optimally distributed across GPUs. This strategy has several disadvantages and does not map well to SNNs:

- The profiling time counts towards the total simulation time. A few seconds of profiling may be negligible in the face of hours of training, but they do add significant overhead in the case of short-lived SNN simulations.
- The thusly obtained neuron costs would only be valid for the profiling period itself. SNNs exhibit very complex dynamic behavior with greatly varying firing patterns over time. A partition which results in even load balancing at the beginning of a simulation, may become completely detrimental a few seconds into it.

We opt for a much simpler, completely static solution inspired by [16]: we split the network into hundreds of equal-width slices and assign them to GPUs in a round-robin

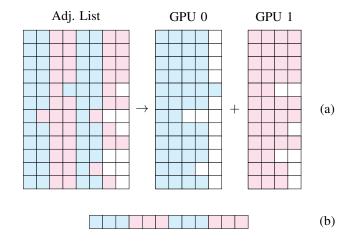


Fig. 4. Our load balancing strategy. (a) We split the network into many slices (here 4) and assign them to alternating GPUs, which averages out the variance and skew present in the neurons' simulation costs. (not shown) The synapse pool is split in sync with the adjacency list. (b) The neuron pool is replicated across GPUs as a whole which keeps global neuron IDs intact. Each GPU only processes its assigned neurons though (according to listing 1).

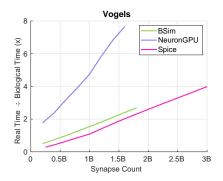
fashion (Fig. 4). This averages out any variance or skew present in the neurons' simulation costs. The effectiveness of this strategy depends on the assumption that the number of neurons far outweighs the dynamic range² of their costs, which is a necessary condition for any load balancing strategy (with neuron-granularity): If the dynamic range tended towards infinity, the possibility of finding a balanced partition would go to zero. Adversarial cases where every #GPU-th slice happens to be more expensive than the rest are rare and, if they occur, can be alleviated by changing the slice count.

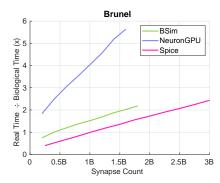
The split happens analogously to Section III-D (albeit with many more pivots) and, once again, can be performed implicitly during network construction. The neuron pool is not physically split but replicated across all GPUs. This wastes a few megabytes of memory but keeps global neuron IDs intact, absolving us from the need for (neuron ID-) translation tables. Each GPU only processes its assigned neuron pool slices by means of simple index manipulation (listing 1).

IV. RESULTS

We compare the performance of our simulator to that of BSim [11] and NeuronGPU [44] using three well-established models: Vogels-Abbott [48], Brunel, and Brunel with plasticity [49], detailed in [31]. We apply a scaling factor to synaptic weights allowing us to vary the network size while maintaining the models' characteristic firing patterns (detailed in [2]). We also use a synthetic model allowing us to vary network topology, size, density, activity (/firing frequency), and delay independently from one another. Unless otherwise noted, all synthetic benchmarks use a single, intra-connected neuron population and a delay of 1. The models will henceforth be referred to as Vogels, Brunel, Brunel+, and Synth.

²the ratio of the largest and smallest values that a certain quantity can assume.





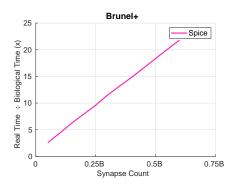
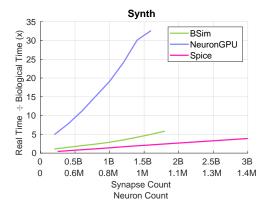


Fig. 5. Simulation time as a function of network size. We measure the time it takes to simulate 10 s of biological time for various synapse counts. We report wall-clock time ÷ biological time.



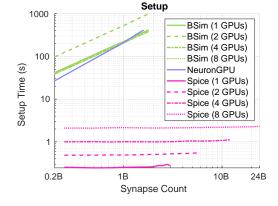


Fig. 6. Same as Fig. 5 but for the Synth model with density=0.156% and activity=0.5%. Neuron counts are provided below synapse counts.

Fig. 7. Setup time as a function of network size for the Synth model with density = 5%. Both axes are logarithmic.

BSim suffered from race conditions on Volta and newer GPUs which we fixed without negatively affecting performance. NeuronGPU and Spice worked out of the box. We implemented our benchmarks using the C++ API for BSim and Spice, and the Python API for NeuronGPU. All the code used for the experiments can be found at:

- BSim github.com/denniskb/bsim, forked from master as of Feb 19, 2020.
- NeuronGPU github.com/denniskb/neurongpu, forked from master as of Oct 20, 2020.
- Spice github.com/denniskb/spice, as of Jan 28, 2021.

All benchmarks were performed on a Google Cloud VM with an Intel Xeon E5-2699 v3, 8× Nvidia Tesla V100 16 GB (with P2P access), and 256 GB RAM, running a headless Ubuntu 20 with CUDA 11 and GCC 9.

A. Simulation Time as a Function of Network Size

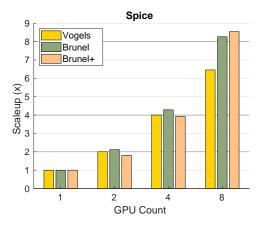
We measure the time it takes to simulate 10 s of biological time for various network sizes (synapse counts). We report wall-clock time ÷ biological time. All simulators scale close to linearly. While both BSim and NeuronGPU technically support spike-timing-dependent plasticity (STDP), we could not make use of it: BSim did not contain any code samples or documentation illustrating the use of STDP. NeuronGPU

does contain a STDP synapse type which unfortunately does not quite reflect the behavior of Brunel+. According to the authors, modifying it "currently is a task for developers, not for users".

It is fair noting that NeuronGPU uses double precision arithmetic and "exact integration" [50] as opposed to single precision arithmetic and Euler integration used by BSim and Spice, which certainly contributes to the performance discrepancy. It is also worth noting that Vogels and Brunel do not perform any faster compared to [2], in spite of the V100 being ~25% faster than the then-used 2080 TI. This is because we are bottlenecked by atomic operations. Brunel+, which is bandwidth-bound on the other hand, does run ~20% faster.

B. Simulation Time for Networks with Large Neuron Pools

Using our Synth model we study the performance of simulators when faced with massive neuron pools that do not fit into cache (Fig. 6). Currently the only way to achieve this is by creating very sparse networks due to limited GPU memory. Both BSim and NeuronGPU seem to exhibit a slight quadratic growth now with the "bend" happening at around 800K neurons which coincides with the V100's cache size. Thanks to the employed cache-aware spike transmission algorithm (Section III-C) our simulator continues to scale perfectly linearly.



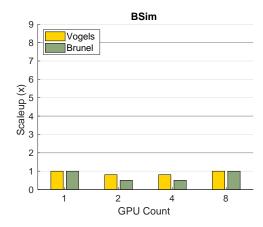
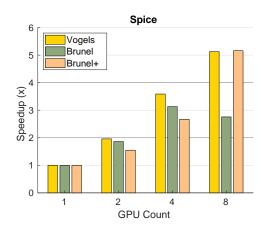


Fig. 8. Scaleup as a function of GPU count: How many times larger can we make a model on 2, 4, 8 GPUs while maintaining single-GPU simulation time?



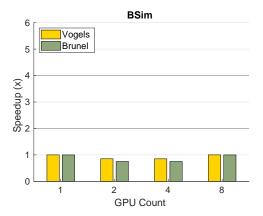


Fig. 9. Speedup as a function of GPU count: How much faster does the same model run on 2, 4, 8 GPUs compared to a single GPU?

C. Setup Time as a Function of Network Size

Fast setup is important as it allows the user to spend a greater portion of their time on running simulations. It also speeds up parameter exploration and -tuning. We see that Spice's setup is lightning fast because it is performed on the GPU (Fig. 7). We further see that it is virtually constant with respect to network size, meaning it is entirely dominated by spooling up threads and allocating memory—our actual setup kernel generates networks at ~200M synapses/ms.

D. Multi-GPU Scaling

Our simulator scales with multiple GPUs in both space and time, allowing one to increase network size while maintaining simulation time ("scaleup", Fig. 8) or to cut down on simulation time while maintaining network size ("speedup", Fig. 9). Both scenarios suffer from a natural limit: spike synchronization time grows linearly with the number of GPUs—add enough and any simulation will eventually be bottlenecked by it, leading to sub-linear or even negative scaling. This effect sets in much earlier in the "speedup" scenario where per-GPU simulation time goes *down* with the number of GPUs, shortening the spike synchronization window. That is why we consider "scaleup" to be the predominant use case of our contribution.

As can be seen, we achieve close to linear scaleup except for Vogels running on 8 GPUs. Vogels has a highly erratic firing pattern alternating between periods during which almost every neuron fires and periods during which few or no neurons fire. While we avoid synchronization altogether if no spikes occur, we still need to download spike counts to determine that no spikes have occurred. In the 8-GPU case this takes enough time to delay subsequent simulation steps and prevent linear scaling.

In some cases our simulator even scales *super*-linearly. This is because making a network n times larger and then splitting it into n slices again does not yield the original network. If the original network needed to deliver S spikes to d recipients each, then a slice would need to deliver $S * \sqrt{n}$ spikes to $d \div \sqrt{n}$ recipients each. While the total amount of work stays the same, the trade-offs change.

BSim performs slower on multiple GPUs compared to a single GPU in our benchmarks. According to the authors, BSim "works well for huge networks with a large number of populations but does not perform well with small number of populations, especially when the numbers of neurons in each population are imbalanced". Our benchmarks fall into this category. On models that do favor BSim, the authors report a speedup of $1.5 \times -2.3 \times$ using 4 GPUs [11, Fig. 7].

TABLE I
COMPARISON OF MEMORY CONSUMPTION BY SIMULATOR

Simulator		BSim	NeuronGPU	Spice
Synapse footprint (adj. data)		8 bytes	9 bytes	4 bytes
Max. synapse count (V100)	Vogels	1.8B	1.6B	3.5B
	Brunel	1.8B	1.6B	3.5B
	Brunel+	-	-	0.8B
Peak RAM usage		200 GB	40 GB	100 MB

E. Memory Consumption

Each simulator's memory usage is summarized in Table I. BSim and NeuronGPU use twice the memory to store a synapse's adjacency information, compared to Spice. For non-plastic models this limits them to half the network size. For plastic models this difference is negligible as then VRAM consumption is dominated by the size of the synapse pool.

More importantly though, BSim and NeuronGPU use very memory-inefficient, intermediate data structures before compacting and uploading them to the GPU. This results in very high RAM usage (peaking at 200 GB in the case of BSim) which may be prohibitive for some users.

V. SUMMARY AND FUTURE WORK

We presented a SNN simulator that utilizes all available hardware at close to 100% efficiency, enabling the simulation of larger models in less time than ever before. The employed multi-GPU parallelization-, spike synchronization-, and latency hiding techniques are not tightly coupled to the rest of our pipeline and should be adaptable to a variety of simulators. Merely the strided load balancing strategy might prove difficult to adapt, seeing as most simulator designs lend themselves to a striped approach.

Several areas for future work can be identified. First, we would like to add support for per-synapse delays. Since the number of distinct delays is finite (and rather small for most models), an obvious solution would be to store per-delay adjacency lists. Instead of transmitting all spikes from *delay* steps ago, one would (in a loop) transmit 1-step old spikes via the first adjacency list, 2-steps old spikes via the second adjacency list, and so on. The total amount of work remains the same and with the help of CUDA Dynamic Parallelism one could also avoid overhead from additional kernel launches. More importantly, this feature would work completely orthogonally to the existing pipeline: each per-delay adjacency list would be split across multiple GPUs just as it is now. We could still hide spike synchronization latency but its efficiency would be determined by the minimum delay in the system.

Typical spike arrays are so small that the spike synchronization time is entirely dominated by CUDA API overhead (cudaMemcpy() calls), effectively serializing operations that ought to run concurrently. It is worth investigating whether the spike synchronization could be carried out more efficiently by the CPU instead, especially for eight or more GPUs.

```
// TID = thread ID
// NT = thread count
// S = slice width
// NGPU = GPU count
// GID = GPU ID
// N = neuron count
void updateNeurons(...) {
  for (int i = TID; ; i += NT) {
    int j = (i / S * NGPU + GID) * S + i % S;
    if (j >= N) return;
    onUpdate(neurons[j]);
  }
}
```

Listing 1. The basic structure of our neuron update kernel. The neuron pool ('neurons') is replicated across all GPUs. Each GPU only processes its assigned slices though, via simple manipulation of the loop index.

Another interesting research direction is procedural connectivity [51]. The authors only store the *parameters* used to create the network and then generate adjacency data on the fly. Perhaps procedural generation could be used for other aspects of a SNN model, too.

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