Variability and disturb sources in ferroelectric 3D NANDs and comparison to Charge-Trap equivalents

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***Abstract*—We investigate physical mechanisms driving the retention and disturb of charge-trap (CT) based and ferroelectric-(FE) based 3D NAND string. Combining a calibrated CT 3D NAND model and calibrated material properties of the FE material (extracted from FE-FinFET), we extrapolate and compare the existing workhorse with the low-power, high-speed contender. We show that: (1) a inherently discretized FE-stabilization combined with the polycrystalline nature of HZO, and interface charge compensation guarantees MLC capability; (2) FE 3D NAND offers higher ON currents that enable further Z-scaling. Furthermore, we develop a retention model and show that independently of the inherited discretization of the storage layer, lateral charge migration (of the parasitically trapped charge that stabilizes polarization) combined with pass voltage (disturb) can cause retention loss of FE 3D NAND. Finally, integration (layer-cut) and material engineering approaches are suggested for mitigation and guaranteeing stable operation of the string.**

Keywords— 3D NAND, charge-trapping, ferroelectric HfOx, FeFET, NVM

I. Introduction

The stabilization of ferroelectricity [1] in CMOS compatible and scalable transitional-metal-oxides made ferroelectric (FE) based-FeFET technology often referred to as a potential game-changer, that would enable low-power storage and analog in-memory computing. Beside a significant increase in speed (1000x) and reduction in operation voltage (6x), 3D-NAND-like FeFETs [2] might also offer an endurance beyond NAND's (10^4 cycles) [3]. However, to be competitive with CT-based 3D NAND Flash, FeFET based 3D NAND must have the multi-level capability. Even though it has already been shown that FE 3D NAND devices may achieve the multi-level-cell operation (MLC) [4] (required for high-density storage), their stability due to the cell-to-cell (C2C) crosstalk and disturb is still unknown. Starting from the CT 3D NAND cell data and variability sources, we analyze the string's reliability and C2C crosstalk and develop a retention model fully capturing the experimentally measured lateral charge migration (LCM). Calibrated channel properties combined with HZO characterization and first principles input of interfaces, phases, and defects were used to extrapolate and investigate Erased-Program-Erased (EPE), Neutral-Program-Neutral (NPN) modes of adjacent cells as one of the most critical configurations in NAND string and physical mechanism behind. Understanding the physics underlying the disturb and retention mechanism is crucial to effectively compare FE and CT equivalents and engineer novel superior cells. For that purpose, we developed material to device (M2D) ecosystem built around the Ginestra® M2D platform [5] coupled with Density Functional Theory (DFT) calculations and extensive electrical characterization. Developed calibrated models and characterized films and devices were used to investigate if the FE-based 3D NAND can guarantee stable retention and MLC capability.

II. Charge Trap 3D NAND

In this section, the properties of the CT 3D NAND will be addressed. The first part will focus on the variability sources originating from the channel and taper angle, a common denominator for both CT and FE variants of NAND architecture.

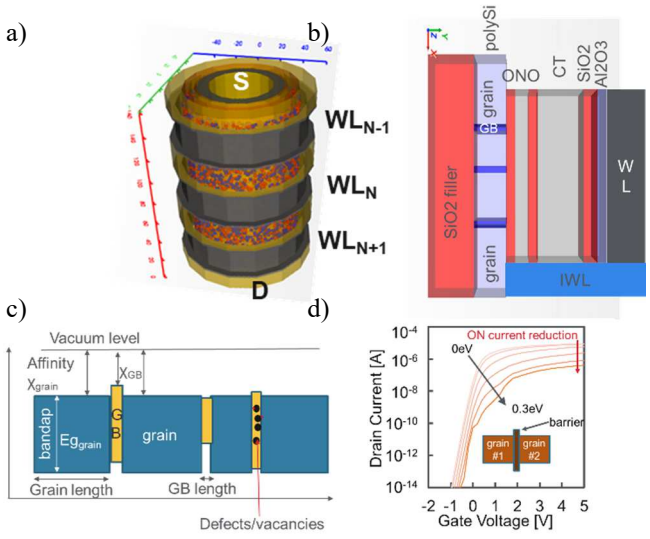

Fig. 1. a) 3D NAND string; b) cross-section of the CT 3D NAND device with depicted grains and grain-boundaries within the channel; c) Channel with grains and GBs in the energy domain. d) ON current degradation and V_{TH} hike toward higher V_G-s with increasing GB barrier.

A. Channel

To capture the mobility degradation and scattering on grain boundaries (GBs) of the polySi channel, we reconstructed a highly granular channel material as shown in Fig.1b enriched with DFT-derived properties of polySi grains, i.e., bandgap – E_g and the energy barrier between grains. Polycrystalline channel in energy domain is sketched in Fig.1c. Defects located on the grain boundaries (GBs) between the different grain orientations and their occupancy modify the electron affinity and result in a barrier that causes electron scattering yielding ON current

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reduction and (see I_D-V_G, Fig. 1d) V_{TH} hike toward higher fields with the increasing grain-to-grain barrier.

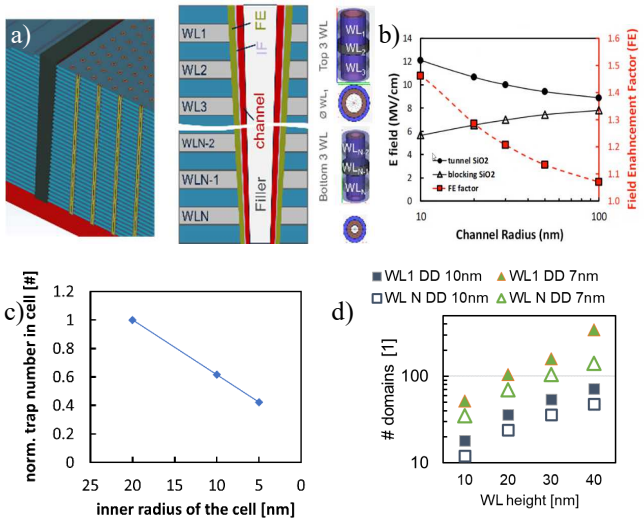

Fig. 2. 3D NAND stack with focus on a) taper angle and b) diameter change induced voltage divider modification across the stack along the string. A number of c) defects and a number of d) domains inside the storage part of the cell depending on the: 1) inner radius of the cell, 2) WL width and domain diameter - DD.

B. *Geometry – taper angle*

Besides the channel and variability originating from its polycrystalline nature, the imperfect deep memory hole (MH) etch results in conical shape and taper angle (Fig.2a). Consequently, the voltage (capacitance) divider comprised of filler oxide, channel, and dielectric layers changes its ratio due to the gradual change of the cell footprint, especially on the top and the bottom of the deck (Fig.2b). Besides altering the voltage divider, the volumetric density of the storage layer also changes. This directly affects the number of defects and number of domains (as explained later in section III) in the layer, which gradually drops, causing additional variability source that must be tackled on the system level when operating the array. This progressive drop with an inner radius of cell is shown in Fig. 2.

Combining those two variability sources with the SiN charge trap layer's defect distribution, we obtained distributions that fully captured (Fig. 3a) the experimental behavior of the 3D NAND devices reported in [6]. To further validate our model, we conducted an experiment investigating the impact of grain size increase towards no-grain epitaxial-like channels. Similar to the experiments, grain size increase resulted in V_{TH} reduction, ON current increase, and decrease of the subthreshold slope (STS) due to the reduction of severity of scattering mechanisms (defects and GBs) in the epitaxial channel. An increase of more than 100x was achieved, fully mimicking the experimental data reported in [6]. The developed model was used to analyze the disturb operations and cell-to-cell (C2C) crosstalk. In the following, we characterize the retention properties depending on adjacent cells' PRG/ERS mode and investigate the required oxide thickness (inter wordline spacing - iWL) between two wordlines (WLs) to guarantee a stable operation.

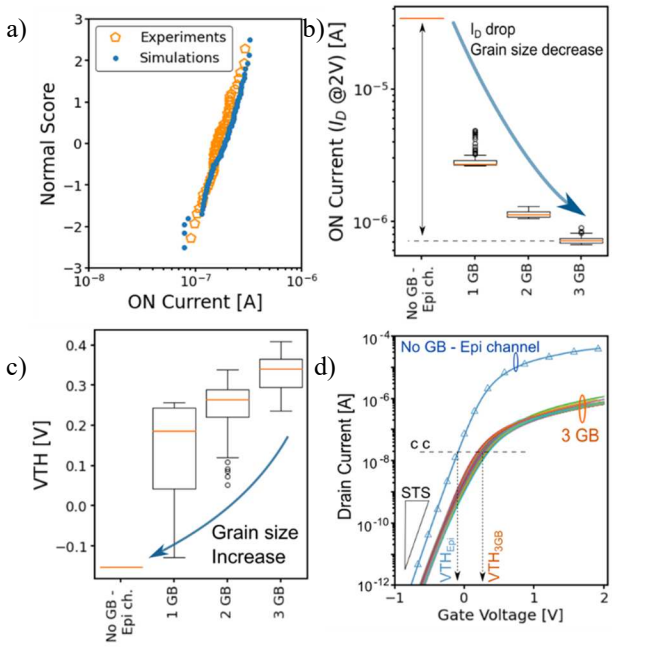

Fig. 3. Channel and taper angle induced variability. a) Calibrated ON current at overdrive voltage. b) ON current reduction and c) V_{TH} decrease with grain size decrease. d) 100x ON current increase with transition from polySi to epitaxial channel.

C. *Lateral charge migration and C2C crosstalk*

The retention evolution with time was studied and modeled at elevated temperatures depending on the mode adjacent cells were set in by the corresponding program – P, erase – E operations, and keeping cell in the neutral – N state. Three modes were analyzed N-P-N, E-P-E, and P-P-P. After setting the string in the erased state or keeping it in a neutral state, the retention of the central cell was analyzed. The retention of the central cell (CC) (after 4V program) with adjacent cells in P, N, or E states was simulated, and the charge dynamics of the system are shown in Figure 4. N-P-N and E-P-E configuration result in a rise of the internal field between the neighboring WLs, which drives the charge redistributions. Clear correlation with internal field and retention losses are observed. In the P-P-P mode, V_{TH} drift reduces significantly compared to other modes because the diffusion of electrons stored in the target cells is suppressed by the field generated by the electrons stored in adjacent cells. The developed model fully reproduces the experimental results reported in [7]. Furthermore, our model shows that at least 25nm thick iWL spacing between WL is required (Fig.4e) to prevent LCM-induced disturb. Alternatively, different more complex integration schemes can be employed to mitigate the disturb.

III. Ferroelectric 3D NAND

In the following FE-based NAND string will be assessed. Storage-wise, the CT layer in 3D FE NAND is replaced with the FE layer, positioned on top of the SiO_2 interfacial layer. It should be kept in mind that this is not the only change. The replacement of the charge trapping stack (comprised of ONO tunnel oxide, SiN CT-layer, and blocking oxide) with the FE HZO layer significantly simplifies the integration and reduction of the steps required to fabricate the 3D NAND. We utilize the previously

calibrated channel to benchmark the performance and couple it with the SiO_2 interfacial buffer layer and FE HZO on top.

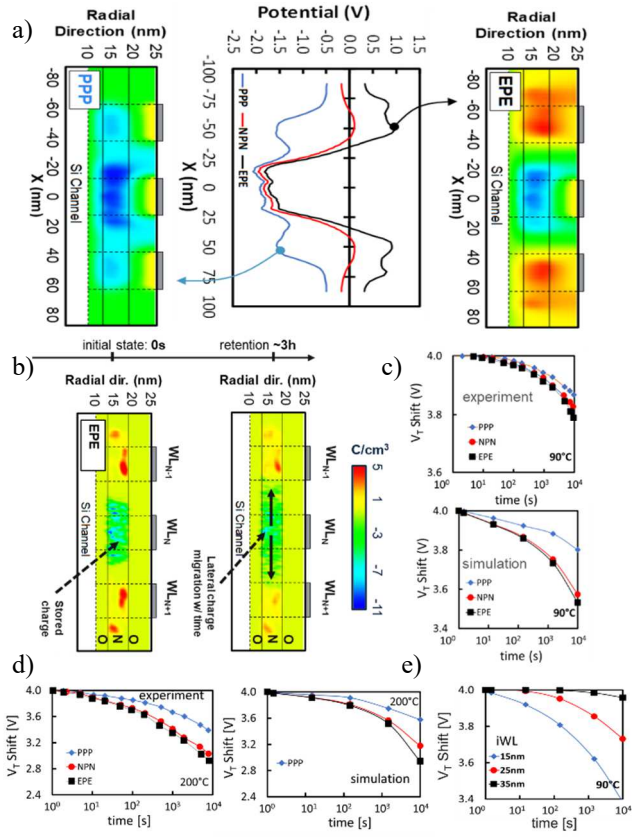

Fig. 4. a) Cell cross-section and resulting internal field generated due to the E-P-E/ P-P-P and N-P-N modes of the array. b) retention loss due to the lateral charge migration driven by the internal field. Comparison of different string modes at elevated temperatures: c) 90°C and d) 200°C. e) impact of the iWL on the P-P-P, N-P-N and E-P-E modes.

A. *HZO induced variability*

The properties and defects in polycrystalline FE HZO were studied by combining the electrical characterization of FE capacitors (FeCaps) and FE FinFETs [8] with DFT simulations and the modeling platform Ginestra® [2]. The developed films exhibit maximized coercive field (E_c) and reduced remnant polarization (Pr), which are essential for reducing the depolarization field of FeFETs [9]. In addition, the interfacial properties between HZO and SiO_2 are investigated as they play a crucial role in polarization stabilization and electron-assisted polarization switching [8]. FE HfO_x has multiple phases, i.e. [monoclinic (m), tetragonal (t), and FE and non-FE orthorombic (o)], separated by O-vacancy rich grain boundaries (GBs). HfO_x phases have different preferential directions of domain growth, k-values, and defect energies that result in different distributions of E_c and P_r.

The properties of O-vacancies (Vo-s) and electron (e^-) traps at SiO_2/HZO interfaces (Fig. 5a) and at GBs between crystalline and crystalline and amorphous HfO_2 phases (Fig. 5b) calculated using DFT show broad distributions of defect characteristics. Injected e^- can trap at GBs in deep states with >1 eV thermal ionization energies and at Vo-s. The calculated defect properties are compared with those obtained experimentally [8,9] and used to understand the SiO_2/FE interface, which is essential for the analysis of retention and disturb that will be discussed below.

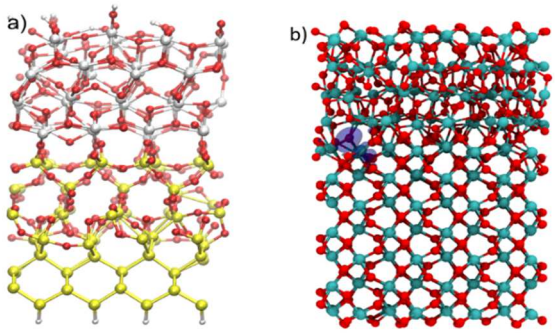

Fig. 5. Structures used in DFT simulations. a) The Si/SiO_2/HZO stack used to calculate properties of defects at SiO_2/HZO interfaces. b) The (o)-HfO_2/amorphous (a)- HfO_2 interface used to study electron trapping at GBs.

B. *FeFET variability*

The calibrated channel, interface, and HZO properties were employed in a multitier model of the 3D-FE NAND and combined with the FE switching and defect properties model. An electron scattering on the GB of the polySi results in ON current degradation, V_{TH}, and sub-threshold swing (STS) fluctuations (Figs. 6a and 6b). We deconvolve the variability sources and simulate the impact of the WF, polySi, FE fluctuations, and trapping on MW, ON current, and STS. We identify the polySi channel as the primary source of device-to-device variability. At the same time, the impact of FE is minimized (averaged out) due to the larger number of domains within the cell (Fig. 2d and Fig. 6b). However, similarly to the CT equivalent, taper angle results in domain number reduction and increasing variability in the cell (see Fig. 2). The higher-k and lower thickness of the FE gate stack result in better gate coupling yielding a much steeper slope and higher ON current than the CT-based equivalent (Figure 6c). The ON current increase of 8x enables further WL stacking and Z-scaling before hitting the sense amplifier limit compared to CT-equivalent.

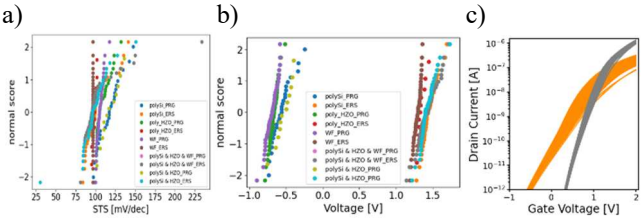

Fig. 6. Variability of the 3D FE NAND. a) STS and b) V_{TH} of PRG and ERS deconvoluted based on the variability source. c) Comparison of the CT and FE based cell (orange – CT and gray – FE device).

C. *FE 3D NAND Cell to cell crosstalk and disturb*

Similar to the trapped charge in CT-based 3D NAND, a polarization charge creates an internal bias field (opposing sign compared to the CT) when adjacent cells are set in N-P-N and E-P-E mode (Fig.7a). The storage layer of FE 3D NAND is inherently discretized compared to the CT equivalent. Namely,

during the stabilization anneal (required for stabilization of FE phase), the stress of barrier metal results in stabilizing the FE phase directly under the WLs while the inter-WL space remains non-FE. In turn, domains are confined in FE-phase stabilization discretized space (Fig.7b). This inherent discretization prevents crosstalk and enables scaling of iWL to point when capacitance and coupling between two adjacent WLs become significant (~7nm). Confined storage space and utilization of the ISPP/ISPE algorithms enable storing of at least four state (2 bits) in an 8nm thick HZO cell (Fig.7c). Due to the balance between the charge compensation between the interfacial charge and target polarization, multiple polarization states are stable after the state is set [8]. An increase of the HZO thickness opens the MW and enables the storage of more states but at the same time compromises retention by increasing the depolarization field.

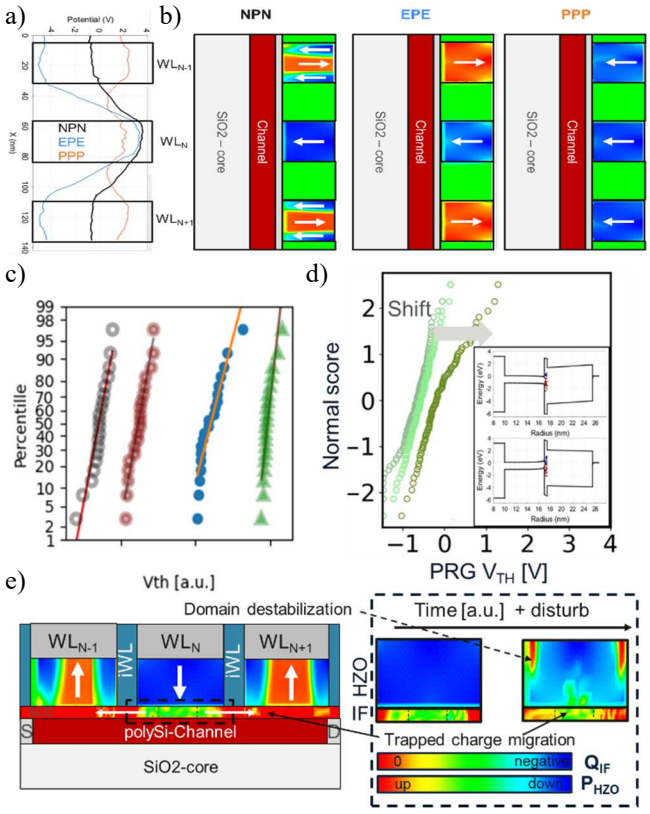

Fig. 7. a) Field distribution across the 3 adjacent WLs and their b) polarization configuration Retention. c) MLC capability of the cell and d) retention loss of PRG state due to the disturb (V_{pass}) and e) lateral charge migration inside the SiO_2. Inset inside d) denotes causality of flipped domain and compensating charge at interface observed on band diagram.

Depolarization field (originating from the imperfect screening of FE) magnified by capacitance divider of the cylindrical geometry (Fig.2b) is minimized by the parasitic trapping in interfacial SiO_2. As shown in our previous study [8], electrons compensate for the absence of the electrode (on the channel side) and stabilize the retention. However, due to the previously discussed internal field (generated by polarization orientation) between the WLs (Fig. 7a), a lateral charge (polarization stabilizing charge) migration occurs along the SiO_2 (which is continuous along the string) combined with the pass voltage disturb results in retention loss of the low V_{TH} – programmed state. To mitigate this issue, multiple pathways are possible: a) integration solution – integration approach that discretizes the SiO_2 interfacial buffer layer would prevent this charge loss; b) material engineering solution – increase of the coercive voltage of the material (e.g. AlScN alternative) and decrease of the remnant polarization would minimize the depolarization field and remove the need of parasitically trapped charge that stabilizes polarization (in case of high P_r mixtures).

TABLE I. FE AND CT CELL PROPERTIES AND COMPARISON

	Cell and integration properties					
	P/E amp	***P/E speed***	***Energy***	***iWL***	***Storage cut need***	***V_{pass} disturb***
CT	24V	100us/ 10ms	>1fJ/bit	20+nm	Y	No
FE	3-4V	100ns – 1us	<1fJ/bit	~7nm	N (but SiO_2 Y)	substantial

IV. CONCLUSION

In this study, we benchmarked a FeFET-based- against charge-trap-based- 3D NAND (*Table I*). Starting from the CT 3D NAND, we calibrated and developed unified variability and physical-retention model which successfully mimicked dynamics of lateral charge migration. This model was used to study the limitations of the CT 3D NAND integration scheme, cell-to-cell crosstalk and disturb. We calibrated the polySi channel, FE properties, and predicted variability and crosstalk of the FeFET-based 3D NAND equivalent. Finally, we show that in order to prevent retention loss (induced by combination of the internal field, generated by the N-P-N and E-P-E modes, and V_{pass}-disturb) it is required to either: 1) discretize the interfacial buffer layer (to guarantee stable retention of FE based array) or 2) conduct material engineering (or use e.g. AlScN), which would increase the coercive field of the material and maintain the charge balance between polarization and interfacial charge.

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