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Design-Time Reliability Evaluation for Digital Circuits

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***Abstract*—A new method of evaluating the reliability of combinational circuits is proposed, this method uses two levels of characterisation: a Stochastic Fault Model (SFM) of the component library and a design-specific Critical Vector Model (CVM). The idea is to move the high-complexity problem of stochastic characterisation of parameters into the generic part of the design process, and do it just once for a great number of the specific designs. The SFM captures variations of the vector of parameters of a library component fault model, those causing a transient fault at the component output; it is meant to be supplied by the foundry, similar to timing library files. The CVM is derived by a limited number of simulation runs on the specific design, and represents the boundary between the erroneous and error-free operation, w.r.t. the vector of parameters of each component. The probability of error-free operation is subsequently calculated by jointly using SFM and CVM. The method is demonstrated on a chain of inverters for simplicity, and subsequently applied to a 3-bit full adder. A complex three-way trade-off between energy, performance and reliability is explored. The method is meant to serve as a basis for design-time reliability evaluation and run-time power-reliability management. A slow stage is added to the circuit under test to improve its reliability.**

I. Introduction

Soft errors caused by neutron particles became a major concern for the reliability of electronic circuits. Since 1990, studies have been carried out to investigate the effect of radiation on ICs. At that time, the minimum observed Linear Energy Transfer (LET) was $15MeV.cm^2/mg$, and the duration of the measured Single Event Transient (SET) was 40ns, at high values of LET, which was enough to introduce an error at the system level. In 2004, LET by value at $2MeV.cm^2/mg$, was sufficient to cause a transient pulse with a duration of a few nanoseconds [1], [2], this can be referred to the technological scaling [3]. Methods were suggested to calculate the soft error rate caused by the radiation effect. Fast Analysis of Soft Error (FASER) was proposed in [4] and a symbolic method based on Binary Decision Diagram (BDD) and Algebraic Decision Diagram was presented in [5] to estimate soft error rate and Failure In Time (FIT).This is done by injecting a transient pulse to the circuit at different input combinations and observing the effect of logical and electrical masking. In [6] the author presented an SER analysis method by using a parametric waveform model based on Weibull function to describe particles strike. The authors in [7], [8], used Monte Carlo simulation to compute Soft Error Rate (SER), this was done by using the nuclear database of neutron-silicon interaction that was built with Monte Carlo simulation. Other methods for analyzing and measuring SER in combinational circuits are studied in [9], [10]. All these methods used Monte Carlo simulation.

The reference methods do not resolve the design-time complexity problem. We propose a method, where the high-complexity task of stochastic characterisation is moved into the platform development stage, which is meant to be performed at the foundry. This will allow the design companies to derive the reliability metric of their designs by a low-complexity procedure.

The proposed method uses two levels of characterisation: a Stochastic Fault Model (SFM) of the component library and a design-specific Critical Vector Model (CVM).

The SFM, for example, may include a probability density function (PDF) of neutron energy, and a model of the current pulse in the transistor as a function of the neutron energy. Its purpose is to represent the cause of faults, so it is fixed and applicable for any design or system under test, possibly expressed in non-electrical terms (e.g., particle energy distribution), as electrical effects (e.g., a voltage pulse at a gate output having its magnitude, duration and arrival time stochastically described). The parameters of the electrical effects form a Parameter Vector (PV) used further in the CVM derivation.

The CVM is derived by a limited number of simulation runs on the specific design, and represents the boundary between the erroneous and error-free operation, w.r.t. the PV. In the above example, the PV includes the shape (a function of LET) and arrival time of a voltage pulse. A number of analogue simulations are performed to determine the LET-time pairs representing boundary conditions between error and no error at the primary output.

Finally, the probability of error-free operation is calculated by combining SFM and CVM as a probability of the PV not reaching the critical values of CVM.

II. CIRCUIT UNDER TEST

A long chain of inverters is intended to mimic a single path through an arbitrary logic circuit used as a part of a synchronous clocked automaton operating under voltage-frequency scaling. The frequency is chosen as a performance metric. It is determined for each value of the voltage supply

Vdd by simulating the circuit and measuring the propagation delay, no margins added. The circuit includes 205 identical inverters implemented with UMC 90nm foundry design kit, all transistors are 80nm in length (standard for this library), pull-down transistor is 400nm, pull-up is 800nm in width (these values as similar to those used in a commercial standard-cell library), standard threshold voltage, standard use Vdd = 1V.

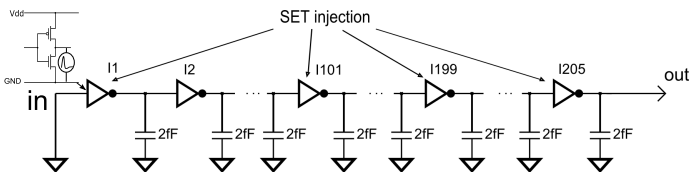

Fig. 1: Circuit under test

Between the inverters there are wires, whose parasitic capacitance we simulate as 2fF capacitors (typical capacitance of a short interconnect wire). In our experiments we estimate the reliability of only four inverters in this long chain, as illustrated in Fig. 1, the values for all of them are very similar, while a minor difference is observed only in the last stage. Therefore, the reliability of all inverters in the path, except the last one, can be accepted to be the same.

The fault model used in this work is an SET pulse modelled as in [11] and injected into a single gate (e.g., the left inverter in Fig. 1). An example of SET pulses in a single strength inverter under different Vdd and LET is shown in Fig. 2. In this model the particle energy is expressed as a metric of LET; this is because we are interested not in the neutrons themselves, but rather in the effect of their interaction with the transistor.

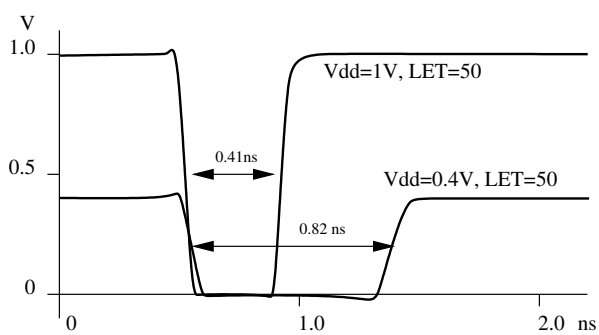

Fig. 2: SET pulse

III. DERIVATION OF RELIABILITY

This section describes the core of the method which does not require Monte Carlo simulations for gaining statistics on the output errors. Instead, the SFM is converted into the reliability value through the properties of the circuit (expressed as CVM).

The first objective of this stage is to find whether an SET would cause an output error of the whole circuit comprising multiple gates (a long chain of inverters in our example) or not. The second objective is to calculate the probability of error-free operation or reliability.

An output error is defined as a Single Event Upset (SEU) [12]–[14], which is an effect of an SET when the latter becomes latched in a flip-flop connected to the output of the combinational circuit with the SET on it. A difficulty here is that not all SETs result in an SEU. Some SETs disappear before the clock signal, or appear too late w.r.t. it. Furthermore, the magnitude of an SET may be below the threshold of the flip-flop sampling, or its duration may be insufficient to be latched, or it may disappear while propagating through the path due to individual stages exhibiting inertial delay behaviour, and suppressing the short duration pulses.

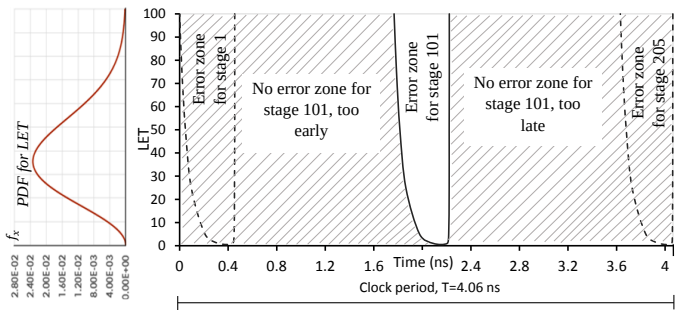

Fig. 3: Critical values of the interference vector

The first objective is achieved by identifying the PV (in this experiment it is an SET characterised with two parameters the LET and arrival time) and simulating the circuit in order to determine the critical values of this vector (PV values causing a transition at the end of the clock cycle). We repeat this for different Vdd values in order to see how reliability changes under voltage-frequency scaling (the clock period is adjusted to the propagation delay under each Vdd value).

Fig. 3 mainly shows the critical values of the interference vector in case of the SET is injected in stage number 101 at Vdd = 1V, for different LET values, these critical values draw a boundary line that separates two zones the error zone and no error zone. The clock period defined as a propagation delay without any margins is T=4.06ns. It is easy to adjust the results to any timing margins used in a particular design, but it is not included in this paper. For the other stages in the path the diagrams are very similar, just shifted left for the low stage numbers and right for the high numbers, *for example* error zones of stage 1 and stage 205 on Fig. 3 explain the difference between the error zones of the three stages.

The second objective is achieved by using the graph in Fig.3 to calculate the probability P_{err} of the system being in the error zone. For this we use the PDF function f_x for LET x_{LET} and the PDF function f_t for SET arrival time t_a; the former known from the fault model, the latter having uniform distribution due to asynchronous nature of SET events. P_{err} in (1) is calculated for a single clock cycle.

$$P_{err} = \frac{\iint_{errorzone} f_x(x_{LET}) \,.f_t(t_a).dx_{LET}.dt_a}{\int_{t=0}^{T}\int_{e_{LET=0}}^{\infty} f_x(x_{LET}).f_t(t_a).dx_{LET}.dt_a}.T.r_{SET} \quad (1)$$

The integrals in (1) are computed numerically. Note, the PDF of the arrival time is constant, i.e., $f_t(t_a) = 1/T.r_{SET}$, where T is the clock period, and r_{SET} is a constant representing SET rate. Instead of the infinite integration limit for e_{LET} we choose 100, as the probability of exceeding this limit is negligible [22]. The PDF of LET in Fig.(3) is defined as Maxwell-Boltzmann formula (2):

$$f_x = \sqrt{\frac{2}{\pi}}.\frac{x_{LET}^2 e^{-x_{LET}^2/(2a^2)}}{a^3} \tag{2}$$

With constant a calculated from $a = \frac{\mu}{2}\sqrt{\frac{\pi}{2}} \approx 25.06$

This is for the probability of error when an SET is injected in the stage 101 of the path. The same procedure was repeated for the other stages, and the computed figures were the same apart from the last five stages, where the probability of error was gradually reduced towards the end, and the last stage produced 10%-20% lower error probability (depending on Vdd), more details can be found in the next paragraph. For low SET rates it is reasonable to assume that no more than a single SET can take place in the path in any particular clock cycle, which leads to the formula (1) being applicable to the path error, and r_{SET} becomes the SET rate in the path. The reliability can be calculated as absence of error, i.e., $P_{reliability} = 1 - P_{err}$.

A. Reliability of a uniform path

The proposed method for deriving a circuit reliability was applied under a range of Vdd values to see the trend of changing the reliability with supply voltage. The error probabilities were calculated and plotted in Fig. 4. The SET rate was chosen as $r_{SET} = 20n.cm^{-2}.h^{-1}$ [15], i.e., 20 neutrons per hour hitting one of the inverters in the path, which is abnormally high. It is interesting that the error probability is reduced if SET is injected in the last stage. This is an effect of the SET expanding when propagating along the path [16]. This expansion only happens when SET is long, i.e., the LET causing it is high. There is no path attached to the last stage, hence no expansion, and lower error probability as a result. Also, the trend of error probability of the last stage at low voltages is different from other cases because the absence of next stages attenuation effect.

Note that in these diagrams the probability of error is calculated per a single clock cycle, rather than per second of operation. This metric is relevant to completion of fixed computational tasks. the overall probability of error is calculated for the circuit and it is illustrated in Fig. 10.

A 3D diagram in Fig. 5 depicts a three way trade-off between energy, reliability and performance, which is one of the main results in this paper. It shows that in the low-energy corner both the reliability and performance drop rapidly, which results in a recommendation to avoid this corner. Interestingly, at very low Vdd the reliability improves again due to slow gates acting as filters for a narrow SET. It is a promising result for extremely low-power designs.

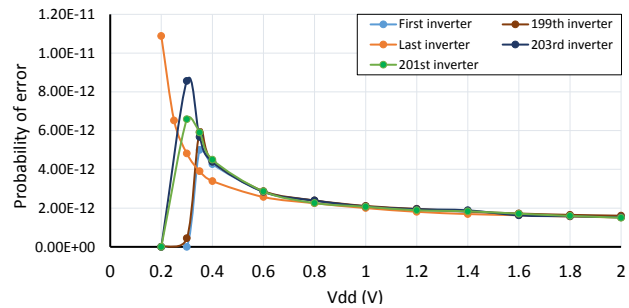

Fig. 4: Error probability vs Vdd

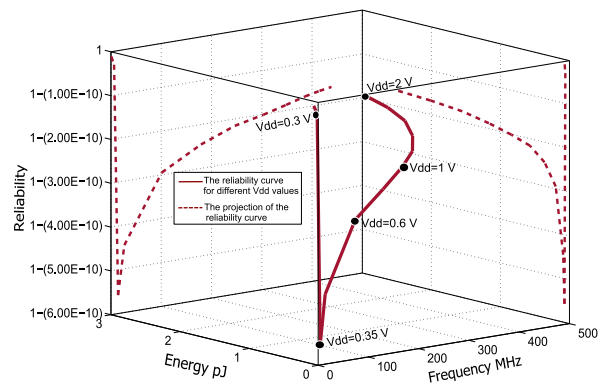

Fig. 5: Energy-Reliability-Performance trade-off

B. Non-Uniform Path

With non-uniform paths (composed of different gates) one cannot rely on many stages contributing equally to the overall probability of error. This means more simulation runs resulting in different CVM for each fault location. At the time of this report we did not have an automated tool for this purpose. Therefore, just one benchmark was processed by hand: the carry path in ISCAS c6288 circuit. The resultant trade-off graph is similar to Fig. 5. A potentially useful effect was observed: the slower gates filter out the glitches which are shorter than the inertial delay of the gate, thus improving the reliability. This effect is studied in Section VI, where a localised anomaly is added to the otherwise uniform path, leading to a dramatic reliability improvement.

IV. MULTIPATH CIRCUITS

In this section we show how the above method of reliability calculation can be applied to a multipath circuit. For simplicity we choose a 3-bit full adder as a benchmark, which is shown in Fig. 6.

Now consider an SET occurring in the inverter I1 and propagating to the outputs through the sensitive paths. The configuration of such paths depends on the input vector applied to the circuit. For example, let's consider the vector $X1 = \langle a0, a1, a2, b0, b1, b2, ci\rangle = \langle 0, 0, x, 1, 0, x, 0\rangle$. The sensitive paths under this vector are shown in Fig. 7.

We simulate the circuit number of times for a fixed Vdd and range of LET values, similar to the chain of inverters

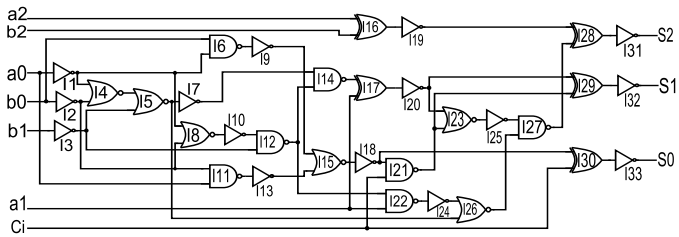

Fig. 6: 3-bit full adder circuit

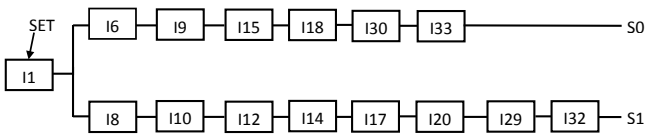

Fig. 7: Sensitive paths for the gate I1 and input X1

in Section III. This time, however, the critical values of the PV are registered when at least one of the paths (two of them exist in this example) produces a "borderline error" (the output voltage 50% of Vdd) at the primary output. The critical values are plotted in Fig. 8. This figure is similar to Fig. 3, just the error zone is wider due to the shortness of the path. The probability of error is calculated as before by using formula (1). In this case P_{err1}=2.47E-12.

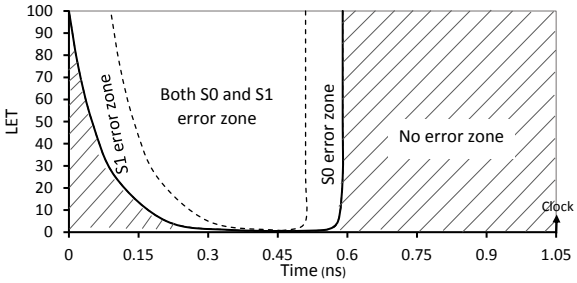

Fig. 8: Critical values for the gate I1 and input X1

The same procedure is applied to the other input vectors, $X2 = \langle 0,0,x,1,0,x,0 \rangle$ and $X3 = \langle 0,1,x,1,0,x,0 \rangle$, the whole input set consisting of only three vectors for simplicity. The calculated error probabilities for I1 are P_{err2}=2.87E-12 and P_{err3}=2.87E-12.

In order to calculate the probability of error for I1 under the whole set of inputs, one needs to know the probability of occurrence of each vector in the input stream, which is a part of the circuit specification. Take, for example, $F_{X1} = 30\%$, $F_{X2} = 20\%$ and $F_{X1} = 50\%$. Then, the weighted average of the error probabilities will be:

$$P_{err}^{I1} = \sum_{i=1}^{n} F_{X\,i} \cdot P_{err\,i} \tag{3}$$

Where n is the number of input vectors. By using the Formula (3), the P_{err}^{I1} = 2.75E-12.

The same should be repeated for each gate in the circuit. As the errors are infrequent, it is reasonable to assume that no more than a single gate will be affected, hence the error probability is the sum of error probabilities for each gate.

$$P_{err} = \sum_{j=1}^{m} P_{err}^{Ij} \tag{4}$$

Where m is the number of instances in the whole circuit. Formula (4) is used to calculate the overall error probability at Vdd = 1V, P_{err} = 8.65E-11.

Now, the overall reliability can be calculated.

$$P_{reliability} = 1 - P_{err} \tag{5}$$

This is a very basic and preliminary example only, because we are currently working on reduction of complexity of error probability calculation and automation of the simulation process, aiming at creating a set of benchmarks to be investigated in the context of reliability-performance-energy trade-off (as in Section III) and with various filters (as in Section V).

V. Improving the Reliability by Using a Filter Stage

Traditional methods for reliability improvement of logic circuits include using "hardened" cell libraries [17], [18], and fault masking [19], [20]. Our approach is different: it is based on adding a slow gate with a long inertial delay to the end of the path in order to stop propagation of short glitches representing SET; this is the effect of electrical attenuation [21]. In the experiment we use an example circuit described in Section II, where either the last stage only, or the last two stages are replaced with the gates of a different size. The weakest filter in the experiment is implemented as a 16x-size inverter at the primary output, while the strongest is constructed of a 0.5x inverter driving a 32x inverter (denoted as "0.5x+32x"). The idea of using two-stage combinations comes from the Logical Effort method [22], effectively doubling the inertial delay. All together, the following filters are simulated: 1x (no filter), 16x, 24x, 32x, 0.5x+16x, 0.5x+24x, 0.5x+32x.

A. Error probability with a filter stage

The Probability of error before and after adding the filter stage to the circuit is shown in Fig. 9, in the case of the particle hitting the first inverter. The probability of error is reduced gradually to small values in the filters with longer propagation delay and is also a function of Vdd.

It can be seen from Fig. 9 that the filters 32x and 0.5x+16x produce almost the same effect as expected according to the Logical Effort method. Therefore, the filters 0.5x+24x and 0.5x+32x are equivalent to 48x and 64x. At low voltages, the filtering effect increases, because the propagation delay of the filter becomes longer relative to the glitch duration. The experiment is repeated with different strike locations to find the overall probability of error that is shown in Fig. 10.

Fig. 11 shows reliability-performance-energy trade-off relation, so the improvement in the reliability after adding the filter

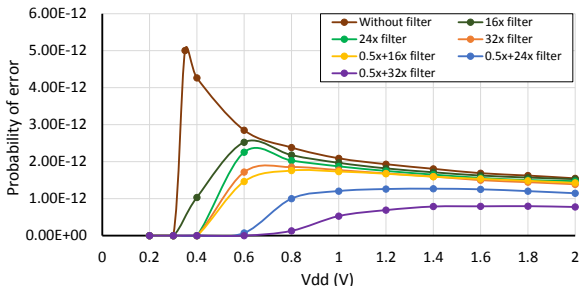

Fig. 9: Error probability for one stage with and without a filter

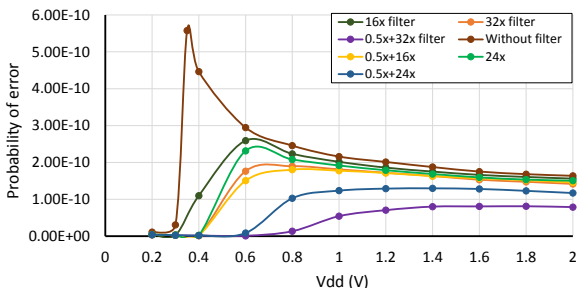

Fig. 10: Overall error probability with and without a filter

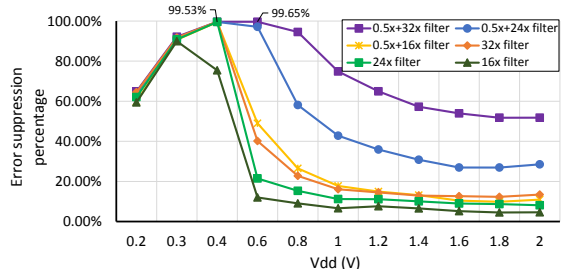

Fig. 12: Error suppression percentage vs. Vdd

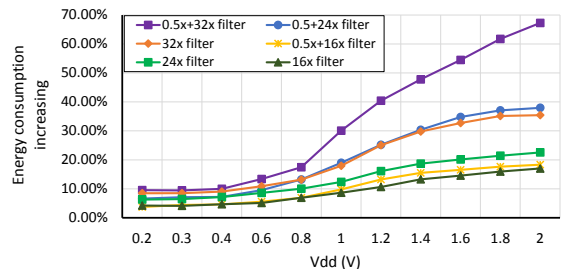

Fig. 13: The effect of filter stage on circuit's energy consumption

stage is significant regarding to the change in performance and energy consumption, which decreased and increased respectively by different values according to the strength of the filter stage. As it can be seen better filters consume more energy, because a slow signal transition in a CMOS gate causes short circuit current losses.

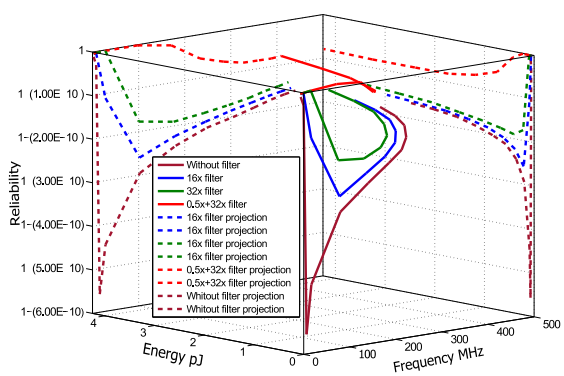

Fig. 11: Energy-Reliability-Performance after adding filter stage

Fig. 12, shows the error suppression percentage that obtained from each filter, the error suppression can be translated as an improvement in the circuit reliability, so it can be noticed that as the supply voltages decreased the reliability increased by different scales depending on the strength of the filter stage. For instance, it is obvious that the 0.5x+32x filter has the highest contribution in error suppression percentage.

B. The effect of the filter stage on the circuit parameters

The filter stage has drawbacks on the circuit parameters, such as a reduction in the performance, an increase in the energy consumption, and an increase in the area overhead of the circuit. Fig. 13, shows the effect of each filter on the energy that consumed by the circuit, so the 0.5x+32x filter contributes to the highest percentage of energy consumption. Even though, this percentage varies due to varying of the supply voltage. Moreover, if we compared between the two filters: 32x and 0.5x+16x we can notice that, from the energy consumption and the error reduction perspectives, it is better to use the two stages structure. Further work on low-energy filters is required.

The effect of the filter stage on the circuit performance is studied. A reduction in the performance is occurred in different percentages depending on the strength of the filter and the supply voltage. This change in the circuit performance is shown in Fig. 14. It can be noticed that, the reduction percentage is decreased with the decrease of the supply voltage, this might be because the circuit is already working in lower frequencies, so the filter stage contribution is low.

By taking a deep look at the results, we can build a good notion on the trade-off between energy consumption, perfor-

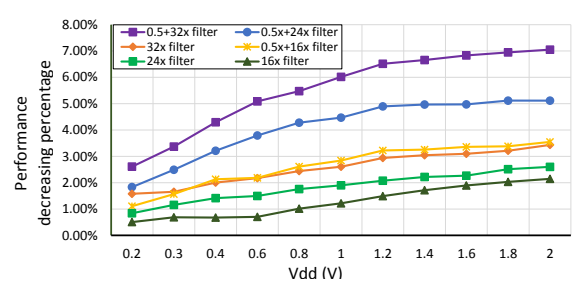

Fig. 14: The effect of filter stage on the circuit's performance

mance and circuit reliability, according to the contribution of each filter on each parameter.

Area overhead is a major concern for chip designers, so we studied the effect of filter stage on the area of the circuit by making a comparison between the area overhead that gained because of adding the filter stage into the circuit. Fig. 15, shows the effect of the filter stage on the area of the circuit. The area overhead is in acceptable range if it is compared with other techniques that used in system level, such as Triple Modular Redundancy (TMR), or information redundancy.

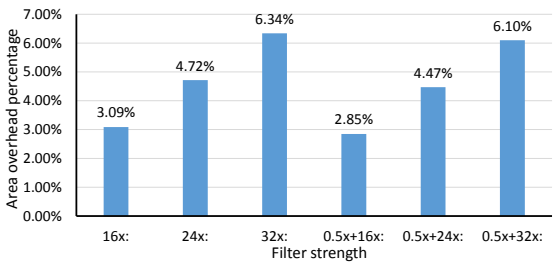

Fig. 15: The effect of filter stage on the circuit's area

VI. Conclusions

Two main achievements reported in this paper are a new method of derivation of reliability metric for digital circuits and a three-way energy-reliability-performance trade-off.

The reliability metric is derived without extremely expensive Monte Carlo simulations or physical experiments, which makes its inclusion into ECAD logic synthesis tools possible. This method may become an enabler for achieving the reliability closure on a system at an early design stage, similar to how the timing closure is addressed.

The method includes two stages. At the first stage the technology library is characterised under a chosen interference model, e.g., a neutron flux with a particular energy distribution, and then "translated" into the electrical domain as an SET model. This is done just once and not repeated for each circuit in the project. At the second stage, critical values for the vector of interference parameters are derived for a particular circuit under test by a limited number of simulations. The critical values are the border between the erroneous and error-free operation. Then, the probability of error is calculated.

The explored three-way trade-off is extending the traditional static or dynamic voltage-frequency scaling concepts by adding the reliability metric. It will help to select the operating point for circuits. It is also an enabler for a new generation of power management which controls the reliability dynamically -power or energy reliability management, PRM or ERM.

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