## Workshop on Multithreaded Architectures and Applications – MTAAP

## Theme

Multithreading (MT) programming and execution models, as well as Many Integrated Core (MIC) and hybrid programming with accelerated architectures, are now part of the high-end and mainstream computing scene. This trend has been driven by the need to increase processor utilization and deal with the memory-processor speed gap. Recent and upcoming examples architectures and processors that fit this profile are Cray's XK and XMT, NVIDIA Kepler, Intel Phi, IBM Cyclops, and several SMT processors from IBM (Power7), AMD, or Intel, as well as heterogeneous clusters with accelerators from AMD and NVIDIA. The underlying rationale to increase processor utilization is a varying mix of new metrics that take performance improvements as well as better power and cost budgeting into account. Yet, it remains a challenge to identify and productively program applications for these architectures with a resulting substantial performance improvement.

The MTAAP 2013 workshop is a full-day meeting to be held at the IPDPS 2013 focusing on Multithreading Architectures and Applications. This workshop intends to identify applications that are amenable to MT, MIC, and hybrid programming and execution models, as well as the underlying architectures on which they can thrive. The workshop seeks to explore programming frameworks in the form of languages and libraries, compilers, analysis and debugging tools to increase the programming productivity. Topics of interest, of both theoretical and practical significance, include but are not limited to:

- Multithreaded, Many Integrated Core, and Hybrid Architectures
- Heterogeneous architectures including graphics processors and other accelerators
- Programming Framework for MT, MIC, and Hybrid architectures
- Compilation and Optimization for MT, MIC, and Hybrid architectures
- Performance Analysis and Debugging Tools for MT, MIC, and Hybrid architectures
- Performance Metrics and Evaluations
- Libraries and run-time systems
- Innovative applications for MT, MIC, and Hybrid architectures

## Chair

Luiz DeRose (Cray)

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