Process-induced anomalous current transport in graphene/InAlN/GaN heterostructured diodes

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***Abstract*—Graphene and III-nitride semiconductors are promising materials platforms for the development of high-frequency, high-power electronic devices. Successful integration of these materials, however, requires a detailed understanding of the electrical properties of the graphene/III-nitride interface. In this work, we investigate the interfacial charge carrier transport across the graphene/InAlN interface. We show that at room temperature the leakage current in these devices is well described by the Fowler-Nordheim tunneling relation. Temperature-dependent measurements between 100 K and 400 K, however, show that as temperature decreases, the leakage current increases. This observation cannot be explained by Fowler-Nordheim or other standard conduction mechanisms (thermionic emission, Poole-Frenkel emission, trap-assisted tunneling). It is proposed that device processing, specifically polymer residue contamination, affects the interfacial coupling between graphene and the InAlN substrate, resulting in the observed anomalous current transport. Evidence for such a mechanism is provided by Raman spectroscopy and temperature-dependent atomic force microscopy studies.**

Keywords—graphene, InAlN, anomalous current transport, heterostructures

I. Introduction

Integration of monolayer graphene (Gr) with III-nitride semiconductor technology has demonstrated the potential to create new high-frequency, high-power electronic devices, such as Gr/GaN hot-electron transistors and Gr/AlGaN/GaN Schottky barrier diodes (SBDs) [1]–[6]. However, microfabrication of such Gr/III-N devices requires the transfer of graphene sheets onto the III-N layer, an inherently contamination-prone process in which residue can greatly affect device performance. For example, polymer residue can introduce unintentional doping and greatly diminish the mobility of graphene-field-effect-transistors [7]. The presence of interfacial residue is especially important in heterostructured devices where interfacial charge transport occurs between graphene and the substrate.

Here, we provide measurements of current transport across the Gr/InAlN interface. To the author's knowledge these are the first such measurements reported in the literature. We find that at room-temperature, reverse-bias current is well described by a Fowler-Nordheim tunneling model. However, the leakage current of the fabricated Gr/InAlN/GaN diode increases by a factor of 25× as temperature is decreased from 400 K to 100 K. This anomalous increase in leakage current at low temperatures stands in stark contrast to standard temperature scaling laws. We argue that this anomalous behavior can be explained by residue introduced during device fabrication processing, as evidenced by Raman spectroscopy and temperature-dependent atomic force microscopy (AFM) studies.

II. Device Fabrication

Devices were fabricated on an InAlN/GaN-on-Si wafer (DOWA) grown by metal−organic chemical vapor deposition (MOCVD) on Si (111). The epitaxial stack consists of 1 nm/15 nm/2 nm AlN/$In_{0.17}Al_{0.83}N$/GaN layers. A two-

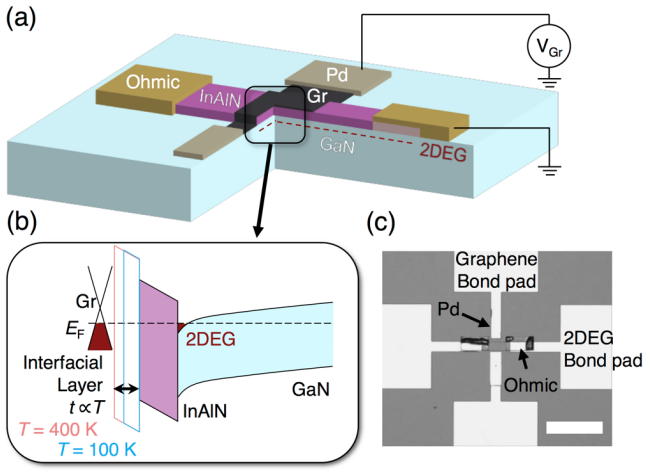

Fig. 1. (a) Schematic of fabricated graphene/InAlN/GaN device with the biasing network indicated. (b) Schematic band diagram of the fabricated device, with interfactial layer included. The increase in interfacial layer thickness (t) with temperature (T) due to process residue results in decreased current at increased temperature. (c) Optical micrograph of measured device. graphene channel runs vertically, 2DEG channel runs horizontally. Scale bar represents 100 μm.

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dimensional electron gas (2DEG) is present at the InAlN/GaN interface. This 2DEG is theoretically predicted to have a sheet density of 2.25 × 10^{13} cm^{-2} [8], consistent with Hall-effect measurements of devices fabricated on the same wafer. Rectangular InAlN/GaN mesas were etched in a BCl_3/Cl_2 plasma. Post mesa-isolation, a standard Ti/Al/Pt/Au Ohmic metal stack was deposited using a lift-off process [9]. The contacts were annealed at 850 °C for 35 s. Subsequently, CVD-grown graphene was transferred by a standard poly(methyl methacrylate) (PMMA) wet-transfer process [10]. The transferred graphene was then etched in an O_2 plasma to define the graphene channel. Devices were fabricated with both a 15 µm × 15 µm and 50 µm × 50 µm overlap between the graphene and 2DEG channels. Pd (40 nm) was used as an Ohmic contact to graphene. A ~20 nm Al_2O_3 passivation layer was deposited to passivate the device using thermal atomic layer deposition. A 3D schematic of the microfabricated Gr/InAlN/GaN devices is shown in Fig. 1a. A band diagram of the fabricated heterostructure is shown in Fig. 1b (excluding the Al_2O_3 passivation layer, and the GaN cap/AlN spacer for clarity). An optical micrograph of a fabricated device is shown in Fig. 1c.

III. Results and Discussion

A. Raman spectroscopy

The Gr/InAlN interface was probed via Raman spectroscopy using 532 nm excitation, presented in Fig. 2. Narrow Lorentzian peaks were observed at 1593 cm^{-1} (G) and 2680 cm^{-1} (G'). The G' peak was well fit by a single Lorentzian, with a full-width-at-half-maximum of 31 cm^{-1}, indicating the presence of monolayer graphene [11]. The G'/G peak height ratio of 1.3 is consistent with previous reports of monolayer graphene on GaN, where a suppressed G'/G ratio is observed [3]. A D peak was also observed at 1349 cm^{-1}, indicating damage was induced in the graphene during processing, however this peak is significantly smaller than the G and G' peaks (D/G < 0.1). In addition to the standard, narrow graphene peaks, we observed three broad gaussian peaks at 1382 cm^{-1}, 1452 cm^{-1}, and 1593 cm^{-1}. The broad peaks at 1382 cm^{-1} and 1593 cm^{-1} can be assigned to the D and G modes of disordered carbon, respectively, consistent with polymer residue being introduced during processing [12]. The peak at 1452 cm^{-1} is characteristic of PMMA, indicating we were not fully able to remove the PMMA support membrane [12]. Such broad peaks may also be present in standard graphene on SiO_2 samples, however they are not typically visible relative to the strong graphene peaks [12]. Though our data indicate the presence of polymer residue, these data do not allow us to determine whether this residue is above or below the graphene layer.

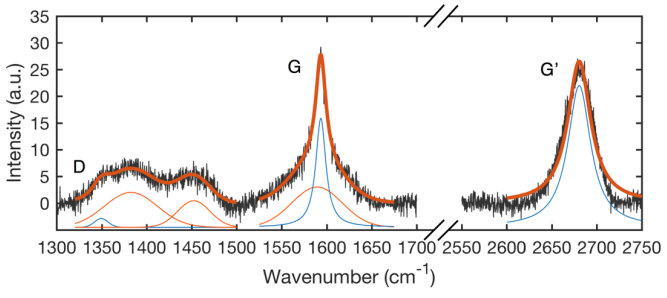

Fig. 2. Raman spectrum of the graphene channel showing narrow G, G' peaks, and D peaks (blue). Further broad peaks are seen at 1593 cm^{-1}, 1452 cm^{-1} and 1382 cm^{-1} (red) indicating the presence of disordered carbon. Curves for the individual fitted peaks are shown below the Raman data.

B. Electrical characterization

Temperature-dependent electrical measurement was conducted under vacuum in a cryogenic probe-station. Measurements were performed in 50 K steps beginning at 100 K and ending at 400 K. Three-terminal measurements of a Gr/InAlN/GaN device are presented in Fig. 3. In this transfer characteristic the graphene is used as a gate, while the source and drain contacts bridge the 2DEG channel, held at a constant bias of V_{DS} = 0.5 V. We observed that in both the on- and off-state, the drain current (I_D) decreased as temperature increased, by a factor of 3.2 and 22, respectively. This corresponds to an on/off ratio that varies between 74 and 510 at 100 K and 400 K, respectively.

The observed decrease in on-state current is consistent with decreased mobility leading to an increase in the sheet resistance of the InAlN 2DEG at higher temperatures [13]. To probe the off-state current, current-voltage characteristics were recorded across the Gr/InAlN interface. Here, graphene functions as a Schottky contact to InAlN. As indicated in Fig. 1a, the graphene is biased relative to the 2DEG and current flows laterally across the graphene layer, vertically through the Gr/InAlN interface, and exits through the 2DEG Ohmic contact. The measured diode characteristics of ten devices with varying Gr/InAlN overlap are presented in Fig. 4a, measured at room temperature in air. All devices show consistent diode characteristics. It is observed that there is a sharp increase in reverse leakage current between V_{Gr} = -2 V and -5.5 V, which levels out when the 2DEG is depleted (V_{Gr} < -5.5 V).

The diode characteristics of the same device presented in Fig. 3 were recorded under vacuum in a cryogenic probe-station, again in 50 K steps beginning at 100 K and ending at

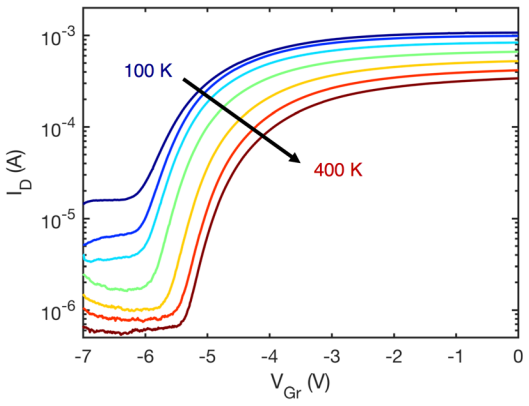

Fig. 3. Temperature-dependant transfer characteristic of InAlN/GaN channel transistor. Both on-state and leakage current decrease as temperature is increased from 100 K to 400 K. Device is held at a constant drain-source bias of V_{DS} = 0.5 V.

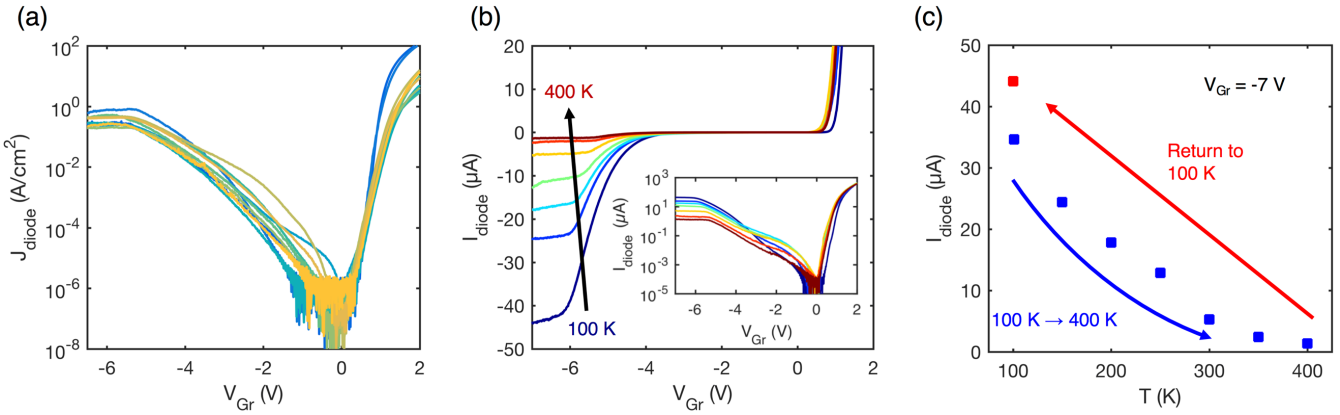

Fig. 4. (a) Room temperature measurement of leakge current in ten devices of various channel dimensions. (b) Temperature-dependent current-voltage characteristics of Schottky diode formed between the graphene contact and the InAlN/GaN 2DEG. An increase in the leakge current is observed at lower temperatures. Inset shows the same data plotted on a logarithmic scale. (c) Reverse leakge current at -7 V, showing a 25× decrease in magnitude as temperature is increased from 100 K to 400 K . Upon return to 100 K, the high leakage current is recovered.

400 K. These measurements are presented in Fig. 4b,c. After reaching 400 K, the measurement chamber was returned to 100 K and measurements were subsequently recorded. Surprisingly, we observed that below the threshold voltage of the transistor (V_{TH}), the leakage current decreases by a factor of 25× as temperature increases from 100 K to 400 K (Fig. 4c). Upon returning to 100 K the high leakage current state is recovered (red data point in Fig. 4c). The magnitude and temperature scaling of the diode leakage current is comparable to that of the off-state current of the transistor (Fig. 3) demonstrating that gate-leakage limits the achievable on-off ratio in these devices. The decrease in diode leakage current at higher temperature stands in stark contrast to the temperature scaling observed in all models considered by the authors that describe leakage in a metal-insulator-semiconductor diode. Fowler-Nordheim tunneling, trap-assisted tunneling, thermionic emission and Poole-Frenkel emission all show either a constant scaling of current with temperature, or an increase in current at higher temperatures [14], and thus cannot explain the decrease in leakage current observed as temperature increases.

C. AFM characterization

In order to investigate this anomalous temperature dependence further, a temperature-dependent AFM study was conducted. Subsequent to cryogenic electrical measurements, the Al_2O_3 passivation layer of the measured device was etched in a buffered HF solution. Non-contact mode AFM scans were performed across the edge of the graphene channel at temperatures of 30 °C and 70 °C using a Park Systems XE-100 AFM. These measurements are presented in Fig. 5. At 70 °C we observed a step height of 8.6 nm between the InAlN mesa and the graphene channel. The height difference between monolayer graphene and the underlying surface as measured by non-contact mode AFM will in general differ from the true height difference, due to variations in surface forces between the AFM tip and the graphene/substrate. Previous work has shown that AFM topography measurements of single layer graphene on various substrates give thicknesses ranging from 0.4 nm to 1.7 nm [15]. Though our measurements do not allow us to precisely estimate the step height, given that our measured thickness is significantly outside of this reported range, it can be safely assumed that polymer residue is also present in the measured device. Our AFM measurements do not however allow us to determine if the residue or the graphene is on top. Measurements of surface roughness show that graphene and InAlN surfaces have a comparable root-mean-squared surface roughness of 1.5 nm and 1.6 nm, respectively, indicating that any polymer residue present is evenly distributed.

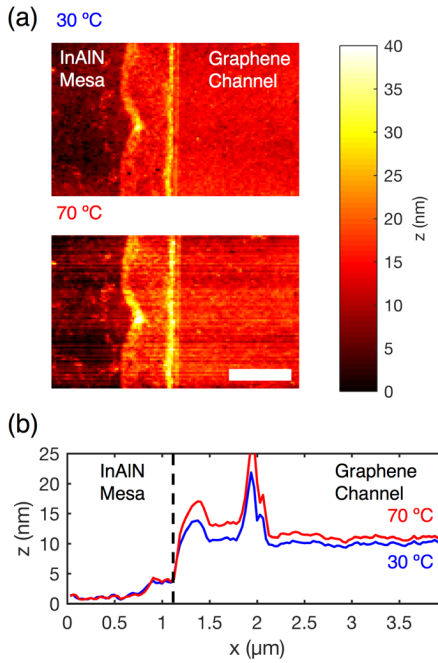

Fig. 5. Temperature-dependent AFM measurements of the fabricated device. Measurements were performed across the edge of the graphene channel on the InAlN mesa. (a) Topography measurements, scale bar represents 1 μm (b) Averaged line scans. An increase of the step height between graphene and the InAlN mesa from 8.6 to 10.1 nm is observed between 30 °C and 70 °C.

As temperature increased from 30 ºC to 70 ºC, we observed an increase in the height of the graphene channel relative to the InAlN surface from 8.6 nm to 10.1 nm (Fig. 5). It should again be noted that due to differing interatomic forces between the AFM tip and graphene/InAlN, these values do not represent the true thickness of the graphene/residue. Regardless, thermal expansion of a polymer layer can affect the coupling between graphene and the InAlN substrate either directly as an interfacial layer, or indirectly by changing the tension on the graphene if the polymer is on top. The observation of increased step height at higher temperatures indicates that the residue can modulate the coupling between the graphene and the substrate as a function of temperature, schematically illustrated in Fig. 1b. The following section will discuss how an increase in interfacial layer thickness can explain the observed anomalous current transport.

D. Anamolous leakage current mechanisms

Thermionic emission models can typically describe charge transport across the InAlN barrier in the forward-bias regime ($V_{Gr} > 0$ V) [16]. The band diagram associated with such a model is presented in Fig. 6c. At small reverse biases it has been shown that Poole-Frenkel emission dominates leakage current across the InAlN barrier (Fig. 6b) [16], [17]. At large reverse biases, this model cannot explain the temperature and field-dependencies, and a Fowler-Nordheim tunneling model must instead be used to describe device characteristics (Fig. 6a) [16], [17]. The dependency of current on electric-field for Fowler-Nordheim tunneling is given by [14]:

$$J \propto E^2 \exp\left[-\frac{4\sqrt{2m^*(q\phi_{FN})^3}}{3q\hbar}\cdot\frac{1}{E}\right] \quad (1)$$

where J is the current, E is the electric field, m^* is the effective electron mass in the InAlN layer, and ϕ_{FN} is the effective Fowler-Nordheim tunneling barrier. A linear-fit to a plot of $1/E$ vs. $\ln(J/E^2)$ can thus allow us to extract ϕ_{FN}. The electric field across the InAlN can be calculated from

$$E = q(n_b - n_{sh})/\epsilon - V_{Gr}/d \quad (2)$$

Where n_b is the bound charge due to the spontaneous polarization mismatch of InAlN/GaN, n_{sh} is the sheet density of the 2DEG at zero bias, ϵ is the dielectric constant of InAlN and d is the total thickness of the epitaxial stack. These parameters are given by theoretical estimates for n_b and n_{sh} (2.73×10^{13} cm^{-2} [18] and 2.25×10^{13} cm^{-2} [8], respectively) as well as $\epsilon = 10.1\epsilon_0$ [19]. Fig. 7a is a plot of $\ln(J_{diode}/E^2)$ vs. $1/E$ for the room-temperature measurements presented in Fig 4a. These data are well described by a Fowler-Nordheim model (dashed lines).

Using $m^* = 0.28m_e$ in InAlN [19], we calculated ϕ_{FN} for the measured devices. As shown in Fig. 7a, among different devices this value ranged from 0.71 eV to 0.93 eV, with an average of ϕ_{FN} = 0.84 eV. These barrier heights are significantly lower than the 2.2 eV barrier height predicted by Schottky-Mott theory, using ϕ_{Gr} = 4.6 eV [20] and

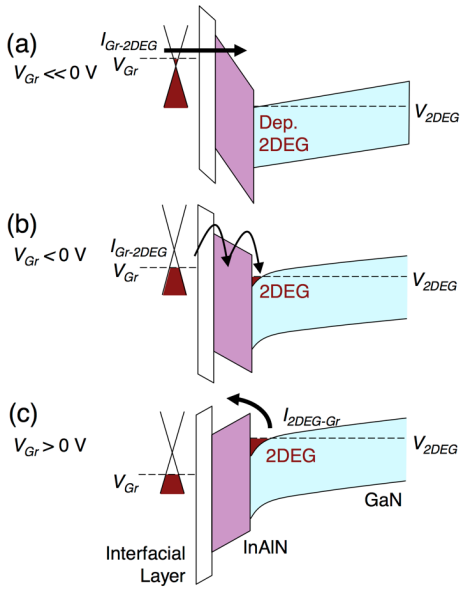

Fig. 6. Band diagram of fabricated device in (a) reverse bias, (b) no bias and (c) forward bias regimes. Effect of polymer residue is represented as a tunnel junction. At a given temperature this junction has a fixed width, however this width changes with temperature (Figure 1b). The relative magnitudes of current flowing from graphene to the 2DEG ($I_{Gr\text{-}2DEG}$) and the current flowing from the 2DEG to the graphene ($I_{2DEG\text{-}Gr}$) are indicated by the arrow size.

χ_{InAlN} = 2.4 eV [18], however they are similar to previous reports of Ni/InAlN junctions where an effective ϕ_{FN} ~0.7 eV was observed [17], significantly less than predicted by Schottky-Mott theory. This relatively low value can be explained by inhomogeneities in barrier height. Due to the exponential dependency of current on barrier height, if there are inhomogeneities present, then the smallest barrier heights in the distribution will dominate conduction [17].

The Fowler-Nordheim model further explains the saturation of leakage current below the threshold voltage of the transistor. Below V_{TH}, the voltage dropped across the InAlN layer is approximately constant, set by the spontaneous polarization difference of InAlN and GaN, resulting in a voltage-independent triangular tunneling potential seen by the tunneling electrons. Though this model explains the saturation of leakage current, it does not account for temperature-dependent phenomena. The standard Fowler-Nordheim model assumes all carriers that tunnel across the triangular barrier have the same characteristic energy, and as such the current is temperature independent [14]. A more detailed analysis of tunneling across a triangular barrier which considers integration over the full Fermi-Dirac distribution introduces a slight temperature dependency, however this analysis predicts increased leakage currents at higher temperatures [17]. Thus, this model cannot explain the anomalous decrease in leakage current we measured.

Other considered explanations for the anomalous leakage current include variations in contact resistance and sheet resistance over the measured temperature range, as well as barrier inhomogeneities. Changes in contact resistance are

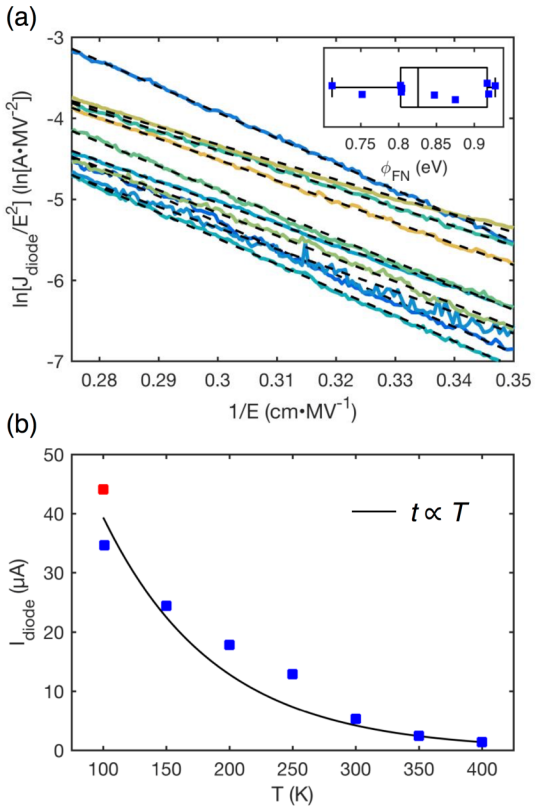

Fig. 7. (a) Fitting of Fowler-Nordheim tunneling parameters at room temperature. Main panel shows ln (J_{diode}/E^2) vs. $1/E$ in the voltage range -5.5 V $< V_{Gr} <$ -3.5 V. Inset shows Fowler-Nordheim barrier height extracted from the slope of linear fit. (b) Fitting of tunneling model described in text to temperature dependent data for V_{Gr} = -7 V.

excluded as an explanation due to the high on-state current of our diodes. Changes in 2DEG mobility are further excluded due to the sheet resistance only changing by a factor of 3.2× across the measured temperature range, as indicated by the on-state resistance of the transistor (Fig. 3), consistent with reports of decreased 2DEG mobility at higher temperatures [13]. Graphene and unintentionally doped GaN show similar small changes in mobility across the same temperature range [21], [22]. While emission models which include spatially inhomogeneous barrier heights can modify the dependence of leakage current on temperature [23], [24], to the authors knowledge there are no reports in the literature of a decrease in leakage current at increased temperatures due to barrier inhomogeneities.

Given the insufficiencies of these mechanisms for explaining the observed anomalous leakage current, we hypothesize that this dependency is due to the presence of an interfacial layer whose thickness is temperature dependent, illustrated schematically in Fig. 1b. It has previously been shown that modulating the width of polymer junctions can lead to large changes in tunneling current [25]. Assuming that the current must tunnel across a gap induced by process residue to reach the InAlN layer, the increase in thickness observed under AFM will lead to decreased tunneling at higher temperatures. Though it cannot be unambiguously determined if the residue is above or below the graphene, this mechanism can explain the anomalous temperature dependence of the reverse current of our structure, where leakage current increases at low temperatures.

The effect of the introduction of a second tunneling barrier whose thickness is temperature dependent is schematically illustrated in Fig. 1b. Such a barrier could describe the change in coupling between graphene and the InAlN substrate due to a residue layer which experiences thermal expansion/contraction. In presence of a rectangular tunneling barrier, the current is proportional to the tunneling probability across the interfacial layer, Γ:

$$J \propto \Gamma = \exp\left[-2t(T)\sqrt{\frac{2m^*q}{\hbar^2}\phi_B}\right] \quad (3)$$

Where $t(T)$ is the barrier thickness as a function of temperature, ϕ_B is the barrier height and m^* is the electron effective mass. This expression assumes that electrons tunnel with a characteristic energy. To first order this expression is field-independent. This approximation is valid because the interfacial layer is expected to be thin relative to the InAlN layer, and as such a small voltage should be dropped across it, relative to the height of the barrier. Because corrections to (3) are only weakly field-dependent, even in the presence of such a layer, the Fowler-Nordheim barrier height can still be extracted by measuring the scaling of current with field-strength. Thus, by postulating the existence of such a layer, we do not invalidate the earlier analysis of Fowler-Nordheim barrier heights.

We can find the change in barrier thickness between temperatures T_1 and T_2 needed to explain the data by noting that $J(T_1)/J(T_2) = \Gamma(T_1)/\Gamma(T_2)$. Rearranging (3) we find:

$$t(T_2) - t(T_1) = \frac{1}{2}\left(\frac{2m^*q}{\hbar^2}\phi_B\right)^{-\frac{1}{2}} \log[J(T_1)/J(T_2)] \quad (4)$$

Assuming ϕ_B is the work function of graphene (~4.6 eV [20]), and m^* is the free electron mass, we find that this model can reproduce the observed 25-fold increase in leakage current if $t(T = 400\text{ K}) - t(T = 100\text{ K}) \approx 0.15$ nm. This order of magnitude estimate verifies that a sub-nanometer change in interfacial layer thickness due to thermal expansion can explain the observed decrease in leakage current at higher temperatures. Though we are making a priori assumptions about the values of ϕ_B, and m^*, varying these parameters across reasonable values results in the same order of magnitude estimate for the change in tunneling gap needed to explain the observed data.

This sub-nanometer value is significantly less than the 1.5 nm change in thickness observed under AFM across a smaller temperature range. This is not a concern however, because the AFM measurements do not allow us to determine how much residue is above and below the graphene layer, thus they provide an upper bound on thickness changes. Assuming a linear coefficient of thermal expansion, the model proposed in (3) can be fit to the data in Fig. 4c. This fitted model is presented in Fig. 7b. We observe that this interfacial tunneling model can accurately represent the measured data.

IV. Conclusions

Measurements of current transport across the Gr/InAlN interface were performed. These measurements show that at room-temperature, in the reverse bias regime, current in our device is well described by a Fowler-Nordheim tunneling model with a barrier height, ϕ_{FN}, of ~ 0.8 eV. Temperature-dependent measurements, however, show that leakage current decreases as temperature is increased from 100 K to 400 K, in contrast to standard temperature scaling laws. We hypothesize that this anomalous transport is due to organic process-residue affecting the coupling between graphene and the InAlN substrate, as a function of temperature. Evidence for the presence of a residue layer is provided by Raman spectroscopy, which indicates the presence of disordered carbon. In addition, temperature-dependent AFM measurements demonstrate an increase in the step height between graphene and the InAlN substrate as temperature is increased. Order of magnitude estimates show that sub-nanometer changes in interfacial layer thickness can reproduce the observed current modulation. In addition to providing information on the electrical properties of the Gr/InAlN interface, this work demonstrates how engineering interfacial layers could allow for the controlled fabrication of devices with anomalous temperature dependencies. Such devices can be used for temperature compensation and sensing applications.

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References

[1] F. Giannazzo *et al.*, "Graphene integration with nitride semiconductors for high power and high frequency electronics," *Phys. status solidi*, vol. 214, no. 4, p. 1600460, Apr. 2017.

[2] A. Zubair *et al.*, "Hot electron transistor with van der Waals base-collector heterojunction and high-performance GaN emitter," *Nano Lett.*, vol. 17, no. 5, pp. 3089–3096, May 2017.

[3] G. Fisichella, G. Greco, F. Roccaforte, and F. Giannazzo, "Current transport in graphene/AlGaN/GaN vertical heterostructures probed at nanoscale," *Nanoscale*, vol. 6, no. 15, pp. 8671–8680, 2014.

[4] S. Tongay *et al.*, "Graphene/GaN Schottky diodes: Stability at elevated temperatures," *Appl. Phys. Lett.*, vol. 99, no. 10, p. 102102, Sep. 2011.

[5] A. Kumar, R. Kashid, A. Ghosh, V. Kumar, and R. Singh, "Enhanced thermionic emission and low 1/f noise in exfoliated graphene/GaN Schottky barrier diode," *ACS Appl. Mater. Interfaces*, vol. 8, no. 12, pp. 8213–8223, Mar. 2016.

[6] B. Pandit, T. H. Seo, B. D. Ryu, and J. Cho, "Current transport mechanism in graphene/AlGaN/GaN heterostructures with various Al mole fractions," *AIP Adv.*, vol. 6, no. 6, p. 065007, Jun. 2016.

[7] J. W. Suk *et al.*, "Enhancement of the electrical properties of graphene grown by chemical vapor deposition via controlling the effects of polymer residue," *Nano Lett.*, vol. 13, no. 4, pp. 1462–1467, 2013.

[8] C. A. Chapin, R. A. Miller, K. M. Dowling, R. Chen, and D. G. Senesky, "InAlN/GaN high electron mobility micro-pressure sensors for high-temperature environments," *Sensors Actuators, A Phys.*, vol. 263, pp. 216–223, 2017.

[9] M. Hou and D. G. Senesky, "Operation of ohmic Ti/Al/Pt/Au multilayer contacts to GaN at 600 °C in air," *Appl. Phys. Lett.*, vol. 105, no. 8, p. 081905, 2014.

[10] J. D. Wood *et al.*, "Annealing free, clean graphene transfer using alternative polymer scaffolds," *Nanotechnology*, vol. 26, no. 5, 2015.

[11] Y. Hao *et al.*, "Probing layer number and stacking order of few-layer graphene by Raman spectroscopy," *Small*, vol. 6, no. 2, pp. 195–200, 2010.

[12] Y. C. Lin, C. C. Lu, C. H. Yeh, C. Jin, K. Suenaga, and P. W. Chiu, "Graphene annealing: How clean can it be?," *Nano Lett.*, vol. 12, no. 1, pp. 414–419, 2012.

[13] J. Xie, X. Ni, M. Wu, J. H. Leach, Ü. Özgür, and H. Morkoç, "High electron mobility in nearly lattice-matched AlInN/AlN/GaN heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 91, no. 13, p. 132116, Sep. 2007.

[14] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2006.

[15] J. S. Cameron, D. S. Ashley, J. S. Andrew, G. S. Joseph, and T. G. Christopher, "Accurate thickness measurement of graphene," *Nanotechnology*, vol. 27, no. 12, p. 125704, 2016.

[16] S. Turuvekere, N. Karumuri, A. A. Rahman, A. Bhattacharya, A. Dasgupta, and N. Dasgupta, "Gate leakage mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and modeling," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3157–3165, 2013.

[17] S. Ganguly, A. Konar, Z. Hu, H. Xing, and D. Jena, "Polarization effects on gate leakage in InAlN/AlN/GaN high-electron- mobility transistors," *Appl. Phys. Lett.*, vol. 101, no. 25, 2012.

[18] J. Kuzmík, "Power electronics on InAlN/(In)GaN: Prospect for a record performance," *IEEE Electron Device Lett.*, vol. 22, no. 11, pp. 510–512, 2001.

[19] L. Lugani, M. A. Py, J. F. Carlin, and N. Grandjean, "Leakage mechanisms in InAlN based heterostructures," *J. Appl. Phys.*, vol. 115, no. 7, 2014.

[20] Y.-J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim, "Tuning the Graphene work function by electric field effect," *Nano Lett.*, vol. 9, no. 10, pp. 3430–3434, Oct. 2009.

[21] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, and M. S. Fuhrer, "Intrinsic and extrinsic performance limits of graphene devices on SiO2," *Nat. Nanotechnol.*, vol. 3, no. 4, pp. 206–209, Apr. 2008.

[22] W. Götz, N. M. Johnson, C. Chen, H. Liu, C. Kuo, and W. Imler, "Activation energies of Si donors in GaN," *Appl. Phys. Lett.*, vol. 68, no. 22, pp. 3144–3146, 1996.

[23] J. H. Werner and H. H. Güttler, "Barrier inhomogeneities at Schottky contacts," *J. Appl. Phys.*, vol. 69, no. 3, pp. 1522–1533, 1991.

[24] Y.-F. Lin *et al.*, "Barrier inhomogeneities at vertically stacked graphene-based heterostructures," *Nanoscale*, vol. 6, no. 2, pp. 795–799, 2014.

[25] F. Niroui *et al.*, "Tunneling nanoelectromechanical switches based on compressible molecular thin films," *ACS Nano*, vol. 9, no. 8, pp. 7886–7894, 2015.