Non-Intrusive Methodologies for Characterization of Bias Temperature Instability in SiC Power MOSFETs

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***Abstract*—The gate oxide reliability of SiC power MOSFETs remains a challenge, despite the improvements of the new generation power devices. The threshold voltage drift caused by Bias Temperature Instability (BTI) has been subject of different studies and methods have been proposed to evaluate the real magnitude of the threshold voltage shift. These methodologies usually focus on the characterization of the threshold voltage shift, rather than its implications to the operation or how the threshold voltage shift can be detected during the application. This paper presents two non-intrusive methodologies which can assess and determine the impact of BTI-induced. The proposed methodologies are able to capture the peak shift and subsequent recovery after stress removal**

***Index Terms*-- SiC MOSFETs, Gate Oxide Reliability, Bias Temperature Instability**

I. INTRODUCTION

Bias Temperature Instability (BTI) is a reliability concern for SiC MOSFETs [1]-[6] due to the higher interface and oxide trap density compared with Si MOSFETs. When the gate terminal is biased, charges are trapped, causing a shift of the threshold voltage (V_{TH}) which will have reliability implications. For example, uneven shift in the case of the parallel connected devices may have catastrophic consequences in the case of current imbalance [7] and increased on-state resistance due to positive V_{TH} shift may lead to increased power dissipation [1], [8]-[9]. Detecting the peak shift of V_{TH} in SiC MOSFETs is challenging, as the trapped charges are released when the gate stress bias is removed. This may lead to underestimating the true extent of the shift [4], [6], hence different methods have been evaluated in the literature, for example [1], [3], [10].

BTI-induced V_{TH} shifts also play a relevant role in power cycling of SiC MOSFETs [11], affecting the accuracy of the test and the junction temperature measurement [12]-[13]. Methods for power cycling SiC MOSFETs have to account for this peculiarity [11], [14]. This V_{TH} shift may also have an impact on the operation of the converter, hence methodologies for assessing the impact of BTI on the converter operation would be fundamental for accelerating the adoption of SiC MOSFETs in industry. Hence, the importance of developing non-intrusive methodologies which can be used for condition monitoring of the gate oxide as well as evaluating the impact of BTI in the application.

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II. THRESHOLD VOLTAGE INSTABILITY IN SIC MOSFETS AND CHARACTERIZATION

Characterizing the threshold voltage shift caused by gate bias stress has been the subject of multiple studies [1]-[6]. The main reliability concerns for SiC power MOSFETs are gate oxide breakdown and BTI [15]. Different performances under Time-Dependent Dielectric Breakdown (TDDB) were reported in [16], with SiC MOSFETs showing a reduced lifetime compared with their silicon counterparts. An improvement in the latest generations was also reported, with some devices showing an oxide breakdown performance under TDDB comparable to silicon devices [16]. Extrinsic failures (related to defects in the oxide and external contamination) are the main issue with SiC devices and breakdown reliability [17]. Manufactures have improved the reliability of their new devices and better performance under BTI has also been reported [16], [18]-[19]. BTI is a concern for SiC MOSFETs because of the higher interface and oxide trap density, together with the reduced band offsets between semiconductor and insulator [1].

Gate voltage bias causes the trapping of charges in the oxide and interface contributing to changes of the threshold voltage. A positive gate bias causes the trapping of negative charges resulting in a positive shift of V_{TH}, whereas a negative gate bias results in trapping of positive charges causing a negative shift of V_{TH}. The recovery of V_{TH} happens when the stress is removed and traps are released. A gate voltage of opposite polarity to the stress accelerates the recovery [20]. This recovery may have serious implications in the qualification of devices, if the true extent of the shift is not captured [6]. Additionally, in the case of SiC MOSFETs there is the phenomenon of V_{TH} hysteresis, resulting in the measurement of a different V_{TH} depending on the sweep direction of the measurement [1].

There has been considerable effort on the development of techniques suitable for capturing the peak shift and recovery of V_{TH} in SiC MOSFETs, as reviewed in [5], where considerations for correct characterization of V_{TH} shift and recovery in SiC MOSFETs are given. Depending on the measurement technique used, different values of V_{TH} can be determined [21], hence it will be important to define a measurement technique or JEDEC standard able to account for

the transient and recoverable effects of gate voltage stress in SiC MOSFETs [22]. This paper contributes to this research area, presenting the application of two novel methodologies.

III. Novel Methodologies For Threshold Voltage Shift Characterisation

A. Body Diode Method

One of the peculiarities of SiC MOSFETs is that reverse conduction of the body diode is affected by the applied gate voltage, requiring a negative gate voltage to fully close the channel [23]. This is shown in Fig. 1, for a set of planar and trench SiC MOSFETs and a planar Si MOSFET [24].

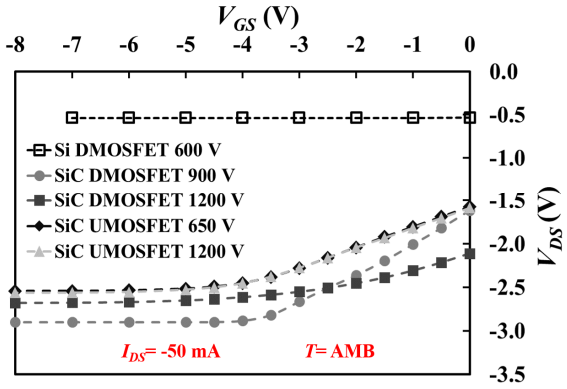

Figure 1. Impact of negative gate voltage on the third quadrant voltage for different Si and SiC MOSFETs[24]

As it can be observed, at V_{GS}=0, the measured V_{DS} voltage during reverse conduction is lower than the expected forward voltage of a SiC PN junction (around 2.7 V). This is caused by a more apparent body effect in SiC MOSFETs and partial channel conduction [23]-[25]. During reverse conduction, the parasitic PN junction is forward biased and, if V_{GS}=0, a positive potential appears at the p-body to n$^-$-SiC interface resulting in the conduction of current through the channel of the MOSFET due to the inversion of the channel [23].

An equivalent circuit is shown in Fig. 2, which shows that the reverse conduction of current can be explained using a current divider between the channel resistance R_{CH} and the parasitic body diode, with forward voltage V_f [24].

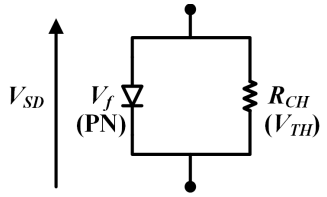

Figure 2. Current divider between the channel resistance and the parasitic body diode of a SiC MOSFET [24]

This partial conduction of current in the channel at V_{GS}=0 is the fundamental mechanism that enables the use of V_{SD} as cursor for BTI-induced V_{TH} shift characterization, as changes in V_{TH} will be reflected in variations of the measured forward voltage V_{SD} across the MOSFET.

A low sensing current is required to minimize the impact of self-heating which will affect the value of V_{SD} as it is temperature dependent [24] and it will be important to consider the possible effect of bipolar degradation on the measured voltage [26].

Summarizing, for a fixed temperature T and a low sensing current, the forward voltage of the body diode at V_{GS}=0 is a cursor of the threshold voltage. A relationship between V_{SD} and V_{TH} can be experimentally obtained using accelerated stress tests. Fig. 3 shows the results for a 650 V SiC trench MOSFET [27], where V_{SD} was measured at ambient temperature using a sensing current I_{SD} of 50 mA. The threshold voltage was obtained from the transfer characteristics of the SiC MOSFET, measured with a curve tracer Tektronix 371B. The normalized values are shown in Fig. 3(b). Full details of the characterization procedure and given in [24], [27].

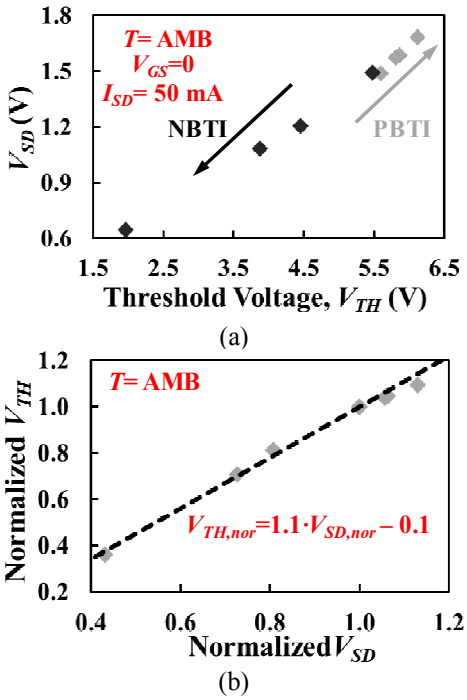

Figure 3. (a) Relationship between measured threshold voltage and body diode voltage (b) Normalized relationship. [27]

Using the circuit shown in Fig. 4, similar to the use of V_{SD} as temperature sensor, the calibration in Fig. 3 can be used for assessing V_{TH} shift of the device under test (DUT) using the relationship given by (1).

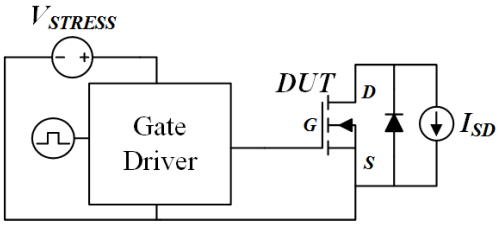

Figure 4. Schematic of the circuit for threshold voltage instability evaluation using the body diode voltage [24]

$$V_{TH,norm} = 1.1 V_{SD,norm} - 0.1 \quad (1)$$

Fig. 5 shows the results of applying the method to the SiC trench MOSFET, for evaluating the impact of a positive stress of 20 V and 10 s duration. Before the stress, V_{GS}=0 V and the current I_{SD} flows through the parallel combination of the body diode and the channel resistance. The measured V_{SD} voltage is around 1.5 V and the pre-stress V_{TH} can be identified.

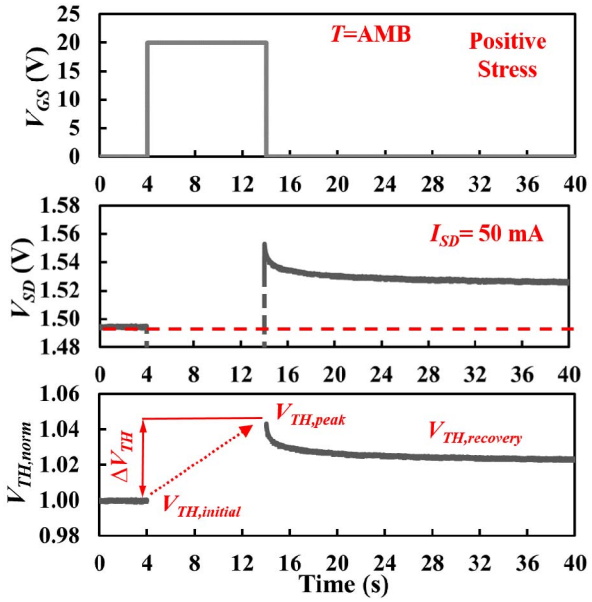

Figure 5. Gate voltage, body diode voltage and normalized threshold voltage for positive gate stress [27]

When the stress is applied (V_{GS}= 20 V) the device turns ON. The current flows through the channel of the MOSFET and the measured voltage is low (V_{SD}=I_{SD}*R_{ON}). At the instant when the stress finishes, the gate voltage applied to the device is 0 V and the current flows again through the parallel combination of the body diode and channel resistance. The positive gate stress caused an upwards shift of V_{TH}, which is reflected in an increase of the measured V_{SD}, as more current circulates through the body diode. After the peak shift, the threshold voltage starts the recovery phase and V_{SD} decreases, as more current starts to circulate through the channel. Fig. 5 described the operation of the method for a positive gate stress, but it can also be used for negative gate stresses [24], as shown in Fig. 6.

In this case, when the stress is applied (V_{GS}=-26 V), the channel is fully closed and the current flows through the body diode only. The measured voltage increases to the expected value of a SiC PN junction. During the stress sequence, as the voltage is high, there may be a slight self-heating of the device. Hence, it is important to select an appropriate value for the sensing current. When the stress finishes, V_{GS}=0 V and the current flows through the parallel combination of the body diode and channel resistance. The negative shift of V_{TH} causes more current to flow through the channel, thereby causing the initial dip of V_{SD}. After the stress, the recovery of V_{TH} is reflected in an increase of V_{SD} with time.

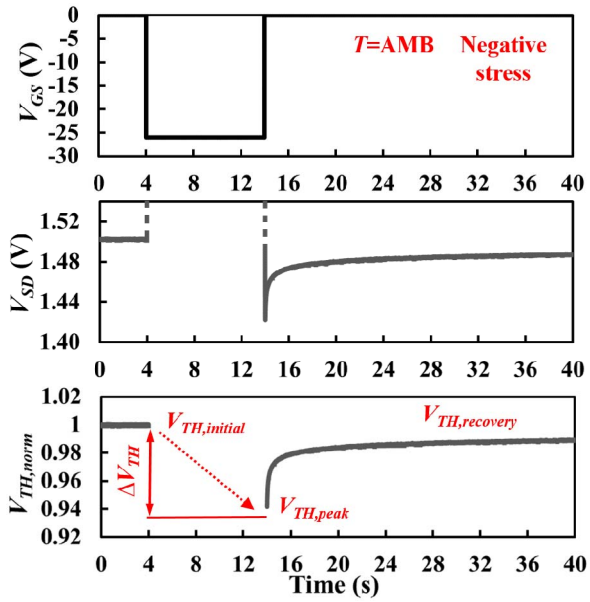

Figure 6. Gate voltage, body diode voltage and normalized threshold voltage for negative gate stress [27]

B. *Shoot-through Current Method*

The shoot-through current caused by parasitic turn-ON of the complementary device in a converter leg (also called crosstalk) is affected by the threshold voltage value [28]-[29]. Hence, this current can be used as BTI cursor. The shoot-through current caused by parasitic turn-ON can be measured using the test circuit shown in Fig. 7. It consists in a half-bridge leg, where the bottom side device, which is the device under test, is connected in parallel with a load resistor R_{LOAD}. The gate driver boards used have the functionality of changing the gate resistors ($R_{G\text{-}TOP}$ and $R_{G\text{-}BOT}$), which is fundamental for the improving the effectivity of this method.

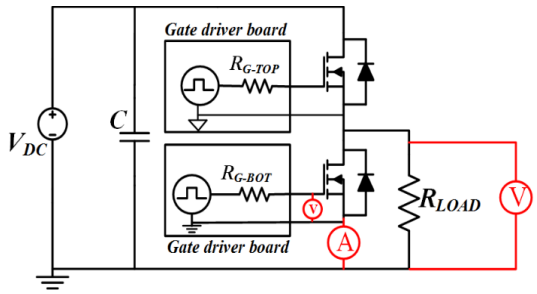

Figure 7. Circuit for evaluation of threshold voltage instability using parasitic turn-ON (Crosstalk) [28]

Analyzing the circuit in Fig. 7, if both devices are in the OFF state, all the DC link voltage is blocked by the top side device, as the value of R_{LOAD} (500 kΩ) is lower than the resistance in the OFF-state of the transistors in the leg. When the top side device is switched (at a switching rate controlled by the parasitic capacitances of the device and the gate resistance $R_{G\text{-}TOP}$), the voltage is transferred to the bottom side device at a switching rate dV_{DS}/dt. Due to the Miller effect, this voltage switching rate couples with the low side device C_{GD} capacitance and a current of value $C_{GD}{\cdot}dV_{DS}/dt$ flows

through the bottom side gate resistance $R_{G\text{-}BOT,}$ causing a parasitic gate voltage [29], which may turn-ON the bottom device if this voltage is greater than its threshold voltage. The transients are shown in Fig. 8, for a DC link voltage V_{DC} of 400 V and a leg formed by two 1200 V planar SiC MOSFETs from Littelfuse. Fig. 8 shows the drain-source voltage V_{DS} across the bottom side device, the parasitic gate voltage V_{GS} of the bottom side device and the drain-source current I_{DS} through the bottom side device. The top side device is switched at the recommended gate voltage of 18 V using a gate resistance $R_{G\text{-}TOP}$=33 Ω, while the bottom side device is kept OFF with V_{GS}=0 V. Two bottom side gate resistors were evaluated: $R_{G\text{-}BOT}$=10 Ω and $R_{G\text{-}BOT}$=220 Ω. Both SiC MOSFETs in the leg are the same.

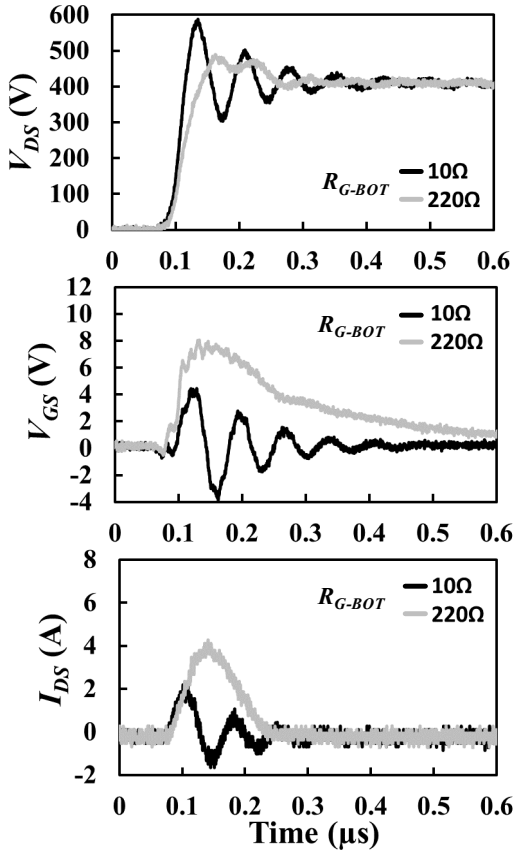

Figure 8. Impact of gate resistor combination on parasitic turn-ON. SiC Planar MOSFET. Bottom device: Drain-source voltage, Gate-source voltage and Drain-source current. Ambient temperature

In order to verify the impact of BTI-induced threshold voltage shifts in the parasitic turn-ON current, an initial accelerated stress test was performed, using a half bridge comprised of two 650 V trench SiC MOSFETs from Rohm [28]. The bottom side SiC MOSFET was subjected to a two stage gate stress, as follows: a first stage of 1 hour at V_{GS}=-35 V and 150°C followed by a 16 hour relaxation phase at V_{GS}=0 V and ambient temperature followed by a second stage of 1 hour at V_{GS}=-38 V and 150 °C followed by a 16 hour relaxation phase at V_{GS}=0 V. These highly accelerated stress tests, beyond the recommended voltages on the datasheet, were selected to have a more permanent V_{TH} shift for characterization, which does not recover after stress removal.

The shoot-through current was characterized before stress and after each relaxation phase. The top side device was switched using a gate resistance $R_{G\text{-}TOP}$=33 Ω and V_{GS} =18 V and the bottom side device was kept OFF with V_{GS}=0 V. Two bottom side gate resistors were evaluated: $R_{G\text{-}BOT}$=10 Ω and $R_{G\text{-}BOT}$=68 Ω. The results are shown in Fig. 9, measured at ambient temperature and a DC link voltage of 400 V.

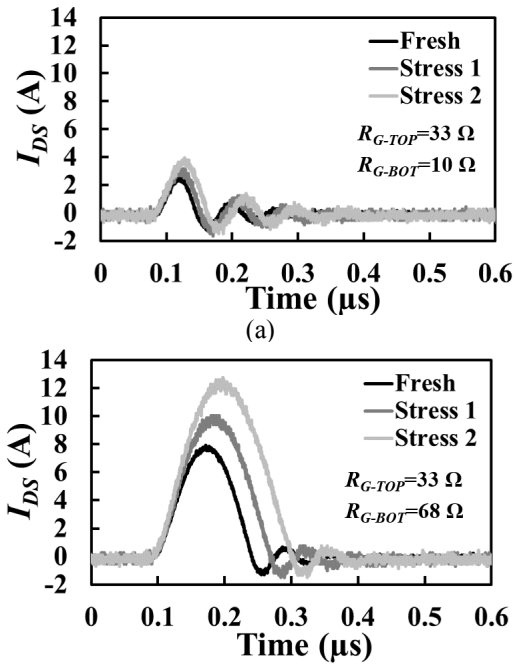

Figure 9. Impact of accelerated negative gate stresses on the measured shoot-through current. SiC trench MOSFET.
(a) $R_{G\text{-}TOP}$=33 Ω , $R_{G\text{-}BOT}$=10 Ω (b) $R_{G\text{-}TOP}$=33 Ω , $R_{G\text{-}BOT}$=68 Ω

Comparing Fig. 8 and Fig. 9, both devices are differently affected by cross-talk. The susceptibility to parasitic turn-ON of the evaluated SiC MOSFET will be fundamental for the effectivity of this methodology, together with the optimal combination of gate resistors, as the results in Fig. 8 indicate. It is recommended to switch the top side device with a low gate resistance $R_{G\text{-}TOP}$ and have a high gate resistance $R_{G\text{-}BOT}$ in the low side device. This will be paramount for obtaining the maximum sensitivity of the shoot-through current and characterize the impact of BTI-induced threshold voltage shifts.

It is also important to mention that in real operation the objective is minimizing the phenomenon of cross-talk. Different methods have been used, including the use of a large resistor for turn-ON and small resistor for turn-OFF or turning-OFF the device with a negative gate voltage [29]. There is plenty of academic research activity in gate drivers for suppression of cross-talk, like [30]-[32].

The highly accelerated stress test results in Fig. 9 were performed using a high negative gate voltage followed by a long recovery at V_{GS}=0, which may be not representative of the real shift in the application. A stress-characterization sequence capable of stressing the device and characterizing

the impact of the V_{TH} shift on the shoot-through current was presented in [28] and it is shown in Fig. 10 for a positive gate stress.

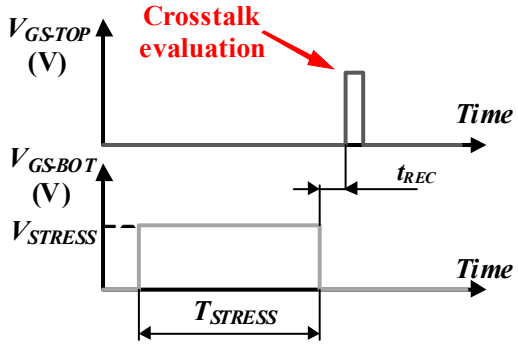

Figure 10. Test sequence for characterization of threshold voltage instability using crosstalk currents

It consists in applying a stress pulse to the bottom device of value V_{STRESS} and duration T_{STRESS}, followed by a short pulse applied to the top device while the bottom side device is at V_{GS}=0. The pulse is applied after a time t_{REC}, which can be in the range of a few hundreds of microseconds to several seconds. The pulse applied to the top device will cause the parasitic turn-ON of the bottom side device, as shown previously, hence the impact of the V_{TH} shift in the shoot-through current can be characterized as a function of the recovery time after stress.

Fig. 11 shows the results for a 650 V SiC trench MOSFET from Rohm and a 20 V gate stress of duration 10 s. The shoot-through current was captured at different recovery times, from 500 µs to 10 s. It is important to mention that in order to avoid the self-heating of the SiC MOSFET due to repetitive semi-short-circuits, a stress-characterization sequence was used for each recovery time value, allowing a time of 180 s between measurements. These measurements were done using the circuit in Fig. 7, using a DC link voltage of 400 V and a gate resistor combination R_{G-TOP}=33 Ω - R_{G-BOT}=68 Ω.

The measurements in Fig. 11 show that the positive stress causes a reduction of the measured shoot-through current, as result of the positive shift of V_{TH}. For a recovery time after

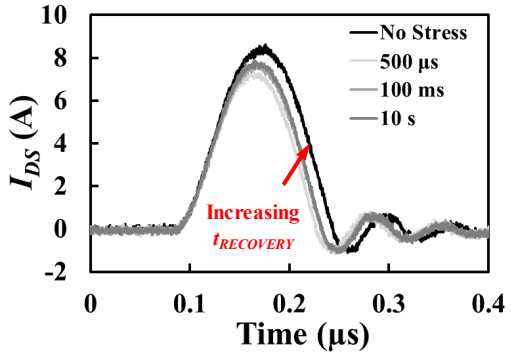

Figure 11. SiC Trench MOSFET. Positive gate stress 20 V/ 10 s. Ambient temperature. Impact of stress recovery on shoot-through current

stress of 500 µs, the peak shoot-through current reduces to 7.3 A, compared with 8.6 A for the no stress measurement. As the recovery time increases, the threshold voltage reduces to its pre-stress value, thereby resulting in an increase of the shoot-through current with recovery time. This is clearly shown in Fig. 12, where the shoot-trough current and charge are plotted as a function of the recovery time.

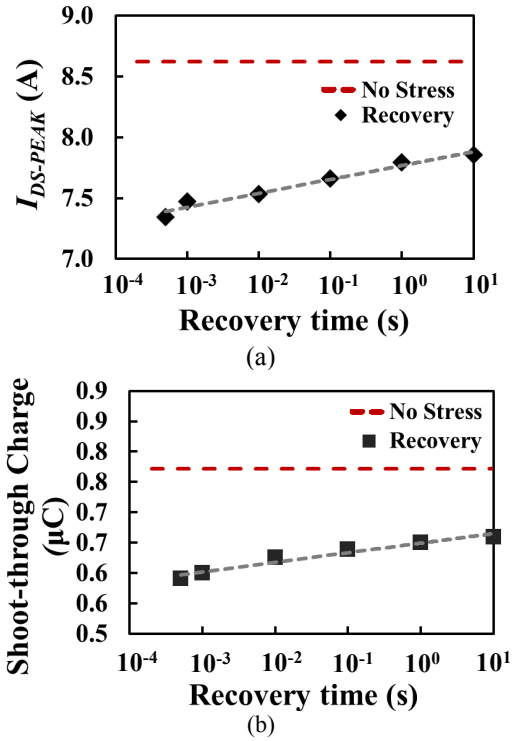

Figure 12. SiC Trench MOSFET. Positive gate stress 20 V/ 10 s. Ambient temperature. (a) Shoot-through peak current and (b) shoot-through charge as function of recovery time

Measuring variables like the peak shoot-though current in a noisy environment may results in measurement inaccuracies due to the resolution of the current probes and measurement noise. The use of the shoot-through charge shows a much better immunity to measurement issues, as can be observed in Fig. 12.

The main benefit of this method is that, rather than characterizing the V_{TH} shift only, it allows to evaluate the impact of V_{TH} shifts on the operation of the leg of a converter. This can be fundamental for understanding the driving limitations of SiC MOSFETs and their implications

IV. Characterization Results

A. *Body Diode Method Results*

The initial test results for the body diode method presented in section III show the initial V_{TH} shift and for a 650 V SiC trench MOSFET, which was calibrated in [27]. In order to evaluate a different device, like a 900 V SiC planar MOSFET, the use of this method requires the calibration of the relationship between V_{SD} and V_{TH} for the selected sensing current at the temperature of evaluation. Fig. 13 shows the

calibration results for a 900 V planar SiC MOSFET from Cree/Wolfspeed [24].

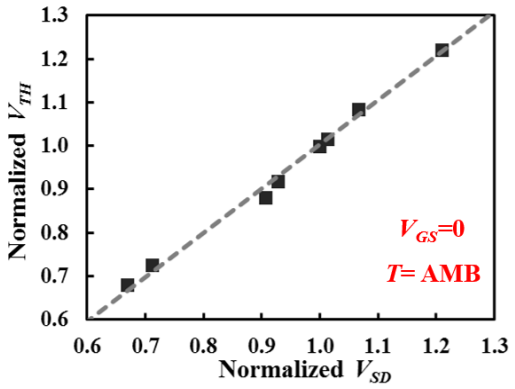

Figure 13. 900 V SiC Planar MOSFET. Relationship between normalized threshold voltage and body diode voltage I_{SD}=50 mA [24]

The authors would like to point out that similar to the use of the collector-emitter voltage V_{CE} of an IGBT or the forward voltage V_F of a PN junction as a temperature sensitive electrical parameter [33] calibration is required. From Fig. 12, the calibration relationship for the evaluated SiC planar MOSFET is given by (2).

$$V_{TH,norm} = 1.02 V_{SD,norm} - 0.02 \quad (2)$$

One of the main benefits of this method is that it allows to characterize the recovery of the threshold voltage after stress in a non-intrusive way and capture the recovery time transients of the captured traps.

The evaluated SiC planar and SiC trench devices were subjected to the same positive gate stress of 20 V during 10 s at ambient temperature. The recovery transients captured using the body diode method for both devices are shown in Fig. 14. For this test, the results show that the SiC planar has experienced a greater shift. Analyzing the recovery transients, the planar device has a faster recovery transient, meaning that the trapped charges have faster time constants.

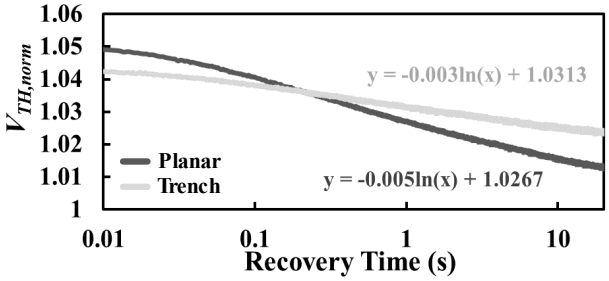

Figure 14. Normalized threshold voltage recovery after postive stress. Planar and trench SiC MOSFETs

It is also important to evaluate the impact of the stress voltage level and longer stresses. It can reveal interesting insights of the devices and help to understand the limitations in gate voltage, including both positive and negative gate voltages. To that end the SiC planar devices (4 devices in total) were subjected to the following stress at ambient temperature:

- Device 1: 15 minutes, V_{STRESS}= + 22 V
- Device 2: 15 minutes, V_{STRESS}= +32 V
- Device 3: 15 minutes, V_{STRESS}= -16 V
- Device 4: 15 minutes, V_{STRESS}= -26 V

The recovery transients are shown in Fig. 15(a) for the positive gate stresses and Fig. 15(b) for the negative gate stresses. The results are shown in Fig. 15 show that the magnitude of the V_{TH} shift is directly proportional to the gate stress voltage. This is especially noticeable for the negative stresses. An interesting observation is the change of slope during the recovery phase, which can be attributed to a different amount of traps with short/long time constants.

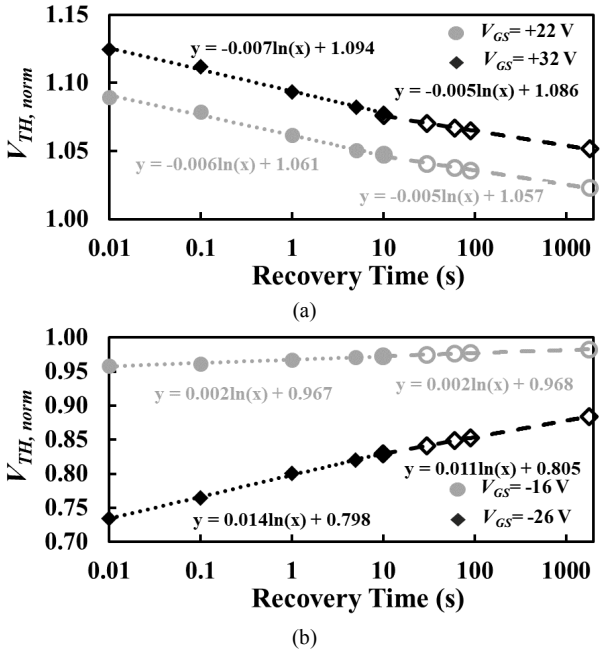

Figure 15. Normalized V_{TH} as function of recovery time. SiC Planar MOSFET (a) Positive stress – 15 minutes (b) Negative stress- 15 minutes

As introduced in [34], an interesting feature of the body diode method is that it allows the study of pulsed stresses. Tests have been performed using different devices at different gate voltage stresses. Gate switching induced V_{TH} shifts appear to have an influence on the lifetime of the gate oxide [35] and methods which can be used for its evaluation will be required.

First, a 900 V SiC planar device was subjected to a low voltage pulsed stress consisting of 40 pulses with 2 s at V_{GS}=+6 V and 2 s at V_{GS}=0 V. The results are shown in Fig. 16. An initial rise of V_{SD} is observed for the first pulse stress, follow by a slight cumulative shift. The partial recovery during the 2 s at V_{GS}=0 V is perceptible and the peak shift of V_{SD} is 3.4% after the complete stress sequence. After a recovery time of 20 seconds the shift of V_{SD} is only 0.9%.

The same device was subjected to a new pulsed stress consisting of 40 pulses with 2 s at V_{GS} = +22 V and 2 s at V_{GS}= 0 V. The results in Fig. 17 indicate a larger peak shift (7.4%), which recovers to a shift of 2% after 20 seconds recovery. The initial peak shift is more noticeable for the higher gate voltage stress. This agrees with the literature, which reports an increased V_{TH} shift with stress voltage level [2], [19], [20]

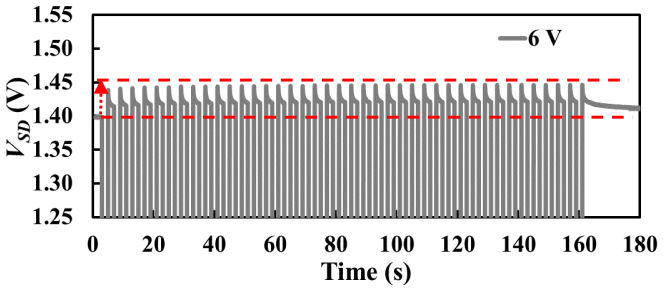

Figure 16. 900 V SiC Planar MOSFET. Measured V_{SD} during pulsed gate stress. 40 pulses, 2 s/+6V and 2 s/0 V. T= AMB. I_{SD}=50 mA

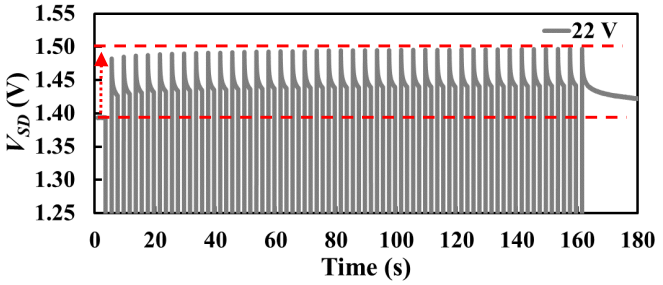

Figure 17. 900 V SiC Planar MOSFET. Measured V_{SD} during pulsed gate stress. 40 pulses, 2 s/+22V and 2 s/0 V. T= AMB. I_{SD}=50 mA

A significant observation already reported in [34] is the existence of the phenomenon of dip-and-rebound at high gate voltage stresses (35 V) in the evaluated planar SiC MOSFET. This phenomenon was also observed for Si MOSFETs [36], at gate stress levels of 65 V.

Following the same stress procedure, a 40-pulse stress consisting in 2 s at V_{GS} = +35 V and 2 s at V_{GS}= 0 V was applied to the planar SiC MOSFET. The results are shown in Fig. 18, where the phenomenon of dip-and-rebound is clearly observed. This indicates a reduction of V_{TH} in the initial stages of the stress, followed by the expected increase of V_{SD} for a positive gate bias stress. The reduction of V_{SD} when V_{GS}=0 V during both stages of the stress sequence indicates that V_{TH}

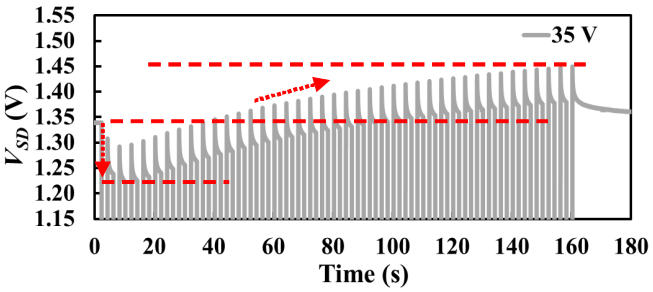

Figure 18. 900 V SiC Planar MOSFET. Measured V_{SD} during pulsed gate stress. 40 pulses, 2 s/+35V and 2 s/0 V. T= AMB. I_{SD}=50 mA

reduces after the gate bias removal. The dip-and-rebound, as explained in [36], is caused by the different contribution of the interface trapped charges, which cause an increase of V_{TH}, and the oxide trapped charges, which reduce V_{TH}. This stress level is higher than the recommended gate voltage and may not represent the real shift in real application, however these type of accelerated stress tests can be relevant for the evaluation of the robustness and reliability of the gate oxide.

The stress tests shown in Fig. 16 to Fig 18 were performed at ambient temperature (22 °C). It is important to evaluate the role of temperature in the gate stress and resultant V_{TH} shift. To that end, the 40-pulse stress sequence of V_{GS} = +35 V for 2 s and V_{GS}= 0 V for 2 s was repeated at a case temperature of 150°C using a non-stressed device. The results are shown in Fig. 19, where it is observed that V_{SD} has reduced to 1.1 V at a temperature of 150°C due to its temperature sensitivity.

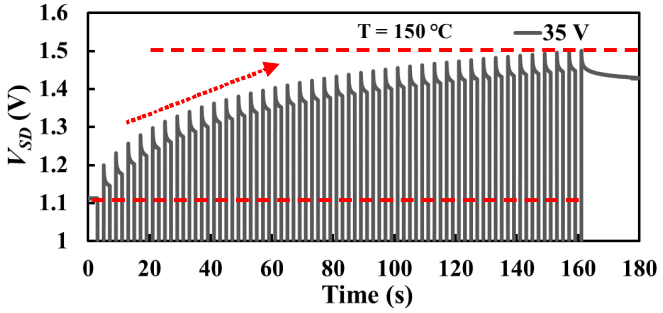

Figure 19. 900 V SiC Planar MOSFET. Measured V_{SD} during pulsed gate stress. 40 pulses, 2 s/+35V and 2 s/0 V. T= 150 °C. I_{SD}=50 mA

The results for the stress at high temperature presented in Fig. 19 indicate a fast increase of V_{SD} with time, increasing from 1.1 V to 1.5 V, namely an increase of around 36%, indicating a high dependence of the threshold voltage shift with temperature. The 40-pulse stress sequence of V_{GS}= +35 V for 2 s and V_{GS}= 0 V for 2 s at ambient temperature was also applied to a 1200 V vintage SiC MOSFET from the same vendor. The results are presented in Fig. 20 and show that the dip-and-rebound is not present and the observed shift of V_{SD} is smaller.

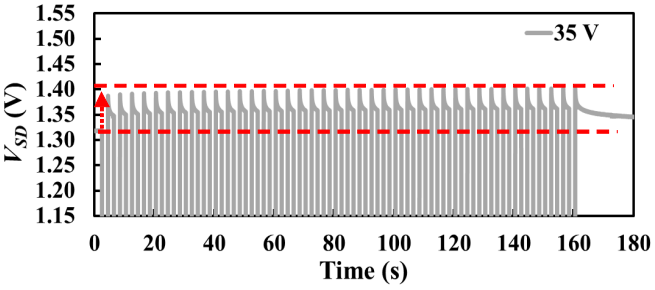

Figure 20. Vintage 1200 V SiC Planar MOSFET. Measured V_{SD} during pulsed gate stress. 40 pulses, 2 s/+35V and 2 s/0 V. T= AMB
I_{SD}=50 mA

Unfortunately, the last two tests highlight two of the principal limitations of the body diode method. First, the calibration of the relationship between V_{SD} and V_{TH} must be obtained for devices from different generations and vendors. Second, as V_{SD} and V_{TH} are temperature dependent, the

relationship between V_{SD} and V_{TH} has to be obtained for the temperatures of interest.

Nevertheless, one of the benefits of the body diode method is that it could be used during power cycling, to assess the impact of the gate stress on the threshold voltage during the power cycling test. The calibrated V_{SD} at V_{GS}=-5 V (fully closed channel) can be used for measuring the junction temperature [11], [14] while the calibrated V_{SD} as function of V_{TH} can be used as indicator of oxide degradation.

B. Shoot-through Current Method Results

Despite the fact that there are plenty of studies on quantification of V_{TH} shift, recovery and implications of the measurement technique [1]-[6], [15]-[17], [19]-[21], the studies on the implications of V_{TH} shift on the operation of the device are scarce in the literature, for example [2], [11] and [37]. The shoot-through current method has the main advantage of showing the impact of V_{TH} shift in the operation of the converter and its implications.

As introduced in section III.B, its effectiveness depends on the susceptibility of the device to parasitic turn-ON and the gate resistor combination used for augmenting the shoot-through current. Two 1200 V SiC planar MOSFETs from two different vendors were subjected to the same positive stress, namely 20 V during 10 s at ambient temperature. The results are shown in Fig. 21 for a 1200 V planar from ST and Fig. 22 for a 1200 V SiC planar from Littelfuse. The current ratings are 16 A for the ST device and 18 A for the Littelfuse device, both at 100 °C. The DC link voltage was 400 V and the resistor combination was $R_{G\text{-}TOP}$=33 Ω - $R_{G\text{-}BOT}$=220 Ω in both cases.

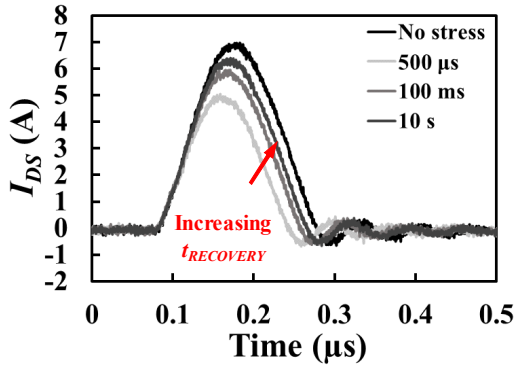

Figure 21. Shoot-through current after positive gate stress measured at different recovery times (20 V/10 s at ambient temperture). ST SiC MOSFET

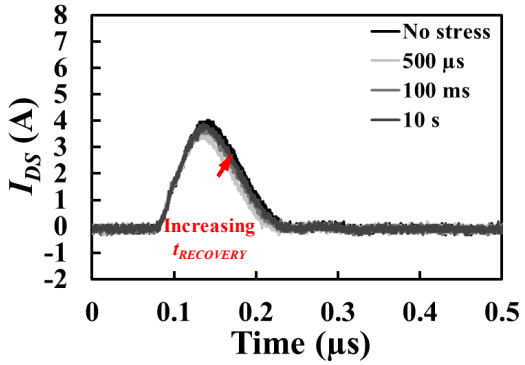

Figure 22. Shoot-through current after positive gate stress measured at different recovery times (20 V/10 s at ambient temperture). Littelfuse SiC MOSFET

The shoot-through current was measured at different recovery times, from 500 µs to 10 s, as described in III.B. In the case of the SiC MOSFET from Littelfuse, measured 500 µs after stress removal, the peak shoot-through reduces from 4.02 to 3.56 A (~ -11%), whereas in the case of the SiC MOSFET from ST, the peak shoot-through current reduces from 6.97 to 5.04 A (~ -28%). Evaluating the shoot-through charge, there is a reduction of -21.8% for the Littelfuse MOSFET and -40.3% for the ST MOSFET.

By comparing Fig. 21 and Fig. 22, it is clear that the devices have completely different susceptibility to parasitic turn-ON, thereby the effectiveness of this technique for assessing the impact of V_{TH} shifts may be affected in the case of low susceptibility. Both devices show a reduction of shoot-through current due to positive gate stress, however the sensitivity is reduced for the device in Fig. 22. This may be caused by a reduced susceptibility to parasitic turn-ON or by a better gate oxide reliability. The ratio of the parasitic capacitances of the MOSFET plays a fundamental role on the susceptibility to parasitic turn-ON, as defined in [38]. The authors suggest that this method is more suitable for devices which are more sensitive to parasitic turn-ON.

The shoot-through charge as function of recovery time is shown in Fig. 23 for both SiC MOSFETs. From the results, it is clearly observed than the shoot-through charge recovers following a logarithmic recovery, with the slope indicating the

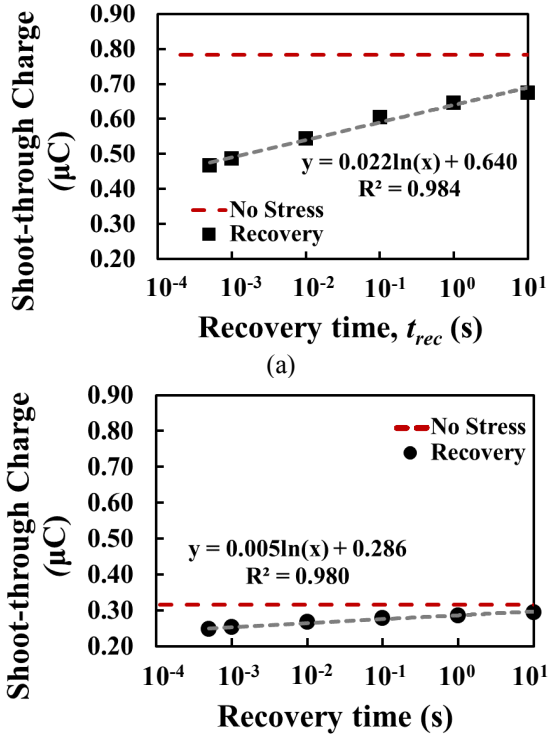

Figure 23. Shoot-through charge after as function of recovery time positive gate stress (20 V/10 s at ambient temperture). (a) ST SiC MOSFET (b) Littelfuse SiC MOSFET

time constant of the trapped charges. Comparing both devices, for the same stress at ambient temperature, after 10 s recovery the shoot-through charge recovers to a 93.2% of the pre-stress value for the Littelfuse SiC MOSFET and 91.8% for the ST SiC MOSFET.

This method also allows to easily evaluate the impact of temperature on the stress and recovery, by just adjusting the temperature of the DUT. The same 20 V/10 s stress and characterization sequence was repeated at a case temperature of 150°C for the Littelfuse SiC MOSFET. The stress was performed allowing long recovery time (72 hours) after the characterization at ambient temperature. The results are presented in Fig. 24, including the shoot-through current and charge. Analyzing the impact of temperature on the parasitic turn ON, the pre-stress shoot-through current increases with temperature, from 4.02 A at ambient temperature to 5.24 A at 150°C, in agreement with [29]. The shoot-through charge does also increase, from 0.316 to 0.540 µC.

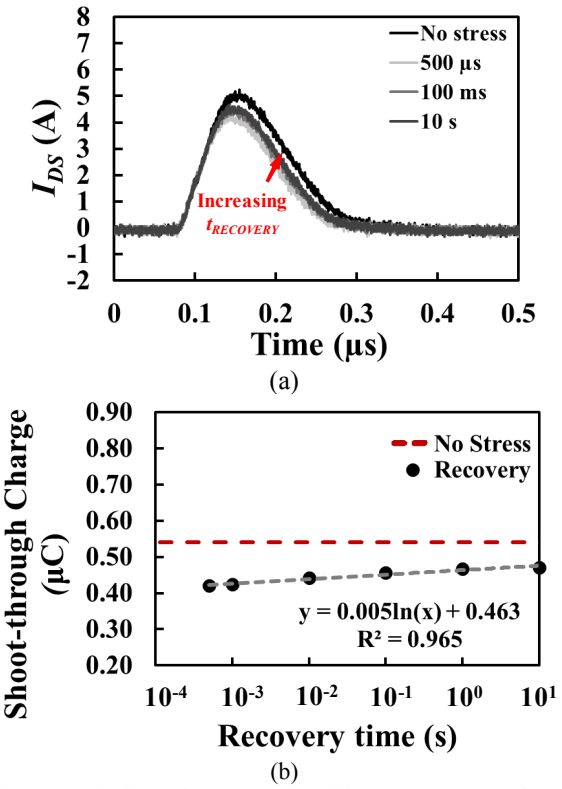

Figure 24. Littelfuse SiC MOSFET. Positive gate stress (20 V/10 s at 150°C) (a) Shoot-through current measured at different recovery times, (b) Shoot-through charge after as function of recovery time

Analyzing the impact of the stress at 150°C, the peak shoot-through current and charge measured 500 µs after stress removal are 4.41 A and 0.421 µC respectively The reduction of the shoot-through charge, measured 500 µs after stress removal, is approximately the same at ambient and 150°C (78.2% and 77.9% of the pre-stress shoot-through charge). However, the recovery is clearly affected by temperature, as the results in Fig. 24(b) indicate. After 10 s recovery, at 150°C the shoot-trough charge returns to only 87% of the pre-stress value.

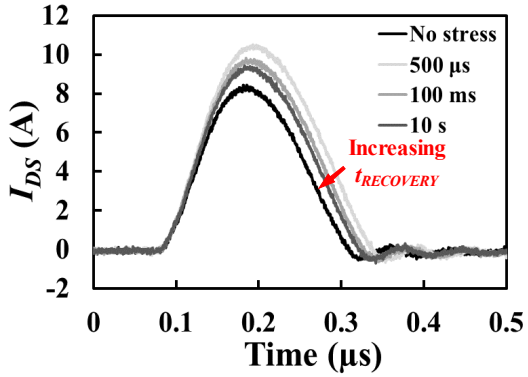

Figure 25 Shoot-through current after negative gate stress measured at different recovery times (-26 V/10 s at ambient temperture). ST SiC MOSFET

These are just some initial studies that show that the shoot-through method can be a highly valuable tool for evaluating and understanding the impact of BTI on the application. Furthermore, other analysis can include the impact of the stress duration, evaluation of longer recovery times or negative gate stresses. Preliminary results for negative gate stresses were already presented in [28], resulting in an increase of shoot-through current, as shown in Fig. 25 for a gate stress voltage of -26 V. The evaluation of long-term negative stresses and its impact on the application at voltages used in real operation, namely -5 V, can be highly relevant and this method allows its study.

V. Conclusions

This paper presented the application of two novel methodologies for characterization of BTI in SiC MOSFETs.

The body diode methodology is based on the impact of the threshold voltage shift on the forward voltage V_{SD} of the body diode when the gate-source voltage is 0 V. It enabled the capture of the peak shift of V_{TH} and recovery after stress removal. It is possible to evaluate both positive and negative stresses and the impact of gate pulsed stresses. Its application at high voltage stresses revealed the dip-and-rebound phenomenon in one of the evaluated devices. The use of V_{SD} as V_{TH} cursor requires calibration before its application and as it is affected by temperature it will be only valid at the calibration temperature. This method could be easily implemented during power cycling of SiC MOSFETs for assessing V_{TH} shifts during the test.

The shoot-through current method is based on the impact of the threshold voltage shift on the shoot-through current. A test methodology has been developed and it is possible to capture the impact of V_{TH} shift on a converter leg. It is applicable for both positive and negative stresses. It has been possible to capture the recovery of V_{TH} after stress removal in the range of hundreds of µs. The impact of recovery time and temperature can be characterized.

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