Characterizing BTI and HCD in 1.2V 65nm CMOS Oscillators made from Combinational Standard Cells and Processor Logic Paths

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***Abstract*—Bias Temperature Instability (BTI) and Hot-Carrier Degradation (HCD) are key aging mechanisms, frequently studied with transistor measurements or inverter-based (INV) Ring Oscillators (RO) measurements. However, large-scale digital circuits are typically manufactured with standard cells (such as logic gates). In a reliability simulation flow (e.g., SPICE-based standard cell characterization with degraded transistors), many assumptions about the standard cells have to be made (such as load capacitance, signal slews, uncertainty in aging models, etc.) and can lead to high simulation uncertainty. In this work, we propose to verify this standard cell characterization with standard cell oscillator measurements in silicon. For this purpose, we present the following novel contributions: 1) The first work with BTI and HCD measurements of heterogeneous oscillators (multiple different cell types in one RO) based on logic paths extracted from processors. 2) The first work exploring the impact of BTI and HCD on oscillators containing combinational standard cells, i.e. single cells incorporating multiple logic gates (such as And-Or-Inverter (AOI) cells and Or-And-Inverter (OAI)) and cells performing complex actions such as full-adders.**

***Index Terms*—Aging, BTI, Bias Temperature Instability, Degradation, HCD, HCI, Hot-Carrier, Oscillator, Ring Oscillator, Measurement**

I. Introduction

Bias Temperature Instability (BTI) and Hot-Carrier Degradation (HCD) are key aging mechanisms, frequently studied in both simulations and measurements. However, most of these measurements are transistor measurements or inverter-based (INV) Ring Oscillators (RO).

A. Aging in Standard Cells

Digital circuits such as processors and micro-controllers are typically manufactured with standard cells (i.e., logic gates, sequential gates, etc.). In order to estimate aging in these large-scale digital circuits, various approaches are used. Typically, industry employs characterizing the standard cells in their best case (fast-fast process corner) and worst case (slow-slow process corner) and then ensures reliability by designing the chip with these worst-case estimations [1]. Here, the foundry provides the delay and power for the standard cells in files called standard cell libraries and the designer has to live with degradation of that technology. However, worst-case assumptions introduce a lot of pessimism (i.e., an unnecessarily high timing guardband, which sacrifices circuit performance) and the circuit cannot be hardened against the aging mechanisms. Hence, techniques like aging-aware synthesis [2] or aging-aware timing analysis are employed to harden the circuits for the expected BTI and HCD degradation.

These techniques rely on standard cell characterizations (estimating delay and power of cells) under various aging conditions, e.g. when the circuit only experiences $80\,^{\circ}\mathrm{C}$ instead of $125\,^{\circ}\mathrm{C}$. By optimizing the circuit itself and exploiting these lower conditions ($80\,^{\circ}\mathrm{C}$), these techniques can reduce the pessimism and design faster, yet reliable circuits. Relying on transistor measurements as a foundation for standard cell characterization requires circuit simulations with many assumptions to evaluate the impact of BTI and HCD on these standard cells. For instance, for each standard cell, many different factors need to be considered, such as a range of signal slews, signal activities and load capacitances [2]. In [1] we have shown, how challenging solely obtaining the worst-case signal activities for a standard cell can be. Additionally, in [3] we explored how supply voltage (e.g., near- or sub-threshold operation) and interdependencies of aging mechanisms (amplification and mitigation of the mechanisms on each other) further complicate these simulations.

B. Verification of Standard Cell Characterization

To overcome this challenge, we propose to cross-check/verify the standard cell characterization (creation of degraded library) with standard cell degradation measurements. To verify the predicted/simulated impact of BTI and HCD on standard cells, we propose to employ cell-based RO as well as path-based RO in our "KIPT" chip. For this goal, this work features the following novel contributions:

- The first BTI and HCD measurements of heterogeneous oscillators (multiple different cell types in one RO) based on logic paths extracted from processors.
- The first BTI and HCD measurements on oscillators featuring combinational standard cells, i.e. single standard cells incorporating multiple logic gates (such as And-Or-Inverter (AOI) cells and Or-And-Inverter (OAI) cells) and cells performing complex actions such as full-adders.

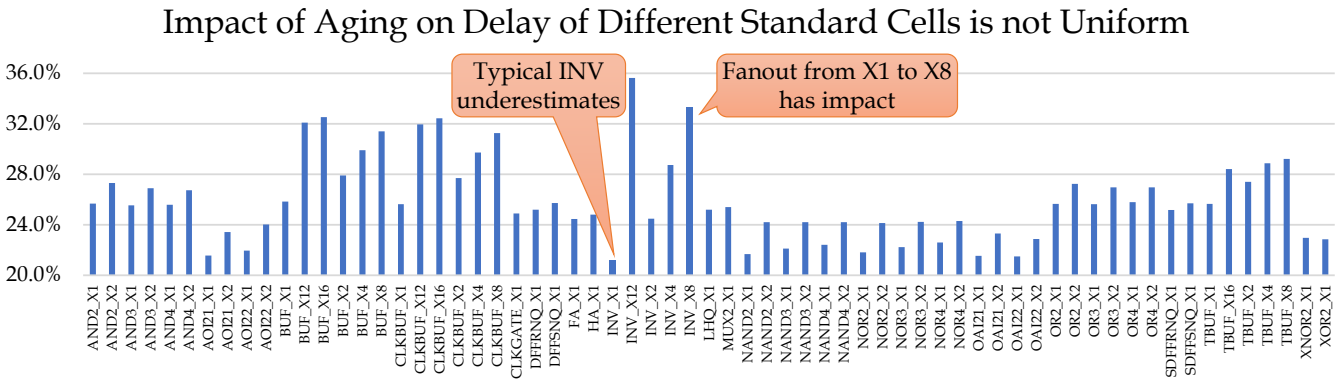

Fig. 1. Simulation of Nangate 14nm OpenCell Library [4] with 14nm FinFET transistors calibrated to Intel transistor data [5]. Each transistor was degraded from $\Delta V_{th} = 0 \rightarrow 51.5\text{mV}$ and the impact on cell delay was measured (averaged per cell over all signal slews and load capacitances).

II. Background - Standard Cells Age Differently

One of the core principles of this publication is that different standard cells exhibit different delay shifts when degraded. We explored this in-depth in previous work about reliability in standard cells such as aging-aware synthesis on degraded standard cells [2], combining BTI and RTN (Random Telegraph Noise) across a large voltage range [3] and exploring the worst-case inputs for standard cells [1]. We present one of these simulations in Fig. 1, which highlights how different cells and their different variants (fan-out) are impacted differently. In addition, aging also impacts the power consumption of cells differently, as leakage and dynamic power is changed differently in each cell as shown in our work in [6]. In summary, each cell type has a unique response in delay and power to aging-induced degradation (e.g., BTI, HCD).

This has been confirmed in silicon measurements from industry [7], [8], which show that different cells have different aging rates. Intel showed in [8], that different standard cells age very differently and concluded when comparing standard cell RO with INV-based RO "*Compared to Inverter-based RO (line-fit), wide variety of aging signatures are seen for other cells*" and further states "*This explains why inverter-based RO, is not a representative circuit to calibrate model parameters*".

This last statement confirms our principle, i.e. we need to characterize each cell individually in terms of delay and power and we cannot take INV-based ROs as a baseline for entire technologies. In fact, neither can any other cell type be representative of the behavior of an entire standard cell library and hence the digital implementation of a CMOS technology.

A. Inverters Over- and Underestimate Aging

Inverters are special standard cells. This is due to the balanced nature of the INV (1 pMOS and 1 nMOS transistor) without any transistors in series or parallel. Hence, an INV-based RO always under- or overestimates with respect to other cells [8]. To explain the underestimations, let us discuss transistors in series. If transistors are in series their degradation accumulates and their combined impact is seen in a prolonged propagation delay through the cell. For the overestimation, we should discuss transistors in parallel. If transistors are parallel, they both drive the same load and as such when just one of the transistors is highly degraded, the other transistor can compensate. Fig. 1 shows how `INV_X1` underestimates the delay impact and the higher fanout `INV_X8` variant (which can provide $8\times$ more current for higher loads) overestimates the delay impact.

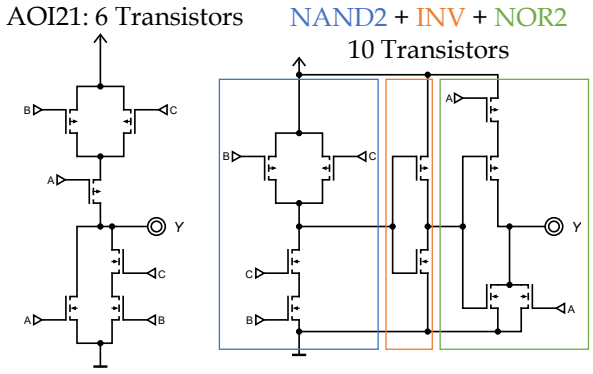

Fig. 2. Combinational or compound cells such as And-Or-Inverter (AOI) save transistors when comparing their implementations to using multiple gates. Cells with fewer transistors feature lower area/power and faster delay. However, their intricate topology results in different aging compared to simple cells. Note, that NAND+INV+NOR is equivalent to AND+INV+OR, but visually closer in terms of topology to the AOI and thus easier to follow.

B. Combinational AOI and OAI Cells

Combinational (or compound) cells such as And-Or-Inverter (AOI) cells and Or-And-Inverter (OAI) cells are much more efficient than their simple cells counterpart. See Fig. 2 for an explanation. These cells are much more complicated compared to simple cells (such as NAND, NOR and XOR) with up to 9 inputs with more than 27 internal transistors. This complexity is necessary as these cells represent more complex Boolean functions by combining multiple Boolean functions of multiple cells into one cell. Additionally, the OAI21 features a wider spread of transistor sizing (e.g., widths) in Table III in the Appendix compared to a single NAND (two are shown).

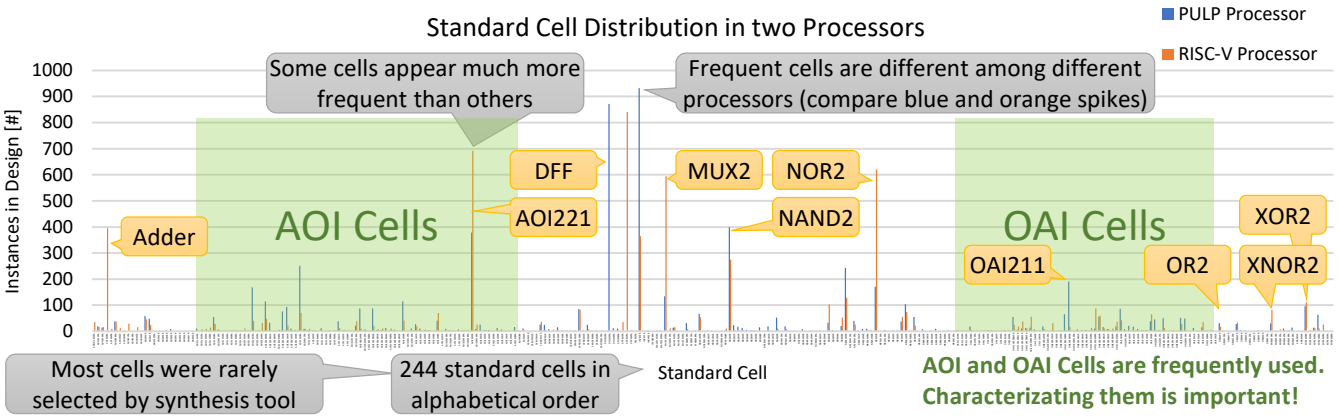

Fig. 3. Distribution of Standard Cells in PULP [9] and RISC-V Processor [10]. 244 Cells are represented in total with multiple versions per type (multiple NAND2, NAND3, NOR4, etc.) for different fan-outs. Processors were synthesized with propagation delay target of 2 ns to enable $f_{clk} = 500$ MHz.

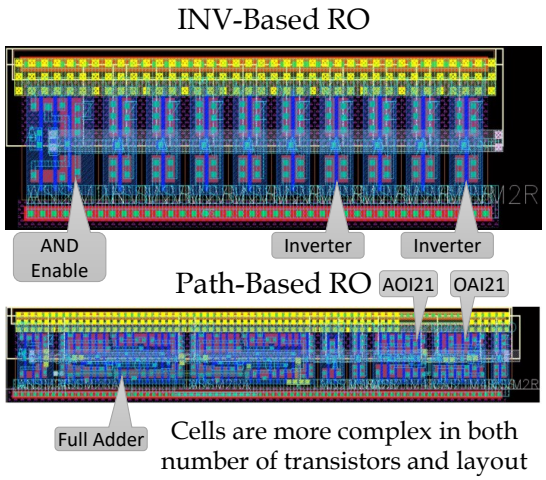

Fig. 4. Path-based ROs differ in two ways from regular reliability oscillators: 1) different cells in the oscillators. 2) Large complex cells incorporated in the oscillators.

III. Limitations of Related Work

This section discusses the limitations of existing work and breaks it down between limitations in existing measurements and limitations in simulations.

A. Measurements

1) Limitations of INV-Based RO: Traditionally, INV-based RO are the most commonly used RO [11], [12] as they are the simplest to design and implement. Additionally, their simplicity allows for evaluations of transistor variants (longer length, higher width (or more fins), lower threshold voltage, etc.) without muddying the results with complicated circuits such as [13], [14].

Unfortunately, INV-based ROs under- or overestimate the impact of aging as shown in Intel measurements in [8] and Sec. II-A. As such, solely employing INV-based RO should not solely be used to characterize a CMOS technology.

2) Limitations of Simple Cell-based RO: Not all works solely explored INV-based ROs. In works targeting digital circuits, ROs consisting of a single cell type such as NAND and NOR are measured in both academia and industry as seen in [7], [8], [11], [12].

However, these works do not cover the standard cells across a standard library. As shown in Fig. 3, a large-scale circuit features 244 different cell types. Importantly, the combinational cells AOI and OAI cells are unexplored. As explained in Sec II we cannot infer their behavior from INV-based or NAND-based ROs. Each cell has its unique degradation. These AOI and OAI cells are frequently omitted as these cells are much more complicated (Sec. II-B). Critically, these cells are among the most frequently used, as they save power/area and gain performance. This is illustrated in Fig. 3, where just one variant (AOI221 - 2-input AND, 2-input OR and INV) features 693 instances and as such is one of the most common cells in the circuit. Additionally, standard cell libraries feature cells, which are not just Boolean logic, such as half- and full adders (frequently abbreviated as HA, FA or AD). Again in our processor in Fig. 3, 395 instances of the 1-bit adder (`ADFM0RA`) are shown, more than $4\times$ more frequent than all OR cells.

Both adders, as well as AOI and OAI cells, are not explored in state-of-the-art oscillators and this work aims to provide initial data for these cell types.

3) Limitations of Logic Path Approaches: Various works do not measure oscillators, but instead logic paths such as the famous RAZOR [15]. Other works use critical (longest delay) logic path sensors of processors such as IBM in [16] to estimate timing in their processors. Most of these sensors and approaches are not specifically designed for aging monitoring such as [17], but can also be used for them.

The key issue with logic path approaches is that there are either complexities of measuring in-situ [15] (which interferes with the measured path and adds measuring logic at congested locations in the circuit) or just a single path is selected as part of a dedicated aging sensor [16]. A single path is solely representative, if that path is the critical path (i.e., path with the longest propagation delay). If the path is critical, then by definition, its delay governs the delay of the entire circuit.

Then, this critical path is used for timing guardband estimations. However, determining if a path is critical, especially if different paths age at different rates (due to their topology or simply because some paths feature higher activity) is very difficult. Consequently, there is an entire research area to determine and thus select the critical paths (typically a set of paths to be safe), such as [17].

In this work, we do not employ aging monitors/sensors. Contrary to the aforementioned and well-known approaches, we do not determine the critical path delay by measuring the path delay directly (e.g., with comparators or counters). Instead, we convert the critical path to oscillators (by selecting the right inputs on the other pins) and measure the oscillation frequency. This has the advantage of removing data words (e.g., applying the right input to the circuit to activate this particular path) and simply activate the path at will (with our AND enable signal). Therefore, we can either use the oscillators to determine the worst-case timing by oscillating for the entire lifetime or we can stop oscillations at any point to consider recovery effects as well. To the best of our knowledge, employing critical paths *in oscillators with enable signals* as a different type of aging sensor has not been explored before.

B. Simulation

1) Mathematical Path Delay Modeling: Degradation due to BTI and HCD depends on various things such as voltage, temperature and the activity (on/off-ratio, toggle rates) of the cells. This is very hard to accurately capture in a simulation. Various works presented simple mathematical approximations of cell delay over time, such as in [18], [19]. However, these works fail to capture the actual behavior of degradation mechanisms, such as layout dependencies [20] and the (non-degraded) transistors opposing the switching of other transistors (e.g., the pull-up transistors are opposing the pull-down transistors) as shown in our previous work in [1]. Furthermore, [1], [2] established that the delay of cells depends significantly on the direct environment of the cell (e.g., load capacitance, signal slew). Therefore, studying degraded standard cells with simple mathematical approximations cannot capture the actual behavior of the cells as part of a circuit (i.e., with circuit parasitics, layout dependencies, load capacitance and signal slew).

2) Machine Learning for Path Delay: Works like [21] rely on machine learning to model path delay. The experimental data in [21] is foundry data for two cells (NAND and NOR), which is then used as training data for a machine learning approach. Our approach differs in that we propose to use each different cell type as the basis for an estimation. The rest of the work in [21] could use our data set to achieve a stronger verification of their work and reduce uncertainty in their machine-learning approach. This larger data set should additionally, simplify training. Hence, this work complements such approaches.

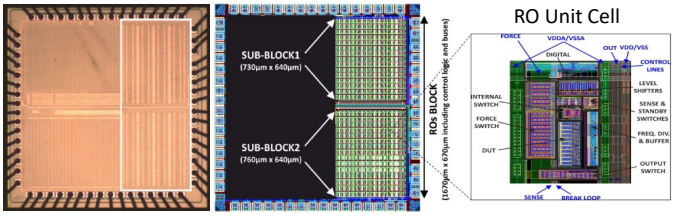

Fig. 5. Micrograph and schematic of the "KIPT" Chip with highlighted ring oscillator (RO) unit cell featuring force-and-sense pads [14].

TABLE I
OSCILLATOR DESCRIPTION

Oscillator	Cells	Description
1	INV	9 × Inverter with Fanout of 2
2	NAND2_X2	9 × 2-input NAND with Fanout of 2
3	NOR2_X2	9 × 2-input NOR with Fanout of 2
4	OAI211_X2	9 × 2-input OR, 1-input AND and INV
5	AOI221_X2	9 × 2-input AND, 2-input OR and INV
6	Pulp Path 1	AND2_X2, INV_X3, NOR2_X4, INV_X1, NOR2_X4, NAND2_X4, OAI21_X1, NOR2_X2, NAND3_X2, INV_X2
7	Pulp Path 2	AND2_X2, INV_X16, NOR2_X8, NOR3_X1, NOR3_X1, NAND2_X3, NOR3_X5 OAI21_X4, AOI21_X4, INV_X2
8	RISC-V Path 1	AND2_X2, Adder_X2, Adder_X2, NAND2_X1, INV_X2, AOI21_X4, OAI21_X4, INV_X2
9	RISC-V Path 2	AND2_X2, Adder_X4, Adder_X2, XNOR2_X8, OAI21_X4, INV_X2

Each oscillator starts with AND2_X2 to provide an enable signal.

IV. MEASUREMENT SETUP

Our setup is the $1.8\,\mathrm{mm} \times 1.8\,\mathrm{mm}$ "KIPT" chip, manufactured in $65\,\mathrm{nm}$ CMOS operating at $1.2\,\mathrm{V}$ and presented in Fig. 5 as well as [13], [14]. The frequency of each RO is passed outside of the chip by routing it over a $16\times$ frequency divider (to simplify design (no RF effects)) to an IO pad. This pad is then routed across our custom PCB and connected to a frequency counter (e.g., an oscilloscope). A DAQ (Data Acquisition System) is used to generate the digital control signals that determine the currently measured RO within the two arrays. A 4-wire power supply with force-and-sense is used to bias the ROs (stress voltage V_{stress} and measure voltage V_{meas}) and the chip is thermally controlled to $80\,^{\circ}\mathrm{C}$ by Temptronics equipment. Lastly, the transistors were carefully sized to minimize random telegraph noise (RTN). This allowed us to keep the measurement uncertainty due to RTN below $1\,\%$ (see Fig. 6).

A. Cell-based and Path-based RO

In this work, we focus on the RO banks on the right in the chip, where we placed nine different RO: Five different cell-based RO and four path-based RO, all presented in Table I. The cells in the cell-based RO were selected as they are the most common cells in large-scale digital design such as microprocessors (see yellow boxes in Fig. 3). Additionally, two paths from the PULP processor [9] and two paths from

TABLE II
STRESS AND MEASURE CYCLES FOR OSCILLATORS WITH $V_{stress} = 1.8\,\mathrm{V}$ AND NOMINAL $V_{meas} = 1.2\,\mathrm{V}$.

Operation	Duration	Voltage	Temperature
Stress	1 s	1.8 V	80 °C
Measure	20 ms	1.2 V	80 °C
Stress	10 s	1.8 V	80 °C
Measure	20 ms	1.2 V	80 °C
Stress	100 s	1.8 V	80 °C
Measure	20 ms	1.2 V	80 °C
Stress	1000 s	1.8 V	80 °C
Measure	20 ms	1.2 V	80 °C
Stress	10 000 s	1.8 V	80 °C
Measure	20 ms	1.2 V	80 °C

During Stress: Enable ON for BTI+HCD, OFF for solely BTI.
During Measure: Enable ON to measure oscillation frequency.

a RISC-V processor [10] were taken. It was infeasible to fit the total path in the space constraint of our measurement (unit cells for each RO), so we selected the most interesting sections of the paths. Both processors were synthesized with a full cell library with 244 different cells. We then connected VDD (logic 1) and GND (logic 0) terminals in such a way to the path, that the logic path started to oscillate. Note, that D-Flipflops (DFF in Fig. 3) are sequential circuits and not logic gates and as such outside of the scope of this work.

B. Measurement Cycle

The stress and measure cycles are presented in Table II. For stress, we either employed DC stress by holding the AND enable (EN) signal to low, preventing oscillation (static transistors) and thus the transistors mainly experience BTI. Or the EN signal can be set to ensure the RO oscillates (switching transistors) during the stress phase (AC stress), resulting in BTI and HCD degradation (HCD requires a current flowing through the transistor). After 1 s, 10 s, 100 s, 1000 s and 10 000 s of stress at $V_{stress} = 1.8\,\mathrm{V}$ we drop the voltage to nominal $V_{meas} = 1.2\,\mathrm{V}$ for 20 ms to measure the oscillation frequency, then we resume the stress. We repeat for $V_{stress} = 2.5\,\mathrm{V}$ to induce a much higher degradation and thus see the differences between the cell types clearer.

V. MEASUREMENTS AND OBSERVATIONS

We first explore a cell-by-cell comparison of cell-based ROs and then cell-based versus path-based RO measurements.

A. Cell-by-Cell Comparisons of Cell-based RO

Fig. 7 illustrates our cell-based RO measurements with 2 samples per cell type measured to account for process variation. The INV-based RO underestimates degradation at DC stress (Fig. 7a) and overestimates it in AC stress (Fig. 7b). Furthermore, each cell type exhibits considerably different degradations, highlighting the need for these measurements and not extrapolating from either INV-based or solely NAND- or NOR-based RO measurements. The NAND and OAI cells are particularly susceptible to HCD degradation, as their degradation doubles from DC to AC, while the AOI and NOR cells just increase by around 40 %.

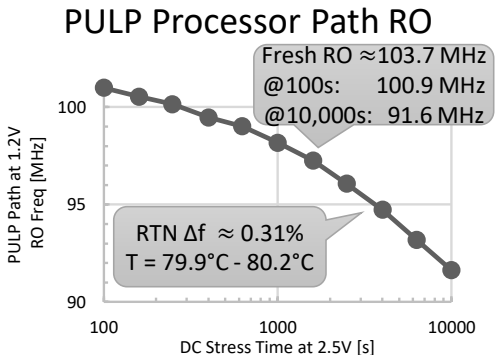

Fig. 6. Frequency degradation of a path-based RO based on a extracted path from the PULP processor [9].

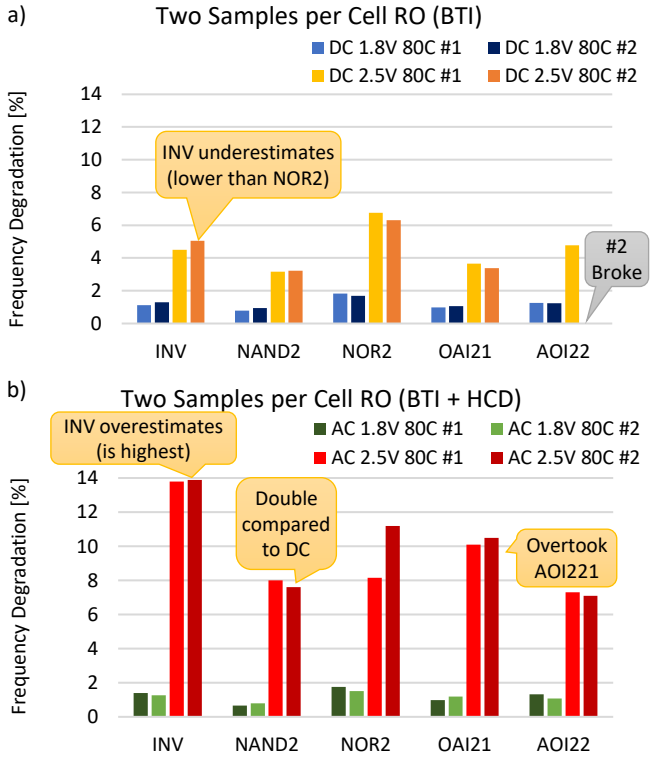

Fig. 7. Aging-induced degradation of oscillation frequency. All oscillators have their frequency reduction measured after 10 000 s of stress (stress at elevated V_{stress}, measurement at nominal 1.2 V) is shown. Two RO samples are measured to account for process variation.

B. Path-Based RO versus Cell-Based RO

Fig. 6 shows the degradation of a path-based RO over time. The RO was designed to oscillate with 1600 MHz and after frequency division by 16 × (see Sec. IV) the measurement starts at 103.7 MHz. With 2.5 V of stress voltage (enable OFF, i.e. DC stress and solely BTI degradation) and 1.2 V measurement voltage, the degradation drops to 100.9 MHz after 100 s and to 91.6 MHz after 10 000 s. Note, that around 1000 s there is an inflection point (change in slope) in the degradation and this is due to the saturation of BTI-degradation, as seen in [3].

Fig. 8 allows a comparison of homogeneous (single cell type) RO with heterogeneous (multiple cell types) path-based

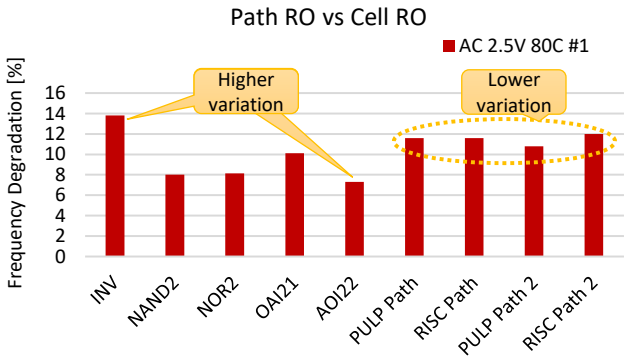

Fig. 8. Aging-induced degradation of oscillation frequency of path-based and cell-based oscillators (see Table I). Note, that the cell-based variations is higher (compare INV to AOI22 with $14\,\%$ to $7\,\%$) than the variation between the path-based ROs (all $\approx 11\,\%$).

RO. It is apparent, that the different cell types average out the degradation along the logic path, resulting in a lower variation between the four paths. In other words, each path oscillates around $11\,\%$ slower after stress is applied, while the cells range from $7\,\%$ (AOI) to $14\,\%$ (INV) slower. This highlights why not just homogeneous RO should be measured, when verifying digital design approaches.

VI. Conclusion

This work shows that measuring combinational cell- and path-based RO instead of INV-based RO, ensures we do not over- or underestimate BTI- or HCD-induced degradations on standard cells. Therefore, these standard cell and path-based RO measurements enable cross-checking/verification of simulation-based aging-aware library characterization approaches such as [1], [2].

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VII. Appendix

TABLE III
Transistor Sizing for NAND2 and OAI21

Transistor	Length	Width	Transistor	Length	Width
OAI21_X4			NAND2_X1		
pMOS 1	60 nm	420 nm	pMOS 1	60 nm	450 nm
pMOS 2	60 nm	1260 nm	pMOS 2	60 nm	450 nm
pMOS 3	60 nm	1260 nm	nMOS 1	60 nm	300 nm
pMOS 4	60 nm	420 nm	nMOS 2	60 nm	300 nm
			NAND2_X4		
nMOS 1	60 nm	420 nm	pMOS 1	60 nm	1260 nm
nMOS 2	60 nm	900 nm	pMOS 2	60 nm	1260 nm
nMOS 3	60 nm	900 nm	nMOS 1	60 nm	900 nm
nMOS 4	60 nm	420 nm	nMOS 2	60 nm	900 nm