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A High–Speed CMOS Current Opamp for Very Low Supply Voltage Operation

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ABSTRACT

A CMOS implementation of a high–gain current mode operational amplifier (opamp) with a single–ended input and a differential output is described. This configuration is the current mode counterpart of the traditional voltage mode opamp. In order to exploit the inherent potential for high speed, low voltage operation normally associated with current mode analog signal processing, the opamp has been designed to operate off a supply voltage of $1.5V$, and the signal path has been confined to N–channel transistors. With this design, a gain of $94dB$ and a gain–bandwidth product of $65MHz$ has been achieved at a power consumption of $30\mu W$.

INTRODUCTION

One of the most popular methods for transformation between the current domain and the voltage domain in analog signal processing is the principle of adjoint networks [1]. Using this principle, many filter constructions well known and characterized in the voltage mode domain are easily transformed into current mode equivalents. Many of them can be implemented using current conveyors [2] as the basic active building block. However, other filters such as Deliyannis bandpass biquad require an active building block with a high gain [3]. In the voltage domain this is easily accomplished with a standard voltage mode opamp, and in the current domain the active building block needed is a current opamp with a single input and a differential output. In the present paper we show a CMOS implementation of a current opamp. As one of the advantages claimed for current mode signal processing is the potential for low voltage operation, the opamp has been designed to require only one N–channel threshold voltage drop in addition to four saturation drain–source
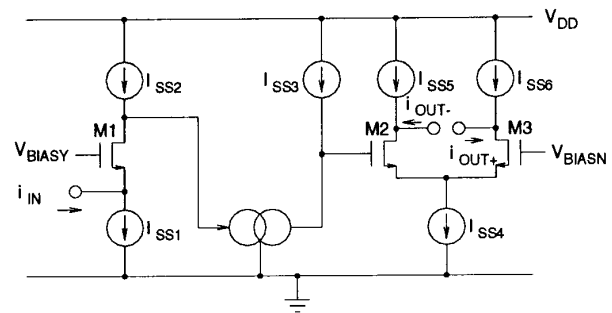

Fig. 1. Current mode opamp configuration with a differential long tail pair output stage and a common gate input stage. The voltages V_{BIASN} and V_{BIASY} are constant bias voltages.

voltage drops, making operation possible at a supply voltage as low as $1.5V$, even in a standard CMOS process with threshold voltages of about $0.9V$.

CURRENT OPAMP CONFIGURATION

A current mode opamp is basically an active device with a low input impedance, a high current gain, and a high output impedance [4, 5]. None of the fundamental components (bipolar transistors or MOS transistors) directly provide these characteristics in any of their basic configurations. Consequently, a two–stage structure is required, consisting basically of a common gate (or common base) input stage to provide a low input resistance and a common source (or common emitter) output stage to provide a high gain and a high output resistance. Thus, the current opamp can be considered as a transimpedance input stage followed by a transconductance output stage and the current gain is equal to the product of the transimpedance and the transconductance.

As a differential output is required, an obvious choice for the output stage is a differential long tail pair with constant current loads. With the tail current equal to the sum of the load currents, this stage provides a high output impedance transconductance stage with the output currents $i_{OUT+} = -i_{OUT-} = -g_{m2}v_Z/2$, where v_Z is the differential input voltage to the stage and g_{m2} is the transconductance of the output transistors. For high speed operation, N–channel transistors are preferable for the long tail pair. As the output stage is driven from a single ended input, one input to the long tail pair is simply connected to a constant bias voltage.

For the input, a common gate stage stage is required. The input resistance of a common gate stage is

$$R_x = \frac{1 + g_{ds1}R_L}{g_{m1} + g_{mb1} + g_{ds1}} \qquad (1)$$

where g_{m1}, g_{mb1}, and g_{ds1} are the MOS input transistor gate transconductance, bulk transconductance, and drain–source conductance, respectively, and R_L is the load resistance at the output (drain) of the common gate stage. From (1) it is evident that with R_L approaching infinity, R_x also approaches infinity. Hence, a moderate value of R_L is required for a low input resistance. However, a large value of R_L is required in order to obtain a high transimpedance. These objectives can be met by the insertion of a current mirror between the common gate input stage and the output stage. With the additional requirement that both the input transistor and the current mirror transistors should be N–channel transistors (for high speed operation), the opamp configuration shown in fig. 1 results. It is evident that all transistor in the signal path are N–channel transistors. It is also seen that the minimum supply voltage required is the gate–source voltage for the output transistor plus the voltage drops required for the current sources I_{SS3} and I_{SS4}.

With this configuration, the resulting differential current gain is

$$A_{0,dm} = \frac{i_{out+} - i_{out-}}{i_{in}} = R_z g_{m2} \qquad (2)$$

where R_z is the parallel combination of the current mirror output resistance and the current source I_{SS3} output resistance.

The opamp also has a finite common mode gain given by

$$A_{0,cm} = \frac{i_{out+} + i_{out-}}{2i_{in}} = \frac{1}{4}\frac{R_z}{R_{SS4}} \qquad (3)$$

where R_{SS4} is the output resistance of the current source I_{SS4}. Hence, the common mode rejection ratio is

$$CMRR = 4g_{m2}R_{SS4} \qquad (4)$$

It is seen that an arbitrarily high $CMRR$ can be achieved through the use of current sources, the output impedance of which can be arbitrarily high [6].

The input impedance R_x is approximately

$$R_x = \frac{1}{g_{m1} + g_{mb1}} \qquad (5)$$

as the last term in the nominator of (1) is much smaller than 1 and g_{ds1} is much smaller than g_{m1}.

The output impedance relations of the differential output stage are described by a common mode output impedance and a differential mode output impedance (corresponding to the common mode and differential mode input impedances for a voltage mode opamp with a balanced, differential input). With ideal current sources I_{SS4}, I_{SS5}, and I_{SS6} (where $I_{SS4} = 2I_{SS5} = 2I_{SS6}$) the common mode output resistance is infinite and there is a perfect matching between the output currents. A difference between the bias current sources results in an offset error between the output currents. Finite current source output resistances result in finite values of common mode output resistance. With $R_{SS5} = R_{SS6}$ a small signal analysis yields the common mode output resistance

$$R_{out,cm} \simeq (2\frac{g_{m2} + g_{mb2}}{g_{ds2}}R_{SS4}) \parallel R_{SS5} \qquad (6)$$

and the differential mode output resistance

$$R_{out,dm} = 2/g_{ds2} \qquad (7)$$

The opamp has a single dominant pole caused by the only high impedance node in the signal path, i.e. the input to the transconductance stage. With C_z being the parallel connection of the input capacitance of the transconductance stage and the output capacitance of the current mirror output stage and R_z being the output resistance of the current mirror in parallel with the output resistance of the current source I_{SS3}, we find the dominant pole at a frequency given by

$$p_d = \frac{1}{2\pi R_z C_z} \qquad (8)$$

This leads to a gain bandwidth product given by

$$GBW = \frac{g_{m2}}{2\pi C_z} \qquad (9)$$

The first higher order pole is most likely caused by the current mirror stage which contributes a pole at a frequency of

$$p_1 = \frac{g_m}{2\pi C_{mirror}} \qquad (10)$$

where C_{mirror} is the current mirror input capacitance in parallel with the output capacitance of the common gate input stage.
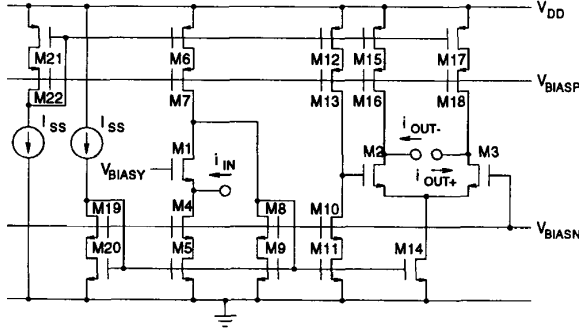
Fig. 2. Transistor diagram of the current mode opamp. The circuit for generating the bias voltages V_{BIASN} and V_{BIASP} is not shown. The voltage V_{BIASY} may be connected to V_{DD} in a system with $V_{DD} = 1.5V$.

EXPERIMENTAL RESULTS

The circuit of fig. 1 has been implemented at the transistor level as shown in fig. 2. For the current sources I_{SS1}, I_{SS2}, I_{SS3}, I_{SS5}, and I_{SS6}, high swing cascode circuits [6] have been employed. For I_{SS4}, a single transistor current source is used in order to enable the output transistors to pull down the output voltage as low as possible. The large voltage swing capability at the output is obtained at the expense of a reduced common mode rejection ratio, see (4).

With this design, we find

$$R_z = \left(\frac{g_{ds10}}{g_{m10} + g_{mb10}} g_{ds11} + \frac{g_{ds13}}{g_{m13} + g_{mb13}} g_{ds12} \right)^{-1} \tag{11}$$

$$R_{SS4} = 1/g_{ds14} \tag{12}$$

$$R_{SS5} = \left(\frac{g_{ds16}}{g_{m16} + g_{mb16}} g_{ds15} \right)^{-1} \tag{13}$$

$$C_z = C_{db10} + C_{gd10} + C_{db13} + C_{gd13}$$
$$+ C_{gd2} + C_{gs2}/2 \tag{14}$$

$$C_{mirror} = C_{db1} + C_{gd1} + C_{db7} + C_{gd7} + C_{db8} + C_{gd8}$$
$$+ C_{gs9} + 2C_{gd9} + C_{gs11} + 2C_{gd11} \tag{15}$$

The circuit has been laid out and fabricated in an industry standard $2\mu m$ CMOS process. All transistors are laid out with minimum channel length, and all N-channel transistors have a channel width to length ratio of 10. The P-channel transistors M12, M13, M21, and M22 have a channel width to length ratio of 30. The P-channel transistors M6 and M7 have a channel width to length ratio of 60. The P-channel transistors M15, M16, M17, and M18 have a channel width to length ratio of 15. The circuit occupies a silicon area of approximately $250\mu m \times 250\mu m$ (not including bias circuits).

TABLE I
TRANSISTOR SMALL SIGNAL PARAMETERS AND OPAMP PARAMETERS

| Transistor parameters		Opamp parameters		
			Calculated	Simulated
$g_{m1}, g_{m9}, g_{m10}, g_{m14}$	$0.150mS$	R_{SS4}	$2.1M\Omega$	
g_{mb1}, g_{mb10}	$0.024mS$	R_{SS5}	$4.1G\Omega$	
g_{ds10}	$0.576\mu S$	R_z	$489M\Omega$	$497M\Omega$
g_{ds11}, g_{ds14}	$0.482\mu S$	C_z	$0.25pF$	$0.26pF$
g_{m2}	$0.105mS$	C_{mirror}	$0.50pF$	
g_{mb2}	$0.018mS$	$A_{0,dm}$	$94.2dB$	$94.2dB$
g_{ds2}	$0.262\mu S$	$A_{0,cm}$	$35.4dB$	$34.0dB$
g_{m13}	$0.126mS$	$CMRR$	$58.8dB$	$60.2dB$
g_{mb13}	$0.037mS$	R_x	$5.7k\Omega$	$5.8k\Omega$
g_{ds12}	$0.268\mu S$	$R_{out,cm}$	$1.3G\Omega$	$1.3G\Omega$
g_{m16}	$0.065mS$	$R_{out,dm}$	$7.6M\Omega$	$7.6M\Omega$
g_{mb16}	$0.018mS$	p_d	$1.30kHz$	$1.25kHz$
g_{ds15}	$0.134\mu S$	GBW	$67MHz$	$65MHz$
		p_1	$50MHz$	
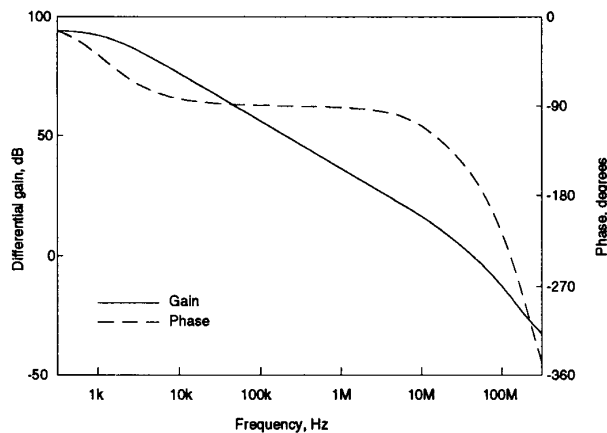
Fig. 3. Simulated open loop frequency response of current mode opamps

Using the design equations (2)–(10) together with equations (11)–(15), we find the opamp characteristics given in Table 1 together with simulated values. The supply voltage used in the simulations is $1.5V$ and the bias current level I_{SS} is $5\mu A$. In the calculation of the capacitances C_z and C_{mirror} according to (14) and (15), it is found that the dominant terms are the drain–bulk capacitances C_{db13} and C_{db7} of the P–channel transistors M13 and M7, respectively. So, even though the signal path transistors are all N–channel, the frequency response is still limited by the parasitic capacitance of P–channel transistors. An obvious route for an optimization of the gain–bandwidth product would then be to increase the width of the output transistors. This would increase g_{m2} and, hence, $A_{0,dm}$ in proportion to the width increase while only slightly increasing C_z, i.e. only slightly decreasing p_d.

Fig. 3 shows the simulated open loop gain and phase response of the opamp. It is seen that the simulations confirm the predictions made from the simple design equations (2)–(10), and the opamp indeed provides a very high gain and bandwidth, even at a power supply of only $1.5V$ and $30\mu A$.

Preliminary measurements on experimental devices obtained through EUROCHIP show performance characteristics close to the simulated values in Table 1. Characterization of the opamp is still in progress and will be reported later. Fig. 4 shows a chip photo of the opamp.

CONCLUSION

A CMOS implementation of a current mode opamp with complementary outputs has been described. The opamp provides a high current gain, and high unity gain bandwidth. It can operate at a supply voltage of $1.5V$ and provides an arbitrarily good matching of the output small signal currents.
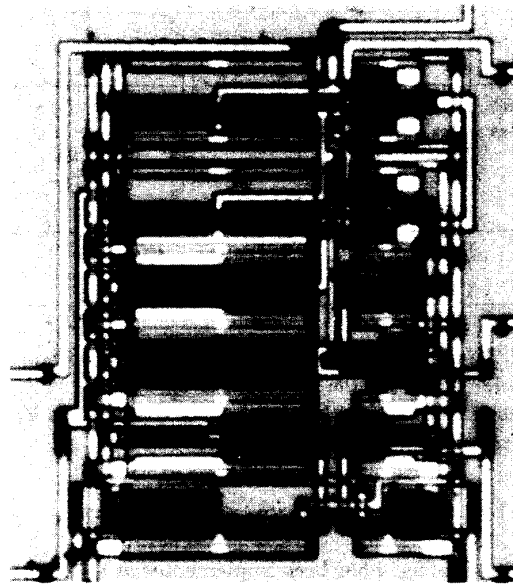

Fig. 4. Chip photo of experimental opamp

Simulation results and measured results from a $2\mu m$ commercial CMOS process confirm the expected behaviour and demonstrate a low frequency gain of $94dB$ and a gain–bandwidth product of $65MHz$ at a modest power consumption of $30\mu W$ (excluding the bias circuitry).

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