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Dynamic Range of Low-Voltage Cascode Current Mirrors

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Abstract — Low-voltage cascode current mirrors are reviewed with respect to the design limitations imposed if all transistors in the mirror are required to operate in the saturation region. It is found that both a lower limit and an upper limit exist for the cascode transistor bias voltage. Further, the use of a signal dependent cascode bias voltage is discussed and a self-biased cascode configuration is presented. This configuration makes it possible to use a higher effective gate-source voltage for the mirror transistors, hence reducing the effect of threshold voltage mismatch on the current mirror gain. The proposed configuration has the advantage of simplicity combined with a complete elimination of the need for fixed bias voltages or bias currents in the current mirror. A disadvantage is that it requires a higher input voltage to the current mirror.

I. INTRODUCTION

Low voltage cascode current mirrors have received considerable attention due to their large output voltage swing and small input voltage compared to a conventional cascode current mirror [1, 2, 3]. This is a most useful property in low voltage/low power analog circuit design. However, as the low voltage current mirror uses a fixed bias voltage for the cascode transistor the dynamic range of the current mirror is limited when both the mirror input transistor and the cascode input transistor are required to stay in saturation. At high input currents the drain-source voltage of the mirror transistors decreases and eventually they will enter the linear region. A consequence of this is

a reduced output impedance and a reduced matching of the mirror transistors. This has been recognized in previous analyses of the low voltage cascode current mirror and puts a design constraint on the cascode bias voltage [2]. At small input currents the input cascode transistor may enter the linear region if the cascode bias voltage is higher than twice the threshold voltage. The output cascode transistor may stay in the saturation region but the mirror input and output transistors no longer see the same drain-source voltages, leading to an increased gain error of the current mirror and to an increased distortion because the gain error depends on the input current.

In this paper we analyze the dynamic range of the low voltage cascode current mirror under the assumption that all transistors are required to stay in the saturation region, and we derive design equations ensuring that this requirement is fulfilled. Further, we discuss circuit configurations which provide an adaptive bias of the cascode transistors and we present a simple biasing configuration which does not require any fixed bias voltages or currents.

II. DYNAMIC RANGE ANALYSIS

The low voltage cascode current mirror is shown in Fig. 1. We assume that the mirror transistors M1 and M2 have identical aspect ratio, i.e. $A_M = W_1/L_1 = W_2/L_2$ where W_1 , W_2 , L_1 , and L_2 are the transistor channel widths and lengths for transistors M1 and M2, respectively. Similarly, M3 and M4 are assumed to have the same aspect ratio, $A_C = W_3/L_3 = W_4/L_4$. The aspect ratio A_M may be different from the aspect ratio A_C . In the analysis of the dynamic range we use the standard Shichman-Hodges transistor model for the transistor in the saturation region and we neglect the bulk effect.

With the input current I_{in} we find the gate-source voltages

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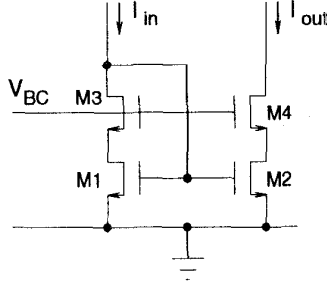


Fig. 1. Low voltage cascode current mirror.

and the drain-source voltages:

$$V_{gs1} = V_T + \sqrt{\frac{2I_{in}}{K'A_M}} \quad (1)$$

$$V_{gs3} = V_T + \sqrt{\frac{2I_{in}}{K'A_C}} \quad (2)$$

$$V_{ds1} = V_{BC} - V_{gs3} = V_{BC} - V_T - \sqrt{\frac{2I_{in}}{K'A_C}} \quad (3)$$

$$\begin{aligned} V_{ds3} &= V_{gs1} - V_{ds1} \\ &= 2V_T - V_{BC} + \sqrt{\frac{2I_{in}}{K'}} \left(\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}} \right) \end{aligned} \quad (4)$$

where V_T is the transistor threshold voltage, V_{BC} is the cascode transistor gate voltage, and K' is the transistor transconductance parameter.

Requiring $V_{gs} - V_T \leq V_{ds}$ for both M1 and M3 results in:

$$\sqrt{\frac{2I_{in}}{K'}} \left(\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}} \right) + V_T \leq V_{BC} \quad (5)$$

$$V_{BC} \leq 2V_T + \sqrt{\frac{2I_{in}}{K'A_M}} \quad (6)$$

Equation (5) ensures saturation of M1 and determines the maximum value of I_{in} for a given value of the cascode bias voltage V_{BC} . We find

$$I_{in,max} = \frac{K'}{2} A_M (V_{BC} - V_T)^2 \left(\frac{\sqrt{A_C/A_M}}{1 + \sqrt{A_C/A_M}} \right)^2 \quad (7)$$

Equation (6) ensures saturation of M3 and determines the minimum value of I_{in} . We find

$$I_{in,min} = \frac{K'}{2} (V_{BC} - 2V_T)^2 A_M \quad (8)$$

In a practical design procedure (8) can be used to determine the maximum value of the bias voltage which will ensure saturation of M3, even at the minimum value of input current, and (7) can then be used to determine values of A_C and A_M which will ensure saturation of M1, even at the maximum value of input current.

In the important special case of $I_{in,min} = 0$ we find from (8) $V_{BC} \leq 2V_T$. From (7) we then find the following design constraint on A_C and A_M :

$$A_M \left(\frac{\sqrt{A_C/A_M}}{1 + \sqrt{A_C/A_M}} \right)^2 \geq \frac{2I_{in,max}}{V_T^2 K'} \quad (9)$$

Assuming as a typical case $W_1 = W_3$ and $L_1 = L_3$, i.e. identical aspect ratios for the mirror transistors and the cascode transistors, we find

$$A_M = A_C = \frac{W}{L} \geq \frac{8I_{in,max}}{V_T^2 K'} \quad (10)$$

In this case the effective gate-source voltage of the mirror transistors M1 and M2 is

$$V_{gs1} - V_T = \sqrt{\frac{2I_{in}}{K'A_M}} = \frac{V_T}{2} \sqrt{\frac{I_{in}}{I_{in,max}}} \quad (11)$$

Obviously, in this case the minimum output voltage of the current mirror is

$$V_{out,min} = V_{BC} - V_T = V_T \quad (12)$$

and is independent of the input current.

In a high precision current mirror one would like to have as large an effective gate-source voltage as possible in order to minimize the effect of threshold voltage mismatch. It is evident that the effective gate-source voltage $V_{gs1} - V_T$ can be increased above the value given by (11) if A_C is increased, i.e. a larger aspect ratio is used for the cascode transistor. In this case the cascode transistor requires a smaller effective gate-source voltage for a given value of input current, leaving more headroom for the drain-source voltage of the mirror transistor. Introducing $N = \sqrt{A_C/A_M}$ we find

$$A_M = \left(\frac{1+N}{N} \right)^2 \frac{2I_{in,max}}{(V_{BC} - V_T)^2 K'} \quad (13)$$

and

$$V_{gs1} - V_T = \frac{N}{1+N} (V_{BC} - V_T) \sqrt{\frac{I_{in}}{I_{in,max}}} \quad (14)$$

We also note that the small signal output resistance of the mirror is given by

$$r_{out} = \frac{1}{g_{ds2}} \left(1 + \frac{g_{m4}}{g_{ds4}} \right) \simeq \frac{1}{g_{ds2}} \frac{g_{m4}}{g_{ds4}} \quad (15)$$

As g_{m4}/g_{ds4} is inversely proportional to the square root of A_C we find that the output resistance is inversely proportional to N . Thus, the higher effective gate-source voltage of the mirror transistors is achieved at the expense of a reduced output resistance.

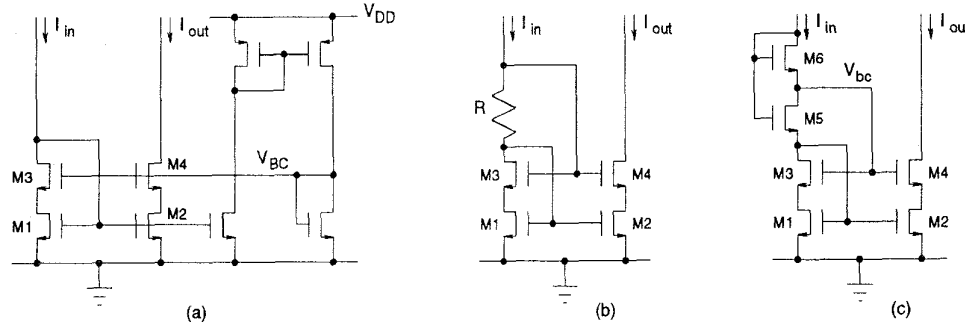


Fig. 2. Cascode current mirrors with adaptive biasing of the cascode transistors. (a) Additional current mirrors for generation of cascode bias. (b) Resistor biasing of cascode transistors. (c) Linear-region transistor biasing of cascode transistors.

III. CASCODE CURRENT MIRRORS WITH ADAPTIVE BIASING

When examining the current mirror of Fig. 1 it is evident that a greater flexibility in the selection of gate-source voltage conditions for a specified range of input currents can be achieved if the cascode transistor gate voltage can be made to increase with increasing input current. If the cascode transistor should be biased to ensure $V_{ds1} = V_{gs1} - V_T$ at all values of input current the cascode bias voltage should be

$$V_{bc} = V_T + \frac{1+N}{N} \sqrt{\frac{2I_{in}}{K'A_M}} \quad (16)$$

A straightforward way to obtain this bias voltage is to generate a replica of the input current and use this to bias the cascode as shown in Fig. 2(a). A more sophisticated method using basically the same idea is to exploit 'super MOS transistors' in the mirror [4]. However, these are fairly complex methods. Another solution is to insert a resistor in series with the input as shown in Fig. 2(b) and use the voltage generated across this resistor as the difference between the mirror transistor gate voltage and the cascode transistor gate voltage. This implementation does not satisfy the nonlinear relation (16) but it does lead to an increase in the input current range and a useful effective input gate-source voltage in excess of the value given by (14). However, it requires that an input resistor in the appropriate range of values can be implemented either as a diffused resistor or as a poly resistor. Also, there is a requirement for matching between the resistor parameters (sheet resistivity) and the transistor transconductance parameter, and this is a problem, especially for poly resistors.

A variation of the approach in Fig. 2(b) is to use a transistor operating in the linear region as a resistor. Equation (16) shows that the resistor should preferably decrease as the input current increases. This is achieved if the gate voltage of the linear-region MOS transistor increases

with the input current. A simple circuit establishing this bias condition is shown in Fig. 2(c). In passing, it can be mentioned that the circuit of Fig. 2(c) is easily extended to provide bias voltages for cascode current mirrors with more transistors in the cascode [2]. Transistor M5 just has to be split into an appropriate number of transistors in order to create more taps on the voltage divider string M5, M6. The voltage divider M5, M6 may be analyzed by first calculating the gate-source voltage of M5 when M5, M6 is considered as a single transistor with an effective aspect ratio A_B given by $A_B^{-1} = A_5^{-1} + A_6^{-1}$. Next, the drain-source voltage of M5 is found using the Shichman-Hodges drain current relation for the linear region

$$V_{ds5} = \sqrt{\frac{2I_{in}}{K'A_B}} \left(1 - \sqrt{\frac{A_B}{A_6}}\right) \quad (17)$$

From (17) we find that (16) is fulfilled if

$$N = \sqrt{\frac{A_M}{A_B}} - \sqrt{\frac{A_M}{A_6}} \quad (18)$$

In order to minimize the input voltage it is advantageous to select a large value of A_6 . As an example, for $N = 1$ and $A_6 = 4A_M$ we find $A_5 = A_M/2$. Thus, the circuit shown in Fig. 2(c) provides almost ideal biasing conditions for the cascode transistors. This is achieved at the expense of an input voltage to the current mirror which is

$$V_{in} = V_{gs1} + V_{gs5} = 2V_T + \sqrt{\frac{2I_{in}}{K'}} \left(\frac{1}{A_M} + \frac{1}{A_B}\right) \quad (19)$$

and this value is about twice the value found in the original low voltage cascode mirror. It is, however, comparable to the input voltage of a conventional cascode current mirror. For the adaptive bias current mirror we find the minimum output voltage given by

$$V_{out,min} = V_{bc} - V_T = \frac{1+N}{N} \sqrt{\frac{2I_{in}}{K'A_M}} \quad (20)$$

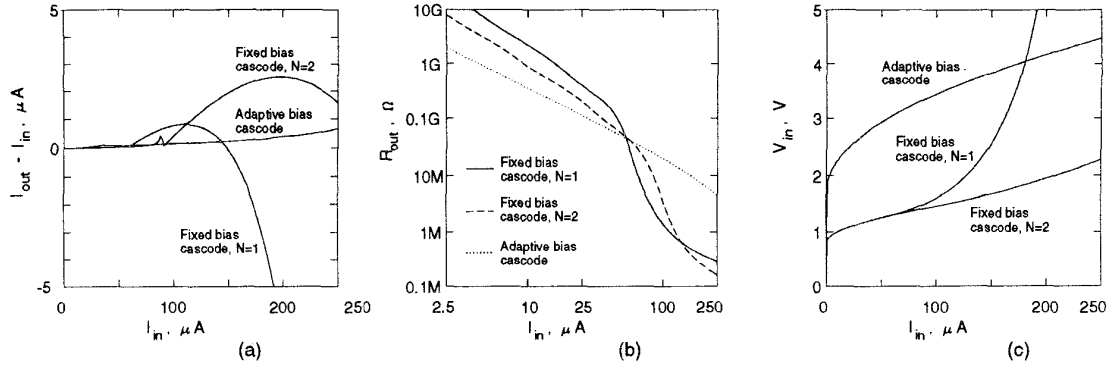


Fig. 3. Simulated results from cascode current mirrors. (a) Output error versus input current. (b) Output resistance. (c) Input voltage.

In contrast to the fixed bias current mirror, this minimum output voltage is dependent on the input current, decreasing with decreasing input current.

We also find the output resistance of the adaptive bias current mirror given by (15) and, thus, the output resistance is in principle unaffected by the biasing circuit. In practice, the biasing of the output transistors at the edge of saturation leads to a somewhat lower output resistance.

Both current mirrors with a fixed cascode bias voltage and the adaptive cascode bias voltage mirror of Fig. 2(c) have been simulated using Spice parameters from a commercially available $2\mu m$ CMOS process. The mirrors have been simulated with $L_1 = 10\mu m$, $W_1 = 100\mu m$, i.e. $A_M \approx 10$. For the fixed bias mirrors V_{BC} has been chosen to be $2V_T$, and the simulations have been carried out for $N = 1$ and $N = 2$. With these geometries we would expect maximum input current ranges of $50\mu A$ and $110\mu A$, corresponding to $N = 1$ and $N = 2$, respectively. For the adaptive bias mirror, we have chosen $N = 1$, $A_5 = 4.5$, and $A_6 = 40$. A_5 has been selected slightly smaller (about 20% smaller) than the value found from (18) in order ensure saturation of M1 and M2, even in the presence of bulk effect or process variations. Fig. 3 shows the simulation results. In Fig. 3(a) we show the difference between the input current and the output current. In Fig. 3(b) we show the simulated output resistance of the mirrors, and in Fig. 3(c) we show the input voltage versus the input current. The simulations show a reasonable agreement with the simple theory outlined above, and they certainly confirm the superiority of the adaptive biasing with respect to dynamic range.

Further simulations show that the adaptive bias current mirror of Fig. 2(c) has high frequency properties which are very similar to those of the fixed bias current mirror. In contrast to this, the adaptive bias current mirror of Fig. 2(a) has an additional signal path to the cascode transistors which slows down the mirror due to the added input

capacitance. However, a thorough discussion of this falls outside the scope of the present paper.

IV. CONCLUSION

We have analyzed a low voltage cascode current mirror and derived a set of design equations ensuring that both mirror transistors and cascode transistor operate in the saturation region. For a mirror with identical transistor sizes it is found that these constraints limit the effective gate-source voltage of the mirror transistors to $V_T/2$ at the maximum input current if the input cascode transistor should work at input currents approaching zero. A higher effective gate-source voltage can be achieved by using cascode transistors with a large aspect ratio W/L . In this way, the effective gate-source voltage can approach V_T for the maximum input current. If even higher gate-source voltages are desired, an adaptive biasing of the cascode transistors can be employed. Several methods for achieving this are shown, including a novel self biasing scheme using only two additional transistors for the cascode biasing.

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