

# RELIABLE ANALYSIS OF SETTling ERRORS IN SC INTEGRATORS – APPLICATION TO THE DESIGN OF HIGH-SPEED $\Sigma\Delta$ MODULATORS

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## ABSTRACT

This paper presents a detailed study on the transient response of SC integrators which takes into account the effects of amplifier finite gain-bandwidth product, slew-rate, and parasitic capacitances. Unlike previous models, both the integration and the sampling phases are considered. Experimental measurements of the settling error power of a 2nd-order  $\Sigma\Delta$  modulator are used to validate the model. When compared to previous models, the new one provides more reliable estimations of the defective settling in optimized high-speed  $\Sigma\Delta$  modulators. The results in the paper show up to -16dB difference in the estimation of the in-band error power of a 2-1-1mb  $\Sigma\Delta$  intended for 14bit@4MSamples/s.

## 1. INTRODUCTION

As the sampling frequency of  $\Sigma\Delta$  Modulators ( $\Sigma\Delta$ Ms) increases in order to cope with XDSL specifications – demanding high-resolution and high-speed operation – integrator defective settling becomes one of the dominant limiting factors in SC implementations. In this scenario, knowing and quantifying the main mechanisms degrading the settling of SC integrators is mandatory to reduce the modulator power consumption by minimizing the amplifier requirements.

Although most SC integrator models [1]-[5] take into account the amplifier finite gain-bandwidth product ( $GB$ ) and slew-rate ( $SR$ ), they do so only for the integration phase, while errors arising during the sampling phase are omitted, leading to an under-estimation of defective settling which becomes specially significant for high-speed applications. The SC integrator model presented in [6] includes all the errors above, but the developed study is centered on

filter design and cannot be easily extended to the case of  $\Sigma\Delta$ Ms.

This paper focuses on the analysis of the transient response of a general SC integrator during both the integration and sampling phases, with special emphasis in SC  $\Sigma\Delta$ Ms. The resulting model provides precise estimations of settling errors limiting the performance of high-speed  $\Sigma\Delta$ Ms.

## 2. TRANSIENT RESPONSE OF SC INTEGRATORS

### 2.1 SC Integrator Model

Fig.1 shows the generic SC integrator scheme considered herein. This scheme includes:

- $i$  input branches connected to switching input voltage levels,  $V_{i1}$  and  $V_{i2}$ ,
- the parasitic capacitor  $C_p$  associated to the integrator summation node,
- the capacitive load  $C_l$  associated to the amplifier output node and to the bottom plate of the integration capacitor  $C_o$ , and
- $j$  branches of an assumed integrator connected to its output during the sampling phase, which has switched to input levels  $V_{nj2}$  during the previous integration phase.

On the other hand, the amplifier, depicted in Fig.2, is considered to have:

- a non-linear static characteristic, with maximum output current  $I_o$ , and
- a single-pole dynamic.

With this model for the SC integrator, the amplifier  $GB$  and  $SR$  limitations are taken into account, as well as parasitic capacitors associated to its input and output nodes. Moreover, capacitive load at the integrator output is considered to change from the integration to the sampling phase, what reflects the actual situation in most SC sections.

### 2.2 Integration Phase

Be  $v_{a,n-1}$  and  $v_{o,n-1}$ , respectively, the opamp input and output voltages at the end of the  $n-1$ -th sampling phase.

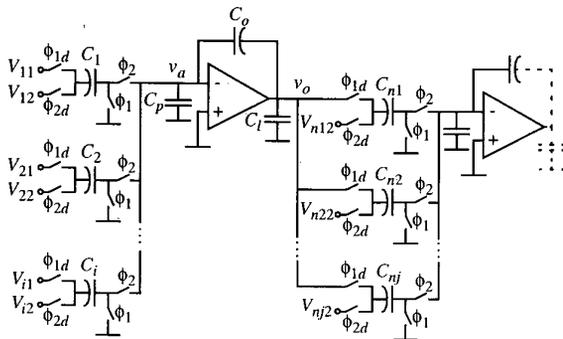


Fig. 1: SC integrator model.

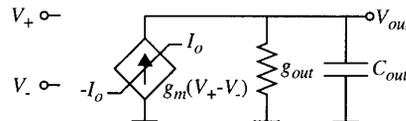


Fig. 2: Amplifier model.

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Charge-conservation at the beginning of the integration phase,  $t = 0$ , determines a jump on these voltages to values:

$$v_{ai,i} = \frac{1}{C_{eq,i}} \left( 1 + \frac{C_l}{C_o} \right) \sum_{k=1}^i (V_{k2} - V_{k1}) C_k + \frac{C'}{C_{eq,i}} v_{a,n-1} \quad (1)$$

$$v_{oi,i} = v_{o,n-1} + \frac{C_o}{C_o + C_l} (v_{ai,i} - v_{a,n-1})$$

where  $C' = C_p + C_l(1 + C_p/C_o)$ , and  $C_{eq,i}$  is the equivalent capacitive load at the amplifier output during the integration phase, given by:

$$C_{eq,i} = C_p + \sum_{k=1}^i C_k + C_l \left[ 1 + \left( C_p + \sum_{k=1}^i C_k \right) / C_o \right] \quad (2)$$

Eq.(1) shows that  $v_a$  and  $v_o$  exhibit, at the beginning of this phase, steps in the opposite direction to their final values (see Fig.3). It must be also remarked that, unlike previous models [1]-[5], we have considered  $v_{a,n-1} \neq 0$ , which reflects the possibility of having this node incompletely discharged by the end of the preceding sampling phase.

Depending on the initial value of the amplifier input voltage, two possibilities can be identified:

- (a)  $|v_{ai,i}| \leq I_o/g_m$ , where  $I_o$  stands for the amplifier maximum output current and  $g_m$  stands for its transconductance. The amplifier will then operate linearly and its input node will discharge exponentially following:

$$v_a(t) = v_{ai,i} \exp\left(-\frac{g_m}{C_{eq,i}} t\right) \quad (3)$$

where  $g_m \gg g_{out}$  has been supposed.

- (b)  $|v_{ai,i}| > I_o/g_m$ ; the amplifier will then slew so that its input node will evolve with constant slope:

$$v_a(t) = v_{ai,i} - \frac{I_o}{C_{eq,i}} \text{sgn}(v_{ai,i}) t \quad (4)$$

The slewing mode will go on until  $t = t_{o,i}$ , when the condition for the amplifier to start operating linearly,  $v_a(t_{o,i}) = I_o/g_m$ , fulfills. From this condition, we get:

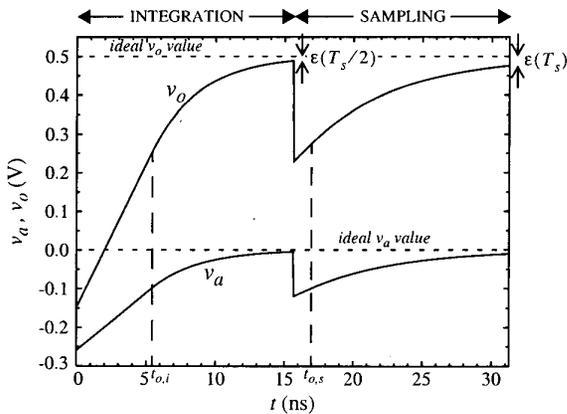


Fig. 3: Transient evolution of the SC integrator.

$$t_{o,i} = \frac{C_{eq,i}}{I_o} |v_{ai,i}| \frac{C_{eq,i}}{g_m} \quad (5)$$

and from then on  $v_a(t)$  will relax exponentially:

$$v_a(t) = \frac{I_o}{g_m} \text{sgn}(v_{ai,i}) \exp\left[-\frac{g_m}{C_{eq,i}} (t - t_{o,i})\right] \quad (6)$$

During the integration phase  $v_o(t)$  is given by

$$v_o(t) = v_{o,n-1} - \left( 1 + \frac{C_p}{C_o} \right) v_{a,n-1} - \sum_{k=1}^i \frac{C_k}{C_o} (V_{k2} - V_{k1}) + \left[ 1 + \left( C_p + \sum_{k=1}^i C_k \right) / C_o \right] v_a(t) \quad (7)$$

where  $v_a(t)$  stands for eq.(3), (6) or (4) depending, respectively, on the amplifier linear operation, partial- or complete-slewing during this phase.

At the end of the integration phase,  $t = T_s/2$ ,  $v_a$  and  $v_o$  will be given by:

$$v_a\left(\frac{T_s}{2}\right) = \begin{cases} v_{ai,i} \exp\left(-\frac{g_m}{C_{eq,i}} \frac{T_s}{2}\right) & |v_{ai,i}| \leq \frac{I_o}{g_m} \\ v_{ai,i} - \frac{I_o}{C_{eq,i}} \text{sgn}(v_{ai,i}) \frac{T_s}{2} & \frac{T_s}{2} \leq t_{o,i} \\ \frac{I_o}{g_m} \text{sgn}(v_{ai,i}) \exp\left[-\frac{g_m}{C_{eq,i}} \left(\frac{T_s}{2} - t_{o,i}\right)\right] & \frac{T_s}{2} > t_{o,i} \end{cases} \quad (8)$$

$$v_o\left(\frac{T_s}{2}\right) = v_{o,n-1} - \left( 1 + \frac{C_p}{C_o} \right) v_{a,n-1} - \sum_{k=1}^i \frac{C_k}{C_o} (V_{k2} - V_{k1}) + \left[ 1 + \left( C_p + \sum_{k=1}^i C_k \right) / C_o \right] v_a\left(\frac{T_s}{2}\right)$$

### 2.3 Sampling Phase

Be  $v_a(T_s/2)$  and  $v_o(T_s/2)$  the opamp input and output voltages, respectively, at the end of the preceding integration phase. Charge-conservation at  $t = T_s/2$  determines new steps<sup>†</sup> on these voltages so that,

$$v_{ai,s} = v_a\left(\frac{T_s}{2}\right) - \sum_{k=1}^j \frac{C_{nk}}{C_{eq,s}} \left[ v_o\left(\frac{T_s}{2}\right) - V_{nk2} \right] \quad (9)$$

$$v_{oi,s} = v_o\left(\frac{T_s}{2}\right) + \left( 1 + \frac{C_p}{C_o} \right) \left[ v_{ai,s} - v_a\left(\frac{T_s}{2}\right) \right]$$

where  $C_{eq,s}$  refers to the equivalent capacitive output load during the sampling phase, given by:

$$C_{eq,s} = C_p + \left( C_l + \sum_{k=1}^j C_{nk} \right) \left( 1 + \frac{C_p}{C_o} \right) \quad (10)$$

Again, eq.(9) shows that the steps in  $v_a$  and  $v_o$  happen in the opposite direction to their final values (see Fig.3).

Depending on the initial amplifier input voltage, two possibili-

<sup>†</sup>. For simplicity purposes, next integrator input node has been supposed totally relaxed by the end of the preceding integration phase.

ties can be identified:

(a)  $|v_{ai,s}| \leq I_o/g_m$ ; the opamp operates linearly and,

$$v_a(t) = v_{ai,s} \exp\left[-\frac{g_m}{C_{eq,s}}\left(t - \frac{T_s}{2}\right)\right] \quad (11)$$

(b)  $|v_{ai,s}| > I_o/g_m$ ; the opamp slews and its input node evolves with constant slope:

$$v_a(t) = v_{ai,s} - \frac{I_o}{C_{eq,s}} \operatorname{sgn}(v_{ai,s}) \left(t - \frac{T_s}{2}\right) \quad (12)$$

The slewing will go on until the instance  $t = t_{o,s}$ , where  $v_a(t_{o,s}) = I_o/g_m$  such that,

$$t_{o,s} = \frac{T_s}{2} + \frac{C_{eq,s}}{I_o} |v_{ai,s}| - \frac{C_{eq,s}}{g_m} \quad (13)$$

From this instance, the opamp starts operating linearly and, consequently,  $v_a(t)$  starts to exponentially decay,

$$v_a(t) = \frac{I_o}{g_m} \operatorname{sgn}(v_{ai,s}) \exp\left[-\frac{g_m}{C_{eq,s}}(t - t_{o,s})\right] \quad (14)$$

During the sampling phase  $v_o(t)$  is given by:

$$v_o(t) = v_o\left(\frac{T_s}{2}\right) + \left(1 + \frac{C_p}{C_o}\right) \left[v_a(t) - v_a\left(\frac{T_s}{2}\right)\right] \quad (15)$$

where  $v_a(t)$  stands for eq.(11), (14) or (12) depending on the opamp linear operation, partial- or complete-slewing during this phase.

At the end of the sampling phase,  $t = T_s$ ,  $v_a$  and  $v_o$  will be:

$$v_a(T_s) = \begin{cases} v_{ai,s} \exp\left(-\frac{g_m T_s}{C_{eq,s}}\right) & |v_{ai,s}| \leq \frac{I_o}{g_m} \\ v_{ai,s} - \frac{I_o}{C_{eq,s}} \operatorname{sgn}(v_{ai,s}) \frac{T_s}{2} & , T_s \leq t_{o,s} \\ \frac{I_o}{g_m} \operatorname{sgn}(v_{ai,s}) \exp\left[-\frac{g_m}{C_{eq,s}}(T_s - t_{o,s})\right] & , T_s > t_{o,s} \end{cases} \quad (16)$$

$$v_o(T_s) = v_o\left(\frac{T_s}{2}\right) + \left(1 + \frac{C_p}{C_o}\right) \left[v_a(T_s) - v_a\left(\frac{T_s}{2}\right)\right]$$

## 2.4 Overall Integration-Sampling Process

Previous analyses can be easily concatenated, so that the transient evolution of the integrator output voltage is accurately described for the overall integration-sampling process. The nine different evolutions that can be obtained for the complete process are summarized in Table 1. Out of these nine possibilities<sup>‡</sup>, the actual SC integrator response will mainly depend on the input signals level as well as on the amplifier static characteristics.

At the end of the integration-sampling process,  $v_o$  will be

$$v_{o,n} = v_{o,n-1} - \sum_{k=1}^i \frac{C_k}{C_o} (V_{k2} - V_{k1}) + \Theta(\tau_i) + \Theta(\tau_s) + \Theta(\tau_p, \tau_s) \quad (17)$$

where error terms derived from an incomplete settling during both

‡. Although possible, evolutions 3 and 7 are unlikely to occur in practice, since they imply a huge change on the values of capacitors in the connected SC sections, which is not usual in  $\Sigma\Delta$ Ms.

TABLE 1: Possible evolutions during the integration-sampling process

	INTEGRATION		SAMPLING	
1	Linear	eq.(3)	Linear	eq.(11)
2	Partial-slew	eq.(6)	Linear	eq.(11)
3	Slew	eq.(4)	Linear	eq.(11)
4	Linear	eq.(3)	Partial-slew	eq.(14)
5	Partial-slew	eq.(6)	Partial-slew	eq.(14)
6	Slew	eq.(4)	Partial-slew	eq.(14)
7	Linear	eq.(3)	Slew	eq.(12)
8	Partial-slew	eq.(6)	Slew	eq.(12)
9	Slew	eq.(4)	Slew	eq.(12)

clock-phases are added to the ideal  $v_{o,n}$  value. These error terms can be obtained for each possible evolution by the linking of its equations during the sampling phase to those of the preceding integration phase (see Table 1).

Fig.3 shows an evolution with a partial-slewing during both clock-phases and illustrates the influence of the sampling dynamics. Considering only the integration phase would lead in this case to an under-estimation of the defective settling error, since the error on the settled voltage at the end of the sampling phase,  $\epsilon(T_s)$ , is larger than it was at the end of the integration phase,  $\epsilon(T_s/2)$ .

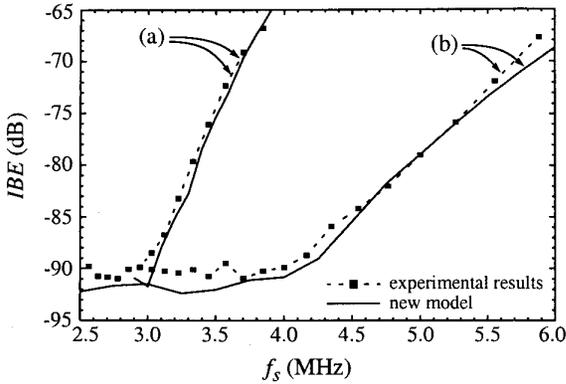
## 3. APPLICATION TO $\Sigma\Delta$ Ms DESIGN

### 3.1 Validation of the New Model by Experimental Results

Previous equations have been introduced in ASIDES [4], a behavioral simulation tool for SC  $\Sigma\Delta$ Ms. A 2nd-order  $\Sigma\Delta$ M [4], designed on a 0.7 $\mu$ m CMOS technology, was used for its verification.

The modulator nominally operates at sampling frequency  $f_s = 2.46$  MHz, with oversampling ratio  $M = 128$ , and  $\pm 1.5$  V reference levels, providing 15bit effective resolution at 19.2kSamples/s. Experimental measurements of the modulator in-band error power (*IBE*) were taken while increasing  $f_s$ , in order to make the defective settling error power the dominant source degrading modulator performance. The modulator output stream was acquired by a HP8200 test unit and transferred to a work-station, where it was decimated with a 1024-coefficient FIR filter using MATLAB. The dynamic of the opamps was externally controlled by changing the biasing conditions, so that experimental results for different opamp features were obtained.

Fig.4 compares experimental measurements of the *IBE* with a -6dB@4.8kHz input tone with behavioral simulations carried out using ASIDES. For two biasing conditions of the amplifiers, it can be seen how defective settling error power becomes dominant as  $f_s$  increases above 3MHz and 4MHz, for the slow and fast case, respectively. Note the good agreement between simulated and experimental results. Moreover, this agreement extends to the whole wide range of sampling frequencies considered,  $2.5\text{MHz} \leq f_s \leq 6.0\text{MHz}$ , in which settling error power grows over other error contributions up to 25dB.



**Fig. 4:** Comparison of the new model with experimental results on a 2nd-order  $\Sigma\Delta M$ , for: (a) Slow case ( $g_m = 229\mu A/V$ ,  $I_o = 16.7\mu A$ ), and (b) Fast case ( $g_m = 294\mu A/V$ ,  $I_o = 28\mu A$ ).

### 3.2 Comparison with Previous Models through Behavioral Simulations

Traditional models for the SC integrator take into account the amplifier  $GB$  and  $SR$  limitations during integration, while possible settling errors derived from the sampling process are omitted. This is done assuming that the amplifier equivalent load during the sampling phase is considerably smaller than that during the integration phase; that is

$$C_{eq,s} \ll C_{eq,i} \quad (18)$$

Under this condition, the integrator summation node completely relaxes during the sampling phase, so that  $v_a(T_s) = 0$  and eq.(16) turns out to be:

$$v_o(T_s) = v_o\left(\frac{T_s}{2}\right) - \left(1 + \frac{C_p}{C_o}\right)v_a\left(\frac{T_s}{2}\right) \quad (19)$$

However, in practice eq.(18) may be either fulfilled or not depending on the particular design. In practice, for many  $\Sigma\Delta M$  designs, as long as the sampling capacitors of the next integrator in the architecture,  $C_{nj}$ , are taken into account  $C_{eq,s}$  becomes comparable to the capacitive load during the integration phase,

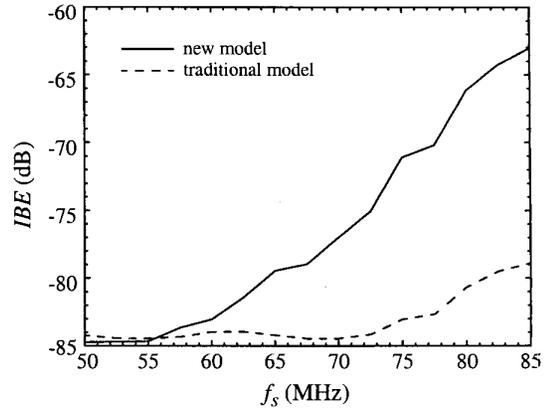
$$C_{eq,s} \sim C_{eq,i} \quad (20)$$

getting higher than  $C_{eq,i}$  in certain cases.

This leads to an incomplete discharge of the integrator summation node, and therefore to an additional error during the sampling phase, which can become important as the operating frequency of  $\Sigma\Delta M$ s increases.

In order to illustrate this, behavioral simulations have been carried out on a high-speed  $\Sigma\Delta M$  with ASIDES, using both traditional and new models for the SC integrator dynamics. The modulator being considered is a 2-1-1mb cascade trying to fulfil specifications of 14bit@4MSamples/s, which nominally operates with sampling frequency  $f_s = 64\text{MHz}$ , oversampling ratio  $M = 16$ , last-stage quantizer resolution  $B = 4$  and reference levels  $\pm V_r = \pm 1V$ .

Fig.5 compares the results obtained with ASIDES for both mod-



**Fig. 5:** Comparison of new and traditional models on a 2-1-1mb  $\Sigma\Delta M$ .

els, showing the modulator in-band error as a function of the sampling frequency. Note that defective settling error power increases as  $f_s$  does, raising over the remaining noise contributions. Nevertheless, the rate of increase is considerably lower for the traditional model. Not considering the errors derived from a finite integrator dynamic during the sampling phase provides in this case a significantly high under-estimation of the defective settling error power, leading to too optimistic results.

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