The Development of Bipolar Log-Domain Filters in a Standard CMOS Process

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Abstract

Log-domain filters have emerged in recent years as a new and important class of continuous-time filter. The attractive features of these filters include their compact structure, their potential to run at high frequencies while operating from low power supplies, and their electronic tunability. At the heart of the log-domain filtering technique is the logarithmic / exponential relationship between voltage and current in a transistor. In this work, the development of log-domain filters in CMOS technology will be investigated. The lateral bipolar transistor, inherent to CMOS processes, will be used for this purpose.

A SPICE compatible model for a lateral PNP transistor, fabricated in 0.35μ CMOS technology, is presented. A log-domain integrator, which makes use of both lateral PNP transistors and MOSFET transistors operating in strong inversion, as well as a biquadratic low-pass log-domain filter and a third order elliptic low-pass log-domain filter, have each been designed and characterized in 0.35μ CMOS technology. Experimental results indicate that these filters are capable of operation at frequencies up to 10 MHz. For the elliptic filter operating at a bias current of 10 μA, the experimentally measured total harmonic distortion is -39.6 dB for an input current of 5 μA (a 50% current modulation index), the dynamic range is -34.1 dB, and the total power consumption is 183 μW / pole from a 2.5 V supply. These filters are capable of operating at significantly higher frequencies than CMOS log-domain filters described in the literature which make use of MOSFET transistors operating in weak inversion.

Résumé

Ces dernières années ont vu les filtres logarithmiques s'imposer comme classe importante des filtres continus. L'attrait pour cette classe de filtres réside, entre autres, dans leur structure compacte, leur potentiel a opérer en très haute fréquence sous faible puissance d'alimentation ainsi que leur "réglabilite". Au coeur de la technique de filtrage logarithmique se trouve la relation logarithmique / exponentielle entre potentiel et courant dans un transistor. Dans ce travail, nous étudions le développement des filtres logarithmique en technologie CMOS. Le transistor bipolaire latéral inhérent aux processus CMOS est utilisé a cette fin.

Un modèle du transistor latéral PNP fabriqué dans la technologie CMOS 0.35μm et compatible avec SPICE est présenté. Un intégrateur logarithmique, utilisant à la fois des transistors bipolaires PNP latéraux ainsi que des MOSFETs en régime d'inversion forte, un filtre logarithmique biquadratique passe bas et un filtre logarithmique elliptique passe bas du troisième ordre on été conçus et characterisés en technologie CMOS 0.35μm. Les résultats expérimentaux indiquent que ces filtres sont capables d'opérer à des fréquences allant jusqu'a 10 MHz. Pour le filtre elliptique à 10μA de courant de polarisation, la distorsion harmonique totale (THD) mesurée expérimentalement est de -39.6 dB pour un courant d'entrée de 5 μA (indicede modulation de courant de 50%), l'étendu dynamique est de -34.1 dB et la consommation totale de puissance est de 183 μW pour une alimentation de 2.5 V. Ces filtres sont capables d'opérer à des fréquences significativement plus hautes que les filtres logarithmiques CMOS décrit dans la littérature ou les transitors MOSFET opèrent en régime d'inversion faible.

Dedication

To Margaret, for your care and wisdom which has pulled me through.

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Chapter 1 - Introduction

1.1 - Motivation

Log-domain filters have emerged in recent years as a new and important class of continuous-time filter. Unlike conventional classes of filters, in which linear circuits are implemented using non-linear devices, log-domain filters directly employ a transistor's non-linear (in this case, logarithmic) behaviour. Without the need for conventional circuit linearization techniques, log-domain filter circuits have a simple and elegant structure, and hold potential to run at high frequencies and operate from low power supplies. Log-domain filters also possess many other attractive features, including the ability to be electronically tuned over a wide range of frequencies. In addition, as is the case with all companding filters, log-domain filters are theoretically capable of obtaining very large dynamic ranges [1].

At the heart of the log domain filtering technique is the logarithmic / exponential relationship between voltage and current in a transistor - traditionally, a bipolar transistor. For economic and system-integration reasons, efforts are underway to extend the log-domain approach from bipolar to CMOS technology. Most research on this topic has focused on the use of the MOS transistor operating in weak inversion. Though such devices exhibit the desired logarithmic / exponential behaviour, the relatively low operating currents place limitations on the bandwidth which can reasonably be achieved.

In addition, the modelling of subthreshold characteristics in commercial CMOS processes is often insufficient for high performance applications.

An alternate approach to the implementation of log domain filters in CMOS technology, and one which avoids the low current and low bandwidth limitations of subthreshold operation, is to design filters using the lateral bipolar device inherent in standard CMOS processes. While the characteristics of the lateral bipolar transistor have traditionally lagged far behind the vertical transistor, the continually decreasing dimensions of CMOS technology have made the lateral device increasingly more attractive. The development of log-domain filters in CMOS technology using lateral bipolar transistors shall be the subject of this dissertation.

The outline of this chapter is as follows: the first section will provide a description of the evolution of the log domain filter as it pertains to this work. The next section will present an introduction to the concepts of log domain filtering, and will provide an overview of a log-domain filter structure and implementation. The final section will discuss the organization of this thesis and provide an outline of its contents. A brief historical background shall be provided to begin.

1.2 - A Historical Background

The concept of the log-domain filter was originally proposed by Adams and introduced to the Audio Engineering Society in 1979 [2]. Adams had developed a method by which the resistor in an RC filter could effectively be replaced with a diode, a non-linear element. By controlling the bias current of the diode, the cutoff frequency of the filter could be electronically tuned over several decades. Adams described the discovery as "a circuit, composed of both linear and non-linear elements, which, when placed between a log converter and an anti-log converter (in the "log domain"), will cause the system to act as a linear filter".

The technique introduced by Adams did not receive significant attention until 1993, when Frey [3] proposed a formal procedure for synthesizing log-domain filter

functions. The method developed by Frey introduced state-space matrices as a means to describe the operation of the filter. Frey demonstrated the technique with the design of a biquadratic log-domain filter and a seventh order Chebychev filter, implemented as a cascade of biquadratic stages.

A more intuitive procedure for synthesizing log-domain filter functions was proposed by Perry and Roberts [4], [5] in 1995. The method introduced signal-flow graphs as a means to describe the operation of the filter, from which common filter design techniques, such as the operational simulation of LC ladders [6], could be applied. Such techniques can be used to simplify the filter design procedure, and can readily be extended to high-order systems. At the heart of this filter design approach is a circuit referred to as an integrator, or in this case, a "log-domain" integrator. Note that the signal flow graph, the method of operational simulation, and the concept and design of the log-domain integrator shall be described in detail and will figure prominently throughout this work.

Numerous implementations of bipolar log-domain integrators have been described in the literature. One of the earliest such integrators was introduced by Seevinck [7] in 1990. Though developed independently of the work by Adams or Frey, Seevinck described "a companding current-mode integrator", a circuit which performed logarithmic compression on input signals and exponential expansions on output signals, yet overall performed a linear integration, conforming very closely to the paradigm of a log-domain filter. Subsequently, many integrator implementations have been described in the literature, and several are described in detail in [1]. Of particular interest will be an NPN-only, low voltage integrator introduced by El-Gamal and Roberts [8], which shall form the basis for the integrator developed in Chapter 3 of this work.

The performance of high-order log-domain filters has been well reported in the literature. Among them, Frey has reported a high-frequency second-order bandpass filter [9], shown to be capable of operation at over 400 MHz. A low-power third-order BiCMOS filter, reported by Punzenberger and Enz [10], has been shown to be capable of being tuned over many decades of frequency, with a maximum frequency of about 10 MHz, while operating from a 1.2 V supply. The NPN-only integrator mentioned in the previous paragraph has been

used by El-Gamal et. al. [11] in the design of a high-frequency third-order filter, shown to be capable of operation at up to 100 MHz while operating from a 1.2 V supply.

Of particular interest in this thesis is the implementation of log-domain filters in CMOS technology. One of the first such implementations was reported by Toumazou et. al. [12] in 1994. In this work, Toumazou described a second order low-pass filter which made use of MOSFETs operating in weak inversion, intended for use in a micropower biomedical application. More recently, many papers have been devoted to the subject of CMOS log domain filters. Those which provide an experimental verification of their findings, however, are relatively few in number [13]-[19]. A comparison of the experimental results in previously published papers with respect to the filter performance attained in this work will be provided at the end of Chapter 4.

The vast majority of log-domain research in CMOS technology to this point has focused on the use of the MOS transistor operating in its subthreshold region [12]-[18], and therefore this research has been confined to low power and relatively low frequency implementations. Attempts have been made to extend the concepts of log-domain filters to CMOS circuits according to the square law relationship of a MOSFET transistor operating in saturation. Such an approach was proposed by Frey [20] in 2000. Although this approach may have merits, the methods involved are not straightforward. Circuits for implementing such relationships have been proposed [20], [21] though to date no experimental implementations of these filters have been reported in the literature, and no information on the simulated linearity and distortion of such filters has been provided.

Rather than making use of MOSFET transistors in weak inversion or developing a new system for implementing square law filters, an alternate approach to implementing log domain filters in CMOS technology is to make use of the lateral bipolar device inherently available within the CMOS process. The development of this approach shall be the subject of the subsequent chapters of this work.

1.3 - An Overview of Log-Domain Filtering

A simple explanation of the principle of log domain filtering can be understood in terms of the diode - capacitor circuit first described by Adams, as shown in Figure 1.1. If one assumes that the current flowing through the diode can be expressed by a simple exponential function, the differential equation describing the operation of this circuit could be expressed as

$$e^{(V_I - V_O)} = C\frac{d}{dt}(V_o) \ , \tag{1.1}$$

which can be rewritten as

$$e^{V_I} = C\frac{d}{dt}(e^{V_O}) \ , \tag{1.2}$$

or written in integral form as

$$e^{V_O} = \frac{1}{C}\int e^{V_I} dt \ . \tag{1.3}$$

This circuit does not implement a linear integrator in terms of the input and output voltages V_I and V_O. However, if these variables were replaced by X_I and X_O, according to

$$V_I = \ln(X_I) \ , \quad V_O = \ln(X_O) \ , \tag{1.4}$$

then Eqn. (1.3) could be rewritten as

$$X_O = \frac{1}{C}\int X_I dt \ . \tag{1.5}$$

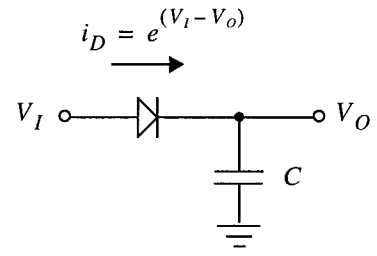


Figure 1.1 A simple log-domain integrator

Therefore, by logarithmically compressing the signal X_I according to Eqn. (1.4) to obtain V_I and the circuit input and by exponentially expanding V_O according to the inverse of Eqn. (1.4) to obtain X_O at the circuit output, a linear integration can be implemented. Such a means of expansion and compression is readily available in the form of the voltage to current relationship of the diode equation itself. In this case, the desired input and output signals, X_I and X_O, are in fact currents, and the integration which is taking place is performed on logarithmically compressed signals, or put another way, in the "logarithmic domain".

Though the advantages of doing so are not immediately obvious, it can be shown that the constant of integration (not included in the previous analysis) can be designed to be proportional to the bias current in the diode. Therefore, the cut-off frequencies of filters designed with such an integrator can be electronically tuned, in this particular case over a range of many decades. In addition, the capacitor storage element for this integrator is subject to signals which have undergone logarithmic compression, and therefore the theoretical dynamic range of the integrator can be very large. Furthermore, this system requires no feedback in order to linearize the response of its components; rather, the inherent non-linearity of its elements are used to its advantage. Each of these features make this simple integrator both intriguing and potentially very useful.

In Chapter 3, a more rigorous mathematical approach to the development of a log-domain will be presented, though the underlying principles will remain the same. Rather than a diode, a bipolar PNP transistor, with a logarithmic / exponential voltage to current relationship given by

$$I_C = I_S e^{V_{BE}/v_T} \tag{1.6}$$

will be used to implement the integrator to be used in this work.

A generic block diagram for a log domain filter is shown in Figure 1.2. This filter is composed of three distinct sections: an input compression stage, a filter stage, and an output expansion stage. Voltage to current conversion and logarithmic compression are

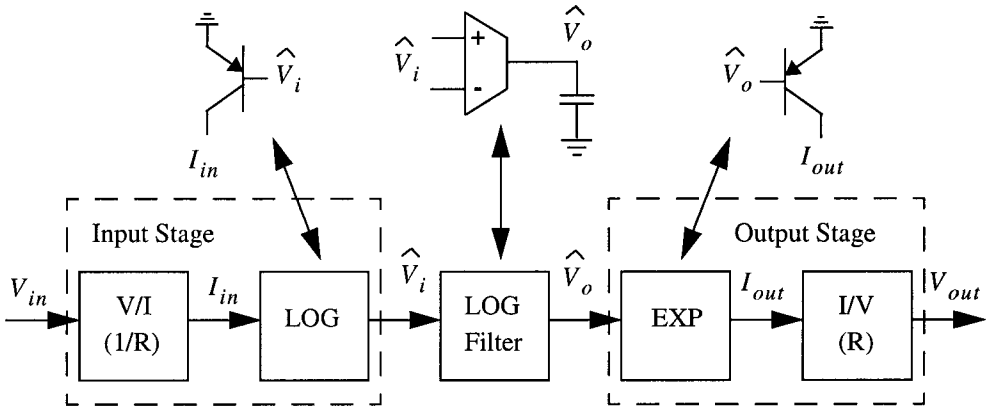


Figure 1.2 Block diagram of a log-domain filter

performed in the first stage, as shown by the progression of the V_{in}, I_{in}, and $\hat{V}_i$ signals in the figure. The V/I conversion ratio is represented by *1/R* in the figure, and the logarithmic compression is performed by means of a bipolar transistor. Filtering (in the logarithmic domain) is performed in the second stage. The symbol for the log-domain integrator, the basic building block for the filter, is drawn in the figure. Exponential expansion and I/V conversion are performed in the final stage, as shown by the progression of $\hat{V}_o$, I_{out}, and V_{out} signals. Exponential expansion is once again performed by means of a bipolar transistor, and the I/V conversion ratio is represented in the figure by R. Each of the blocks shown above will be described in detail in this work.

1.4 - Thesis Outline

The development of log-domain filters in CMOS technology using lateral bipolar transistors shall be the subject of this dissertation. The presentation in this work will be organized according to three distinct levels of hierarchy. The first of the three shall be an investigation at a device level, where a characterization of the lateral PNP transistor will be performed. The second shall be an investigation at a circuit level, where the design of a log-domain integrator and associated circuitry will be developed. The third shall be an investigation at a system level, where the implementation of an entire log-domain filter will be described in detail.

Following this outline, Chapter 2 will describe the characterization of a lateral PNP transistor in a standard 0.35μ CMOS process. The structure and layout of the transistor will be presented, and a SPICE-compatible circuit model for the device will be developed. Techniques for determining the device parameters and physical insights into the device operation shall be described, and a comparison of the modelled and measured low frequency response of the transistor shall be provided.

Chapter 3 will describe the development of a log-domain integrator which makes use of these lateral PNP devices. The theoretical background required to understand the operation of a log-domain integrator will be provided and the methodology of mapping the log-domain integrator from bipolar into CMOS technology will be presented. The simulated and experimentally measured integrator response shall be compared, demonstrating some of the capabilities and limitations of this new log-domain filtering approach.

Chapter 4 shall describe the complete implementation of an log-domain filter. The theoretical background required to synthesize second and higher-order filters, based upon on the log-domain integrator, will be provided. The filter synthesis, complete circuit implementation, and experimental characterization of a biqudratic and a third-order elliptic filter will be performed. A comparison of the characteristics of the CMOS log-domain filters developed in this work to other log-domain filter implementations described in the literature will be provided.

As a result of this work presented in these chapters, a first, second, and third order log domain filter will have been thoroughly investigated. The final chapter shall provide conclusions which may be drawn from this work, and will discuss a few future directions for log-domain circuit design in CMOS technology.

Chapter 2 - Modelling Lateral PNP Transistors in CMOS Technology

In order to realize log-domain circuits in CMOS technology, a logarithmic-exponential device such as a bipolar transistor is required. The lateral bipolar transistor, which may be fabricated in a standard CMOS process, can be used for this purpose. However, this device is not in widespread use in CMOS circuit design, and transistor models for the lateral bipolar device are generally not provided by semiconductor manufacturers. In this chapter, a SPICE compatible model for a lateral PNP transistor, fabricated in 0.35μ CMOS technology, will be presented.

Keeping the lateral PNP model as simple as possible has been one of the key motivations of this work. Therefore, the number of parameters used to describe the device behaviour has been kept to a minimum. Furthermore, each of the parameters can be either determined from physical considerations, extracted from straightforward device measurements, or adopted from standard information provided by the manufacturer. The model can therefore be readily developed within any CMOS process.

The outline of this chapter is as follows: the first section will describe the lateral PNP transistor structure and will discuss several device layout considerations. The second section will describe each of the SPICE parameters used in modelling the transistor, and will provide both physical insights into the device operation and techniques for extracting the parameters from measurements where applicable. The final section of the chapter will provide the complete SPICE model for the transistor. The model will form the basis for all the designs and simulations of log-domain filter circuits described in this work.

2.1 - Lateral PNP Transistors: Structure and Layout

In standard n-well CMOS technology, two types of bipolar devices can be fabricated: a vertical PNP transistor and a lateral PNP transistor. A cross sectional diagram of each type of device is shown in Figure 2.1. Note that in an n-well technology, only PNP devices, rather than NPN devices, can be formed.

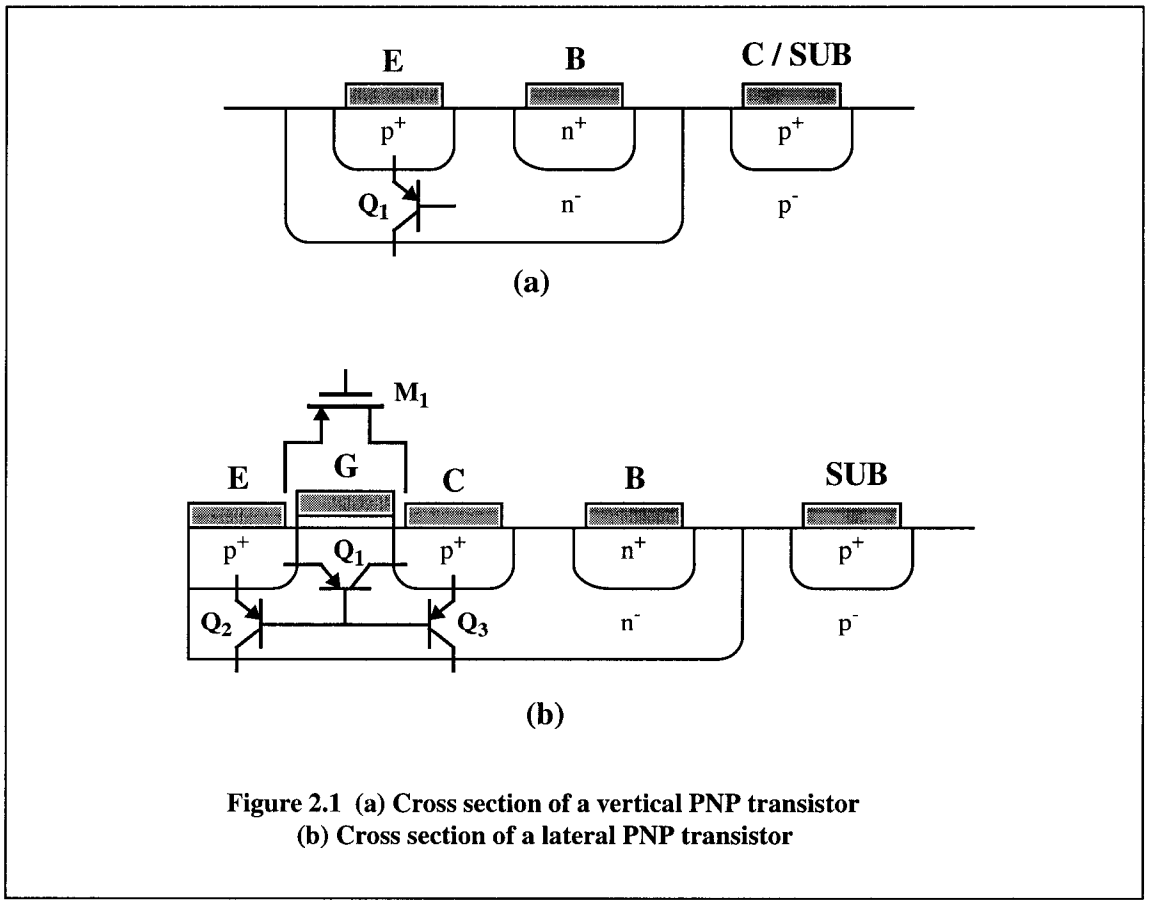


Figure 2.1 (a) Cross section of a vertical PNP transistor
(b) Cross section of a lateral PNP transistor

The vertical PNP transistor is formed using a p^+ diffusion for the emitter, an n-well for the base, and the p^- substrate for the collector, as indicated by Q_1 in Figure 2.1(a). The structure is straightforward, and models for vertical PNP transistors are generally provided by the semiconductor manufacturer. These devices, however, are of limited use for most analog applications since the collector coincides with the substrate of the chip.

The lateral PNP transistor is formed using the structure of a PMOS transistor. The p^+ diffusions of the source and drain of the PMOS transistor are used to form the emitter and collector of the device, while the lightly doped n-well region under the gate of the PMOS transistor is used to form the base of the lateral device, as indicated by Q_1 in Figure 2.1(b). However, by the nature of this structure, three undesired devices are also present: two other parasitic vertical bipolar transistors (Q_2-Q_3), and the original PMOS transistor (M_1) used in forming this lateral device.

The model of the behaviour can be simplified if the structure is operated with the gate terminal connected to a sufficiently large positive potential, thereby ensuring that the PMOS transistor (M_1) is off. The modelling can be further simplified by observing that the contribution of the second parasitic vertical bipolar transistor (Q_4) will be minimal if the lateral bipolar device (Q_2) is kept from operating deeply into saturation. The behaviour of this structure can therefore be modelled adequately by including only the two remaining devices, shown schematically in Figure 2.2(a) and symbolically in Figure 2.2(b). This two transistor configuration will form the basis for the lateral PNP model described in this chapter.

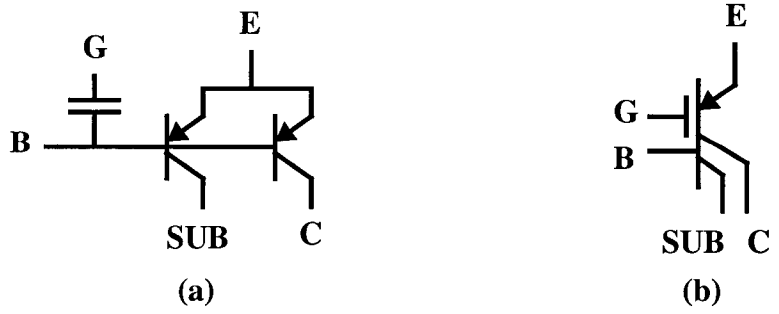


Figure 2.2 (a) Schematic and (b) Symbolic representation of a lateral PNP device

Before discussing the specifics of the modelling, several layout considerations should be mentioned. First, lateral PNP transistors are conventionally laid out in circular fashion, with the emitter at the centre. This improves the injection efficiency, since the emitter is entirely enclosed by the collector, and serves to keep the injection uniformly distributed, since the device is symmetric. Secondly, the lateral emitter injection is, to a first approximation, proportional to the emitter perimeter, which scales with the diameter, while the vertical emitter injection is, to a first approximation, proportional to the emitter area, which scales with the square of the diameter. To maximize the ratio of lateral to vertical collector current, the diameter of the emitter should therefore be kept to a minimum. Finally, note that base width of the lateral device is set by the gate length of the original PMOS transistor. In order to maximize the current gain of the lateral device, the gate length should be kept to a minimum. The layout of a typical lateral PNP device, fabricated in 0.35μ CMOS technology, is shown in Figure 2.3.

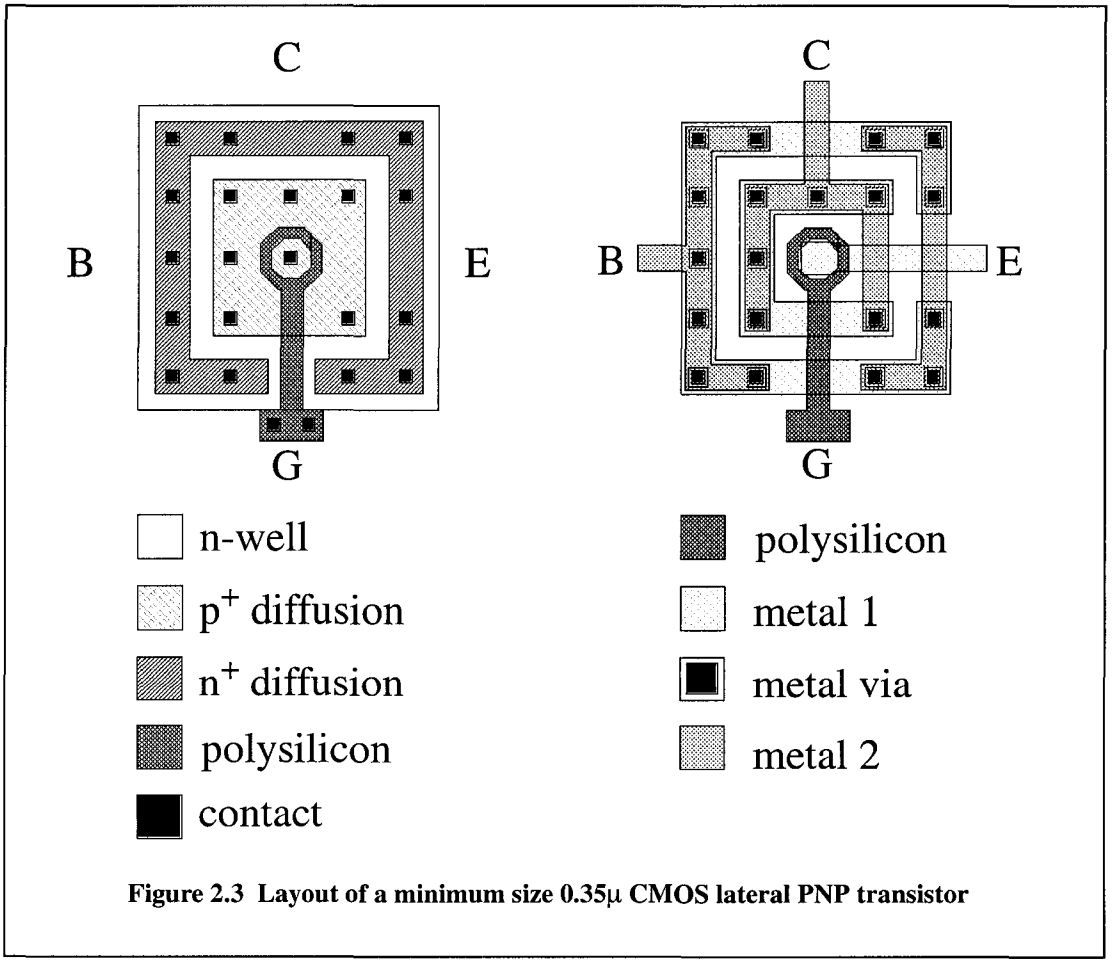


Figure 2.3 Layout of a minimum size 0.35μ CMOS lateral PNP transistor

2.2 - Lateral PNP Transistors: SPICE Model Parameters

A two-transistor SPICE compatible model as shown in Figure 2.2 has been developed for the 0.35μ CMOS lateral PNP transistor as shown in Figure 2.3. The number of parameters used to describe the device behaviour has been kept to a minimum (a total of fourteen SPICE parameters and one additional capacitance) with the intention that the model should be sufficiently simple to be readily developed in any CMOS process. Low frequency parameters have been measured or fitted directly, while AC parameters and parasitic parameters have been adapted from existing modelling information provided by the manufacturer. A listing of each of the SPICE parameters used in developing this model are given in Table 2.1. A detailed description of these parameters can be found in several references, including [22] and [23]. Previous work in developing SPICE models for lateral bipolar transistors can be found in [24] and [25].

Table 2.1:SPICE Parameter Listing

SPICE Parameter	Parameter Description (Common Usage Name in Brackets)
IS	Saturation Current (I_s)
NF	Forward Emission Coefficient (n_F)
BF	Maximum Forward Current Gain (β)
VAF	Forward Early Voltage (V_A)
IKF	Forward Knee Current (I_{KF})
RE	Ohmic Emitter Resistance (R_E)
RB	Ohmic Base Resistance (R_B)
TF	Forward Base Transit Time (τ_F)
CJE	Zero Bias Base-Emitter Junction Capacitance (C_{je})
VJE	Base-Emitter Junction Built-In Potential (ϕ_{je})
MJE	Base-Emitter Junction Grading Coefficient (m_{je})
CJC	Zero Bias Base-Collector Junction Capacitance (C_{jc})
VJC	Base-Collector Junction Built-In Potential (ϕ_{jc})
MJC	Base-Collector Junction Grading Coefficient (m_{je})

One of the most significant complications in developing a model for the lateral PNP transistor stems from the fact that the lateral and vertical devices, which share emitter and base regions, do not operate independently of one another, as would be assumed by the two transistor model presented in Figure 2.2(a). This problem manifests itself in two ways. First, when making transistor measurements, the parameters of one device may depend on the bias conditions of the other device. For example, the vertical collector current has been observed to have a dependence on the voltage bias of the lateral collector-base junction. Secondly, when measuring certain device quantities, the contribution of the lateral and vertical devices cannot be distinguished from one another. For example, the base currents of the lateral and vertical devices cannot be separated, since they are connected though one common terminal. To alleviate the first of these problems, the transistors have been modelled using bias conditions which most closely resemble those under which the devices will operate in log-domain filter applications. To alleviate the second problem, reasonable approximations have been made when quantities cannot be directly measured. Comparison of measured values with first order physically-based models have been used for this purpose whenever possible.

Another significant complication in developing a model for the lateral PNP transistor stems from the relatively light doping of the n-well in this 0.35μ CMOS process. The doping concentration of the n-well, which is used to form the base of the transistor, on the order of 5×10^{16} cm^{-3} (see the listing in the Appendix), which is approximately a factor of ten lower than would be the case in a standard bipolar process [26]. The light doping in the base affects the transistor behaviour in several ways, and will be given particular attention as the transistor model is presented.

The following sections of this chapter will describe the SPICE model parameters of Table 2.1, including the physical origins of each parameter as well as the parameter measurement techniques where applicable. The theoretical background presented this chapter has been compiled from [22], [26]-[29]. Additional information on lateral bipolar transistors, including detailed discussions of the devices physics, can be found in [24], [30] and [31].

Each of the parameter values developed in this section will be used in a final model optimization, which will be described in Section 2.3 at the end of the chapter.

2.2.1 - Saturation Current (I_S)

The saturation current (I_S) is one of the most fundamental parameters in the operation of a bipolar transistor. For a PNP device, the collector current is determined from I_S according to

$$I_C = I_S \cdot e^{\frac{V_{EB}}{v_T}} \tag{2.1}$$

where I_C represents the collector current, V_{EB} represents the emitter-base voltage, and v_T represents the thermal voltage. This section of the chapter will provide a brief theoretical derivation of the saturation current (which will be referenced throughout the chapter) and will present a comparison between the theoretically modelled and experimentally measured collector currents for the lateral PNP devices.

A first order model of collector current can be developed by assuming that the current arises entirely from the diffusion of holes (the minority carrier) through the base from the emitter to the collector of the device. This diffusion current can be expressed as

$$i_p = qA_{EB}D_p\frac{dp_n}{dx} \tag{2.2}$$

where i_p represents the hole diffusion current, q represents the charge of an electron, A_{EB} represents the effective area of the emitter-base junction, D_p represents the diffusion constant for holes in the base, and $\frac{dp_n}{dx}$ represents the gradient of the concentration of holes in the direction from the emitter to the collector.

If one assumes that negligible carrier recombination occurs in the base (a valid assumption given the light base doping of these devices) the concentration of holes can be approximated as varying uniformly between the emitter-base junction and the base-collector junction. The gradient of the concentration can therefore be expressed as

$$\frac{dp_n}{dx} = \frac{p_{n(ebj)} - p_{n(bcj)}}{W_B} \approx \frac{p_{n(ebj)}}{W_B} \tag{2.3}$$

where $p_{n(ebj)}$ and $p_{n(bcj)}$ represent the hole concentration on the n-doped side of the emitter-base junction and collector-base junction respectively, and W_B represents the effective width of the base. Under normal operating conditions, the concentration of holes at the reversed biased base-collector junction is approximately zero, and therefore $\frac{dp_n}{dx}$ is directly proportional only to the concentration of holes in the base at the emitter-base junction, as indicated by the approximation in Eqn. (2.3).

For low to moderate levels of emitter-base voltage, the concentration of holes at the emitter-base junction will equal the rate of injection of holes from the emitter, given by

$$p_{n(\text{ebj})} = p_{no} \cdot e^{\frac{V_{EB}}{v_T}} \tag{2.4}$$

where p_{no} represents the equilibrium hole concentration in n-doped base, V_{EB} represents the forward bias placed across the emitter-base junction, and v_T represents the thermal voltage. Since holes are the minority carrier, the hole concentration can be expressed in terms of the majority carrier concentration, which at low levels of injection is equal to the doping concentration of the base. Therefore p_{no} can be replaced by n_i^2/N_B, where n_i is the intrinsic carrier concentration of silicon and N_B represents the doping concentration in the base. The collector current can therefore be expressed by combing equations (2.2), (2.3), and (2.4) to give

$$I_C = \frac{qA_{EB}D_p n_i^2}{N_B W_B} \cdot e^{\frac{V_{EB}}{v_T}} = I_S \cdot e^{\frac{V_{EB}}{v_T}} \tag{2.5}$$

where the saturation current, I_S, is defined according to Eqn. (2.5), as is found in several references [27]-[26]. This parameter is also often defined as the value of collector current when V_{EB} is set equal to zero.

From this definition, it is possible to estimate a theoretical value of I_S for both the lateral and vertical PNP transistors present in our model. Using the dimensions and physical constants tabulated in the Appendix, the theoretical value of I_S can be calculated to be $2.09 \cdot 10^{-18}$ A for the lateral device and $7.53 \cdot 10^{-19}$ A for the vertical device.

A comparison between the theoretically modelled and experimentally measured collector currents is shown in Figure 2.4. All measurements have been made with V_{CB} fixed at 0 V, the gate to emitter voltage, V_{GE}, set to +0.5 V, and the substrate voltage, V_{SUB}, set to -2 V below the emitter voltage. This biasing arrangement most closely resembles the conditions under which the device will be operated in the intended log-domain filter applications. The experimental values shown here represent the average of six measurements: two independent sets of measurements each from three lateral bipolar devices, each device originating in a different silicon chip.

As is shown, there are significant deviations between the modelled and measured collector currents. The decrease in collector current for large values of base-emitter forward bias can be attributed to high-injection effects and parasitic base and emitter resistance. These effects will be addressed and modelled in Section 2.2.5 and Section 2.2.6. There are also significant deviations in lateral collector current at low values of base-emitter voltage, and in particular, there is a variation in the slope between the modelled and measured lateral collector current curves. This effect is difficult to model theoretically, and has been accounted for empirically using the forward emission coefficient, n_F, which will be discussed in the next section.

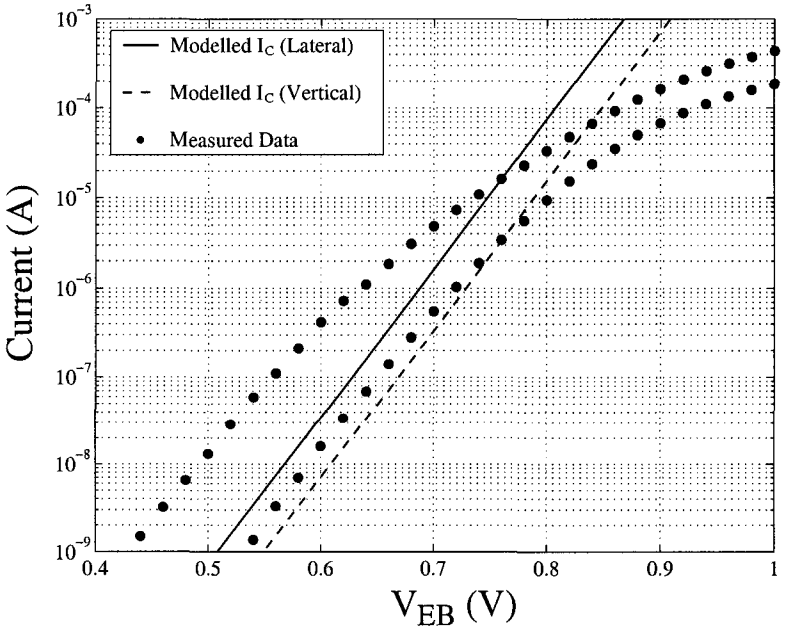


Figure 2.4 Comparison of Eqn. (2.5) and experimentally measured collector currents

2.2.2 - Forward Emission Coefficient (n_F)

In order to compensate for the difference between the theoretical and experimental collector currents at low values of base-emitter forward bias, a second parameter, the forward emission coefficient (n_F) needs to be introduced. The forward emission coefficient for a PNP transistor is defined in [22] and given by

$$\frac{1}{n_F} = \frac{v_T}{I_c} \cdot \left. \frac{dI_C}{dV_{EB}} \right|_{V_{CB}=0} \tag{2.6}$$

and is incorporated into the calculation of collector current according to

$$I_C = I_S \cdot e^{\frac{V_{EB}}{n_F v_T}}. \tag{2.7}$$

In most modern bipolar devices, the value of n_F is very close to unity and therefore this parameter is often omitted in device models. However, due to the relatively low doping concentration in the n-well in the 0.35μ CMOS process used here, this variable must be included. This section will provide a brief explanation of the physical mechanism which gives rise to the need to model n_F, and will describe the curve-fitting technique used to empirically determine n_F from experimental data.

When a low forward bias is placed between the base and emitter, a depletion region exists on either side of base-emitter junction. The penetration of the depletion region into the base, W_{DR}, at a zero volt forward bias can be approximated, using equations given in [27], according to

$$W_{DR} = \left(\frac{2\varepsilon V_o}{qN_D(1 + N_D/N_A)} \right)^{1/2} \tag{2.8}$$

where V_o represents the built-in potential of the junction (approximately 0.9 V), V_f is the forward bias across the emitter-base junction, N_A and N_D are the doping concentrations on the emitter and base sides of the junction respectively, ε represents the permittivity of silicon and q represents the charge of the electron. The resulting penetration of the lateral

emitter-base depletion region is approximately 0.12μm for a zero-volt forward bias. The penetration will approach zero as the forward bias approaches the built-in potential.

This modulation of the base, which amounts to slightly over 1/3 of the entire base width, is similar, although inverse, to the Early effect (see Section 2.2.4) and has been facetiously referred to as the Late effect [22]. This modulation leads the collector current to be significantly higher than would be predicted by first order theory, specifically at low values of forward bias. This effect is difficult to model accurately, particularly with the geometries involved in these lateral devices. However, because the effect is so pronounced in this case, it must be accounted for. In general, the technique for compensating for the Late effect is to empirically model the collector current using the forward emission coefficient, n_F.

To perform an empirical fit, Eqn. (2.7) can be rearranged into the form y = mx + b,

$$\ln(I_C) = \left(\frac{1}{n_F v_T}\right) v_{EB} + \ln(I_S) \tag{2.9}$$

and values of n_F and I_S extracted from the slope and y-intercept of plot, respectively. Best fit curves for both lateral and vertical devices have been made using collector currents measured below V_{EB} = 0.7 V. This was done to avoid including high injection effects which become a significant factor at approximately V_{EB} = 0.8 V (see Section 2.2.5). The resulting empirically calculated parameters are $I_S = 1.20\times10^{-15}$ A and n_F = 1.19 for the lateral device, and $I_S = 2.75\times10^{-18}$ A and n_F = 1.03 for vertical device. The empirically modelled collector currents, plotted with the experimentally measured currents, are shown in Figure 2.5.

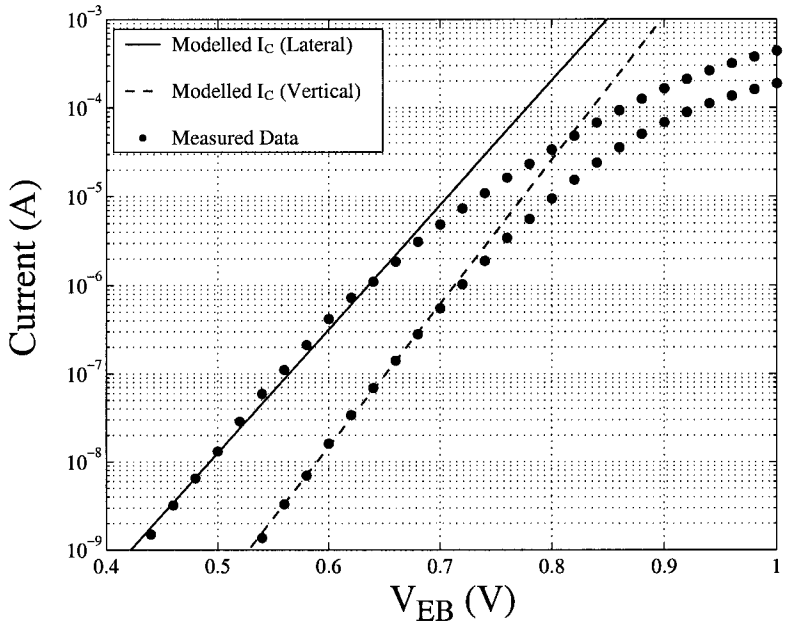


Figure 2.5 Empirical Fitting of I_S and n_F to experimentally measured currents

Note that the derivation given by Eqn. (2.2) to (2.5) remains a valid model for I_S. Between the regions of operation in which the Late effect and the high current injection and resistive effects dominate, Eqn. (2.5) can still be used to provide a reasonable estimate of I_S, and the derivations in Eqn. (2.2) to (2.5) will be used in later sections to derive reasonable theoretical quantities for parameters such as I_{KF} and β, as described in upcoming sections. However, for the purpose of accurately capturing the collector current at low forward bias, the empirical values of I_S and n_F will be taken as the SPICE parameters. These parameters will be used as the starting point in the final model optimization, to be described in detail in Section 2.3.

2.2.3 - Forward Current Gain (β)

The maximum forward current gain, β, is a fundamental parameter in the operation of a bipolar transistor. It is also a parameter which has been shown to have a significant impact on the performance of log-domain filters [32]. The value of β is defined simply as ratio of collector to base current,

$$\beta = I_C / I_B \,. \tag{2.10}$$

This section will provide a derivation of the theoretical value of β and will provide (by examining the resulting base currents) a comparison between the theoretically modelled and experimentally measured values of β for these lateral PNP devices.

In most modern bipolar transistors, the dominant mechanism which gives rise to base current is the injection of minority carriers (electrons for a PNP transistor) from the base into emitter of the device [28]. In this case the theoretical value the base current can be derived in a similar manner to collector current, defined by Eqn. (2.2) to (2.5). The expression for base current can therefore be expressed by

$$I_B = \frac{qA_{EB}D_n n_{ie}^2}{N_E W_E} \cdot e^{\frac{V_{EB}}{v_T}} \tag{2.11}$$

where N_E and W_E are the doping concentration and effective width of the emitter, and n_{ie} is the effective intrinsic concentration in the emitter.

In deriving this expression, it is important to distinguish the effective intrinsic concentration, n_{ie}, used in Eqn. (2.11), from the intrinsic concentration, n_i, used in Eqn. (2.5). In 0.35μ CMOS technology, the emitter is degenerately doped (that is, the doping level is sufficiently high that the Fermi level moves into the valence band for a p-type semiconductor, or into the conduction band for an n-type semiconductor). Therefore, the effective energy bandgap of a degenerately doped semiconductor is decreased by an amount ΔE_g, leading to an effective intrinsic concentration given by

$$n_{ie}^2 = n_i^2 e^{\left(\frac{\Delta E_g}{kT}\right)} \tag{2.12}$$

where k represents Boltzman's constant and T represents temperature [26]. The effective energy bandgap in the emitter is reduced by 0.125 eV, leading to an effective intrinsic concentration of 1.68×10^{11} cm^{-3}.

An expression for the theoretical value of β can be found by combining Eqn. (2.11) with Eqn. (2.5) to give

$$\beta = \frac{I_C}{I_B} = \frac{N_E W_E D_p n_i^2}{N_B W_B D_n n_{ie}^2}. \tag{2.13}$$

as stated in [28]. Using the dimensions and constants from Appendix, the theoretical value of β can therefore be calculated to be β = 58 for the lateral device and β = 8 for the vertical device.

A comparison between the theoretically modelled and experimentally measured values of β is shown in Figure 2.6. All measurements have been made with V_{CB} = 0 V, V_{GE} = +0.5 V, and V_{SUB} = -2 V, and the measurements again represent the average of three individual devices. Since the base currents for the lateral and vertical devices cannot be independently measured in practice, the base currents shown in the figure are the sum of the contributions from both devices. Therefore, the accuracy of the theoretical value of β is represented by the comparison of the theoretical and measured base currents.

The theoretical values of β = 58 and β = 8 have been used to calculate the theoretical base current, as shown by the solid line in the figure. The agreement between the theoretical and measured base currents is reasonable. An improved empirical fit, based on increasing each value of β (while preserving the approximate ratio of lateral and vertical current gain) to β=150 and β=20, is shown by the dotted line in the figure. The increased empirical values will be used as the starting point in the final model optimization.

Note that neither curve accounts for the decrease in collector current for large values of base-emitter forward bias. This decrease can be attributed to high-injection effects and parasitic resistances, and will be addressed in Section 2.2.5 and Section 2.2.6.

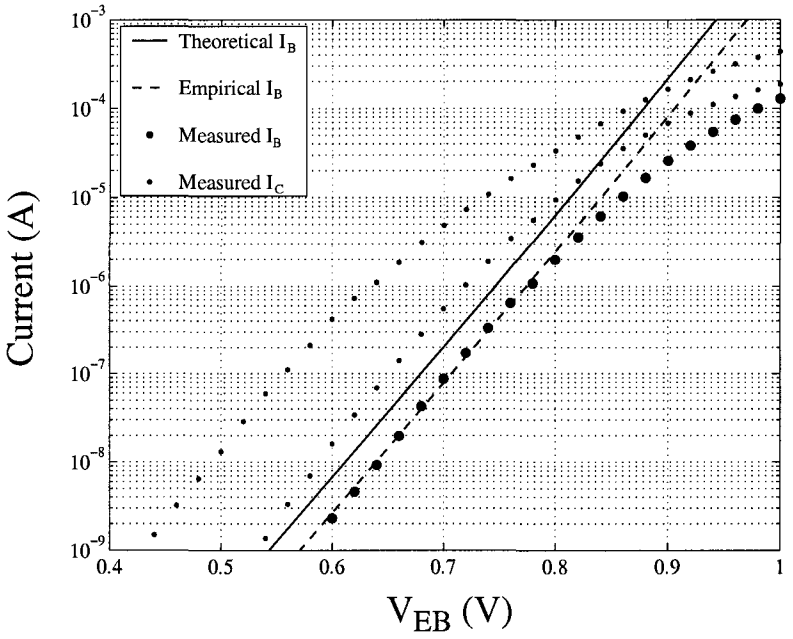


Figure 2.6 Comparison of modelled and measured base and collector currents

2.2.4 - Early Voltage (V_A)

The Early voltage (V_A) is a fundamental parameter in the operation of a bipolar transistor. It is also a key parameter which has been shown to have a significant impact on the performance of log-domain filters [32]. The Early voltage for a PNP transistor is defined as

$$V_A = \left(\frac{1}{W_B} \cdot \left. \frac{dW_B}{dV_{CB}} \right|_{V_{CB=0}} \right)^{-1} \tag{2.14}$$

where W_B represents the base width, and V_{CB} represents the voltage across the collector-base junction [22]. A more common expression for Early voltage is given by

$$V_A = \frac{I_C}{r_o} \tag{2.15}$$

where r_o represents the effective output resistance of the transistor. This section will provide a brief derivation of a theoretical value of V_A, will describe some of the differences observed between the first order theory and the measured results, and will describe the technique used to empirically determine V_A from experimental data.

The Early voltage is used to model the variation in the width of the depletion region at the base-collector junction as a function of the base-collector bias voltage. This variation modulates the effective width of the base, giving rise to variation in collector current. An approximation of the Early voltage can be found by relating the derivative in Eqn. (2.14) to the base-collector junction capacitance according to

$$qN_B \cdot \frac{dW_B}{dV_{CB}} = c_{BC} \tag{2.16}$$

where c_{BC} represents the base-collector junction capacitance per unit area, which can in turn be described as C_{BC}/A_{BC}, the entire base-collector junction capacitance divided by the total effective base-collector junction area. The Early voltage can therefore be appoximated as

$$V_A = \frac{qN_B W_B A_{BC}}{C_{BC}} \tag{2.17}$$

as given in [28]. Using the parameters tabulated in the Appendix, the theoretical value of V_A would be 2.4 V for the lateral device and 76 V for the vertical device. The expected value for the lateral device is extremely (and somewhat unrealistically) low, but demonstrates important relationships, both resulting from the relatively low base doping of these devices. First, since the Early voltage is proportional to N_B, the value of V_A should be expected to be very low when a lightly doped n-well is used to form a base, as is the case here. Second, the Early voltage is proportional to W_B, and therefore the "Late effect" as described in Section 2.2.2 can be expected to have an impact on the measured value of V_A. This effect is demonstrated below.

A comparison of experimentally measured collector currents, taken at two values of collector-base voltage, is shown in Figure 2.7. The dark data points in the figure represent measured currents with V_{CB} = 0 V at the lateral junction, while the light data points represent the currents with V_{CB} = -1 V. The lateral base width modulation which results from the increased reverse bias is reflected in the figure by the percentage change in the lateral collector current. The percentage change can be seen to vary over the range of V_{EB}, being most pronounced at low values of forward bias (when the base-emitter depletion region penetration is at its maximum). As a result, the measured value of V_A, which would normally be assumed to be a constant, is in fact an increasing function of V_{EB}.

It is also worth noting that there is a second and somewhat surprising effect shown by Figure 2.7. The increase in lateral collector current (due to the reverse bias on the lateral junction base collector junction) is accompanied by a decrease in vertical collector current. The two transistor model of Figure 2.2 would assume the complete independence of the two devices, which is shown here not to be an entirely accurate assumption.

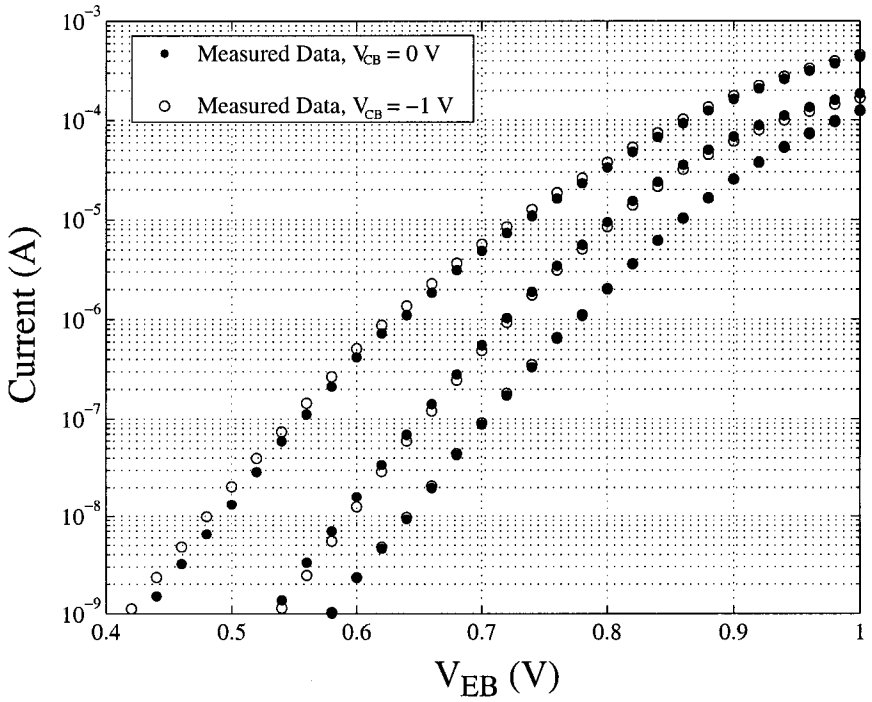
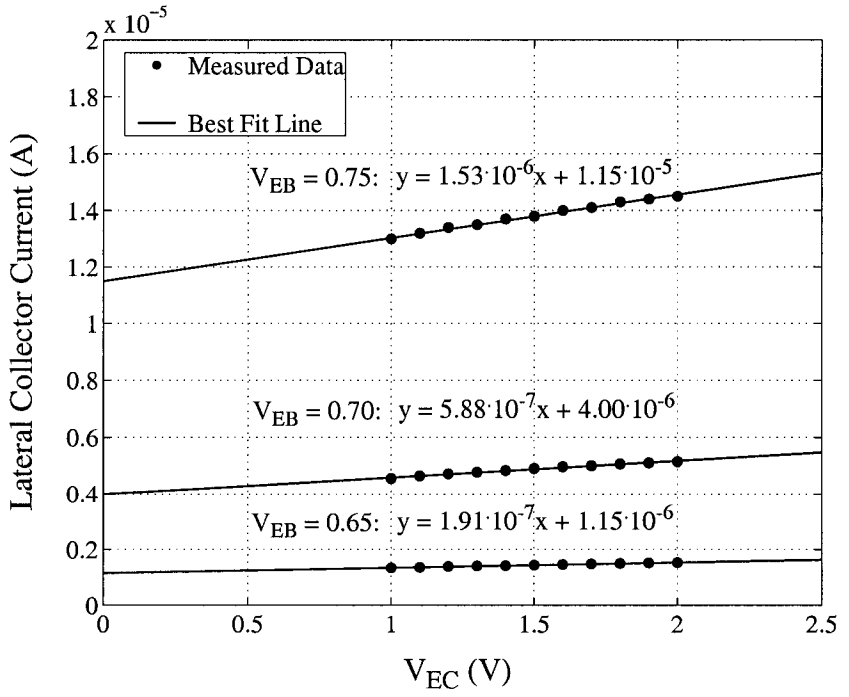


Figure 2.7 Measured base and collector currents with V_{CB} = 0 V and V_{CB}= -1 V

Neither of these effects can be adequately captured with a simple first order model. In the interests of model simplicity, a constant value of V_A, measured at the operating point V_{EB} = 0.7 V, has been used. Measured lateral collector currents, plotted as a function of V_{EC} for three values of V_{EB}, are shown in Figure 2.8. Each curve once again represents the average measurements taken from three individual devices. Best-fit curves have been included in the figure. The value V_A can be extracted from the x-intercept of these best-fit curves. A summary of the extracted values of V_A for V_{EB} = 0.6V to V_{EB} = 0.8V is also provided in the figure. The Early voltage can be seen to be an increasing function of V_{EB} forward bias.

The value of Early voltage for the vertical device can be found in a similar manner shown in Figure 2.7. However, since the vertical collector is formed by the substrate, and since the substrate voltage is normally fixed, the value of V_A for the vertical device itself is not a critical parameter to model. It has been measured at V_A = 40V. The two measured values of V_A, 6.8 V for the lateral device and 40 V for the vertical device, will be taken for the final device optimization.



V_{EB} (V)	V_A (V)
0.60	4.94
0.65	6.02
0.70	6.80
0.75	7.52
0.80	8.25

Figure 2.8 Measured collector currents vs V_{EC}

2.2.5 - Forward Knee Current (I_{KF})

The forward knee current (I_{KF}) is a fundamental parameter used to model high-injection effects in a bipolar transistor. High injection effects, along with the presence of parasitic emitter and base resistances, are largely responsible for the collector current roll-off at large values of V_{EB}, as has been noted in the previous sections. This section will provide a brief derivation of a theoretical background to high injection effects and will describe some of the considerations used in determining the value of I_{KF}.

The onset of high injection occurs when the minority carrier concentration injected into the base of the device becomes equal to the equilibrium majority carrier concentration in the base [28]. Due to charge neutrality, the majority carrier concentration at the base-emitter junction will be increased by an amount equal to the injected minority carrier concentration. This leads to a non-uniform distribution of majority carriers in the base, which in turn leads to an internal electric field being formed across the base region. The derivation of the expression for collector current, as given in Eqn. (2.2) to Eqn. (2.5), must be modified to include the effect of this electric field.

The previously derived expression for collector current, repeated here for convenience, is given by

$$I_C = \frac{qA_{EB}D_p n_i^2}{N_B W_B} \cdot e^{\frac{V_{EB}}{v_T}} \tag{2.18}$$

while the expression for collector current including high injection effects is given by

$$I_C = \frac{2qA_{EB}D_p n_i}{W_B} \cdot e^{\frac{V_{EB}}{2v_T}} . \tag{2.19}$$

Note in particular the factor of two in the denominator of the exponent in the second equation. The voltage at which these two expressions for collector current coincide, shown graphically in Figure 2.9, can be found by equating V_{EB} in equations Eqn. (2.18) and Eqn. (2.19), which gives

$$V_{KF} = 2v_T \ln\left(\frac{2N_B}{n_i}\right). \tag{2.20}$$

The corresponding current can be found by substitution of V_{KF} into either collector current expression, which gives

$$I_{KF} = \frac{4qA_{EB}D_pN_Bn_i}{W_B} = I_s\left(\frac{2N_B}{n_i}\right)^2 \tag{2.21}$$

as given in [28]. I_{KF} is the parameter commonly used to model high injection effects in bipolar transistors. From the parameters tabulated in Appendix, the theoretical value of I_{KF} can be calculated to be 145 μA for the lateral device, and 21 μA for the vertical device. The corresponding value of V_{KF} is approximately 0.8 V in each case. The value of each of these parameters is quite low, due largely to the relatively light doping of the base region of these transistors. The fact that theoretical values of I_{KF} and V_{KF} are well within the expected operating regime of these transistors emphasizes the importance of adequately modelling the high injection.

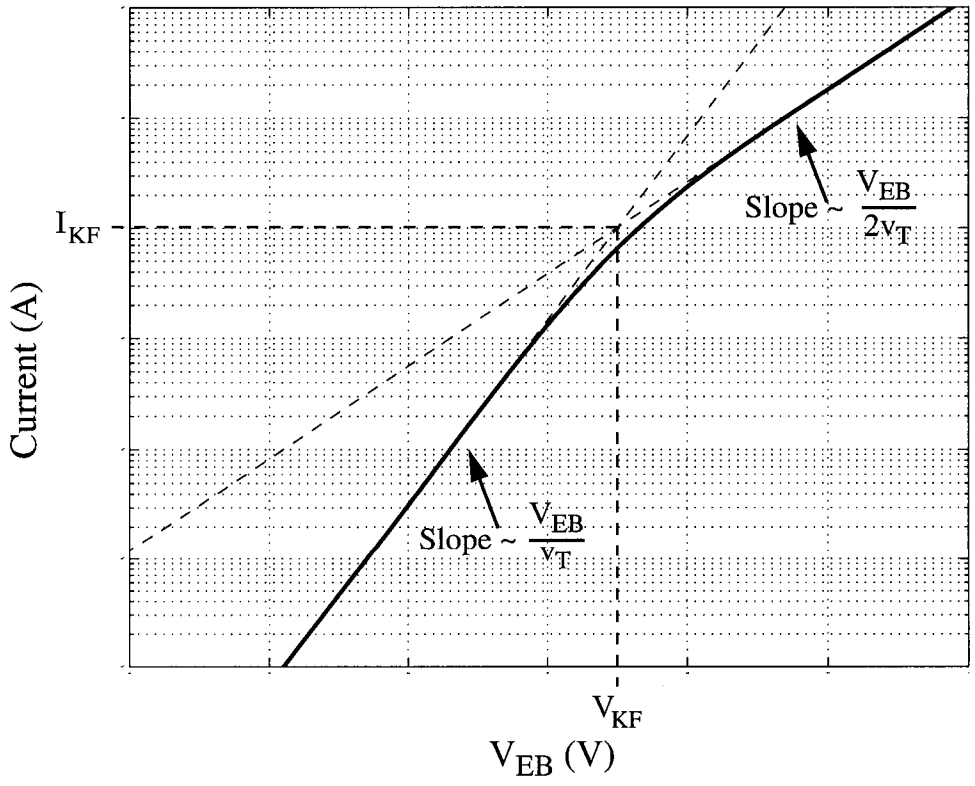


Figure 2.9 Representation of ideal collector current and high-injection effects

A comparison between the theoretically modelled and experimentally measured values of I_{KF} is difficult to make for several reasons. First, the onset of high injection effects are not abrupt, as shown by the dotted lines in Figure 2.9, but is instead gradual, as shown by the solid line of the figure. Second, the exact location of I_{KF} is obscured by the presence of parasitic emitter and base resistances, which also lead to a reduction of collector currents at large values of forward bias. Third, the Late effect, though minimal at the point at which high injection effects occur, does affect the slope of the collector current in the low-injection, which makes the detection of I_{KF} more difficult. Finally, and perhaps most importantly, since the lateral and vertical devices share a common base and emitter, and are observed to interact with one another, it is not clear from a theoretical standpoint whether the two values of I_{KF} can be effectively measured (or calculated) independently of one another as was assumed above. In view of this, the values of I_{KF} = 145 μA for the lateral device and I_{KF} = 21 μA for the vertical device were used as the starting values for the final model optimization, but curve fitting in the high-injection region (which also includes the effect of parasitic resistances) must be used to determine the final values of I_{KF}.

2.2.6 - Emitter and Base Resistance (R_E and R_B)

The emitter and base resistances, R_E and R_B, are important parasitic parameters that must be taken into account in the operation of a bipolar transistor. These resistances are also important since they have been shown to have a significant impact on the performance of log-domain filters [32]. Since both parameters are parasitic, they are better measured experimentally than predicted theoretically. This section will discuss the techniques used for extracting emitter and base resistances and will provide measured estimates of these resistances.

The most common methods for determining emitter and/or base resistances include DC techniques, high frequency and S-Parameter techniques, pulse-measurement techniques, and noise measurement techniques [22]. Given the nature of log-domain applications, and given the complexity of making high frequency and noise measurements, DC measurement techniques are the most practical in this case. The most

common DC techniques for determining emitter and base resistance make use of I_B vs V_{EB} measurement curves, and several variations on this method are described in [33]. The simplest such method [34] is outlined below.

Typical I_B vs V_{EB} characteristics have been shown previously, such as in Figure 2.6. The measured base current deviates from the ideal curve at large values of V_{EB} due primarily to resistive drops across the emitter and base resistances. The voltage generated across these resistances can be expressed as

$$\Delta V_{EB} = [R_B + (\beta + 1)R_E]I_B \tag{2.22}$$

which can be rearranged in the form y = mx + b,

$$\frac{\Delta V_{EB}}{I_B} = \beta \cdot R_E + (R_E + R_B) \tag{2.23}$$

where β is the independent variable. A best-fit curve, measured at lower values of forward bias, can be used to calculate an ideal value for V_{EB} and I_B, from which ΔV_{EB} can be determined. The value of $\frac{\Delta V_{EB}}{I_B}$ can then be plotted versus β, and the values of R_E and R_B extracted. However, note that this method, as with other DC extraction techniques, is made more complicated by the unique two device structure of these transistors. Because the base and emitters of each device are connected through common terminals, the value of I_B, and therefore β, cannot be individually determined. To most accurately estimate the values of R_E and R_B using this method, three different sets of data have been analysed.

For the first two sets of data, an assumption has been made that the total base current can be divided into two equal contributions, attributed to the lateral and to the vertical device. A value of β can therefore be calculated in each case, and Eqn. (2.23) plotted for each device. For a third set of data, the assumption has been made that the two devices can be treated as a single unit. The value of β can therefore be calculated based on the combined base and collector currents, and Eqn. (2.23) plotted once again. All three plots, along with best-fit curves, are shown in Figure 2.10.

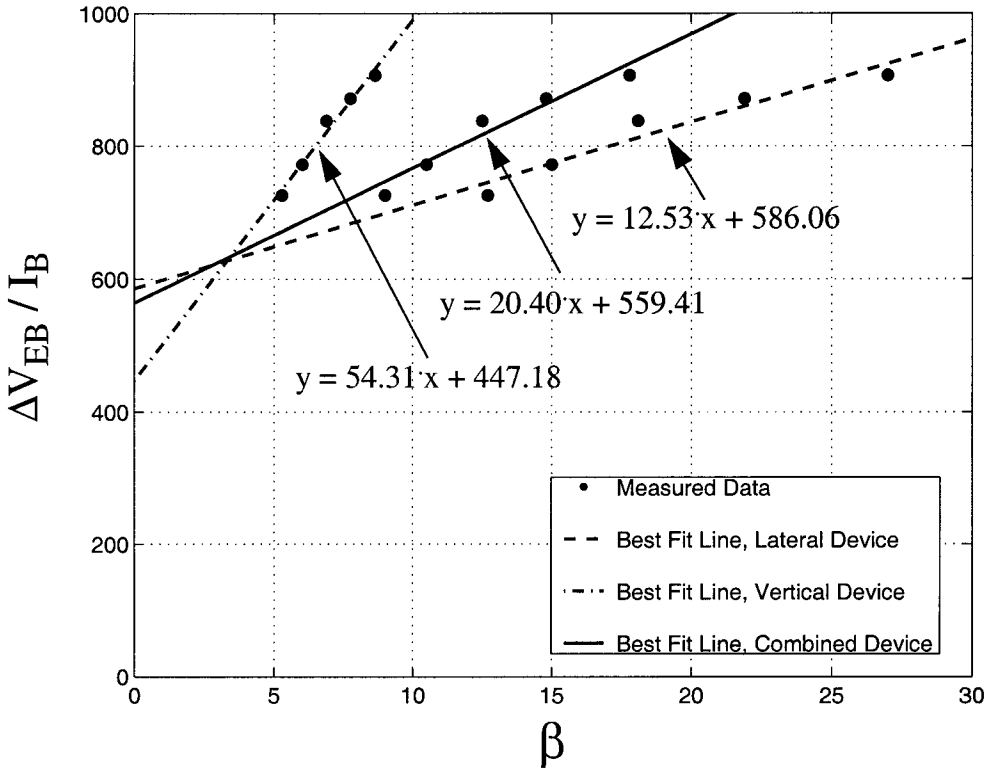


Figure 2.10 Best-fit curve for measurement of R_E and R_B

The data in Figure 2.10 has been taken from V_{EB} = 0.8 V to V_{EB} = 0.9 V, the minimum range of values for which a significant value of ΔV_{EB} could be measured. All values of I_B and I_C have been based on measurements from three individual devices.

From Figure 2.10, the extracted value of R_E varies from 12.5 Ω to 54.3 Ω, with an average of 29 Ω. The value of R_B varies from 393 Ω to 574 Ω, with an average of close to 500 Ω. The slope of the curves for the lateral and vertical devices was found to be very sensitive to the proportion of base current attributed to each device (chosen arbitrarily to be equal between the two devices) which partially explains the wide variation observed in the value for R_E.

To provide a verification of the value of emitter resistance, the open collector method [22] was used. Using this technique, the collector of the transistor is left in an open circuit condition, and the voltage at the collector can be expressed as

$$V_{EC} = v_T \ln\left(\frac{1}{\alpha_R}\right) + I_B R_E \tag{2.24}$$

where α_R represents the reverse current transfer ratio ($\alpha_R = \frac{\beta_R}{\beta_R + 1}$) and $I_B = I_E$. A plot of I_B vs V_{EC} produces a characteristic curve such as the one shown in Figure 2.11. The inverse of the slope of the curve in its linear region provides a measurement of R_E. The data in this case has been taken with both lateral and vertical collectors open, and once again taken from three individual devices.

The value of R_E has been measured to be between 35Ω-45Ω, in reasonable agreement with the average measured value of R_E extrapolated from Eqn. (2.23). The values of R_E = 35Ω and R_B = 500Ω, will be used as the starting point in the model optimization for both the lateral and vertical devices, and curve fitting (which will include the effect of I_{KF}) will be required to determine the final values of the emitter and base resistances.

Note that the collector resistance, R_C, has not been included within the SPICE model for the sake of simplicity. Based on geometric considerations, the value of R_C can be assumed to be lower than R_E, and the inclusion of a collector resistance of this size does not have any significant impact on the simulated log-domain circuit performance.

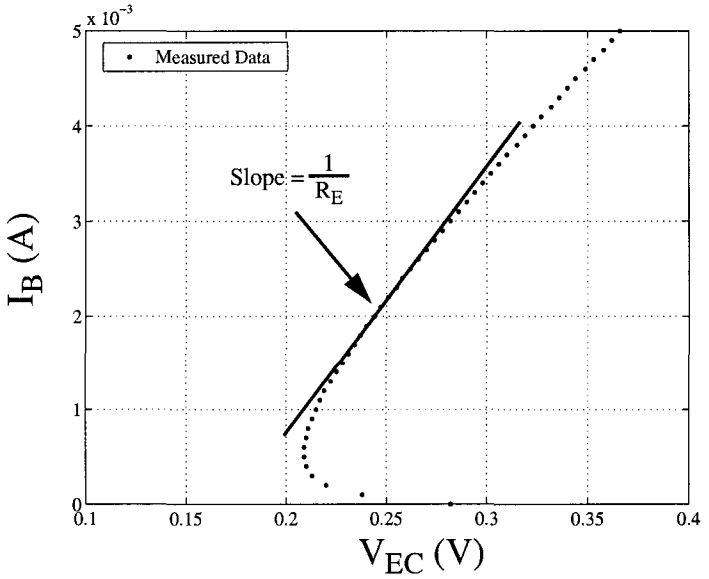


Figure 2.11 Plot of I_B vs V_{EC} used in measuring R_E

2.2.7 - Forward Base Transit Time (τ_F)

The forward base transit time (τ_F) is one of the most important parameters in defining the frequency response of a transistor. Base transit time is defined according to

$$\tau_F = \frac{Q_b}{I_C} \tag{2.25}$$

where Q_b represents the total dynamic minority carrier charge in the base, and I_C represents collector current, leading to the physical interpretation that τ_F represents the average time required for minority carriers to diffuse from the emitter to collector of the device. The parameter τ_F is used to define the total base charging capacitance of the transistor, C_b, one of three important capacitances which primarily determine the transistor frequency response. The value of C_b can be expressed as

$$C_b = \tau_F g_m \tag{2.26}$$

where g_m represents the transconductance of the device. The value of τ_F can also be used to determine the upper bound on the maximum theoretically operating frequency of the device, which can be defined as

$$f_{Tmaximum} = \frac{1}{2\pi\tau_F} \tag{2.27}$$

where $f_{Tmaximum}$ represents the maximum obtainable unity gain frequency of the transistor.

The value of Q_b is a function of the emitter-base forward bias voltage. Assuming a simple rectangular base geometry and a charge distribution which varies linearly from $p_{n(ebj)}$ at the emitter to zero at the collector, the value of Q_b can be expressed as

$$Q_b = \frac{1}{2} q p_{n(ebj)} A_{EB} W_B = \frac{1}{2} q A_{EB} W_B \cdot \frac{n_i^2}{N_B} e^{\frac{V_{EB}}{v_T}} . \tag{2.28}$$

Combining equations (2.5), (2.25), and (2.28) provides the following simple expression often used to calculate the base transit time [27]-[26],

$$\tau_F = \frac{W_B^2}{2D_p} . \tag{2.29}$$

However, when working with two separate collectors (and working within a circular structure) the derivation of Q_b is more complex. This section will present an analysis adapted from [29] that will be used to estimate the value of Q_b which can be attributed to both the lateral and vertical devices. From these values, the base transit time, τ_F, can be determined. Note that an experimental verification of the theoretical values of τ_F has not been performed in this case.

A cross sectional diagram, which can be used to approximate the minority charge distribution within a lateral PNP transistor, is shown in Figure 2.12. The three-dimensional cylindrical region below the emitter can be defined as Q_{b1}, and the charge distribution within this cylinder can be modelled as varying uniformly in the vertical direction, from $p_{n(ebj)}$ at the emitter junction to zero at the substrate junction. The hollow cylindrical shell between the emitter and lateral collector can be defined as Q_{b2}, and the charge distribution in this case can be modelled as varying uniformly in the radial direction, from $p_{n(ebj)}$ at the emitter to zero at the lateral collector. The remaining cylindrical shell can be defined as Q_{b3}, and the charge

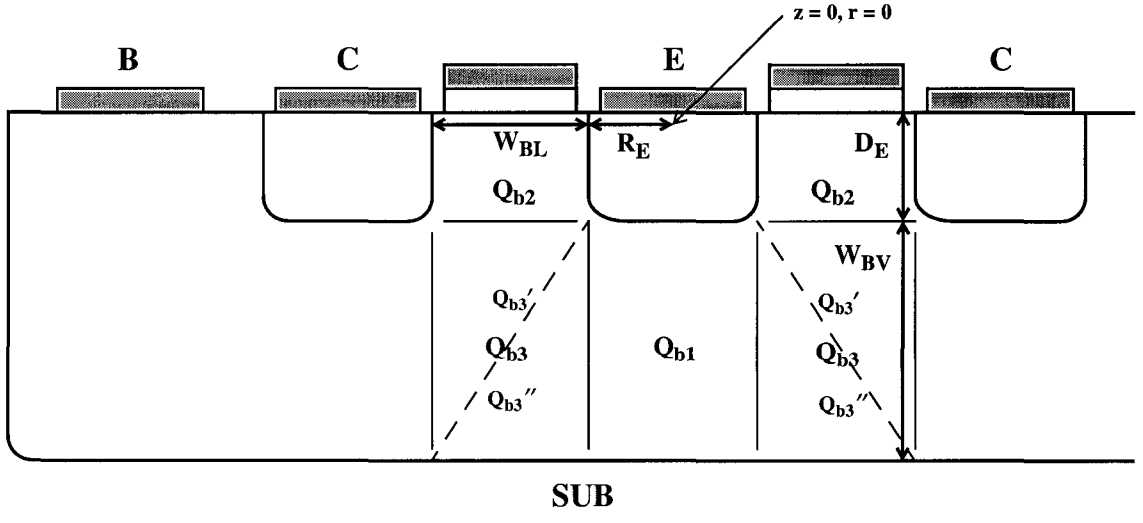


Figure 2.12 Cross sectional diagram of a lateral PNP minority charge distribution model (vertical axis not to scale)

distribution can be modelled as varying in both the vertical and radial directions, from $p_{n(ebj)}$ at the emitter edge to zero at both the substrate junction and zero at cylinder's exterior edges. The minority charge outside these cylindrical shells can be treated as negligible [29] and will be omitted for the purposes of this analysis.

The total charge in the Q_{b1} region can be found by integration along the vertical dimension of the vertical base region. Using the dimensions as defined Figure 2.12, the value of Q_{b1} can be approximated as

$$Q_{b1} = qp_{n(ebj)} \int_{z=D_E}^{z=D_E+W_{BV}} \int_{r=0}^{r=R_E} \left(1 - \frac{z - D_E}{W_{BV}}\right) \cdot 2\pi r dr dz$$

$$= qp_{n(ebj)} \cdot \frac{\pi}{2} \cdot W_{BV} R_E^2 \,. \tag{2.30}$$

Similarly, the total charge in the Q_{b2} region can be approximated as

$$Q_{b2} = qp_{n(ebj)} \int_{z=0}^{z=D_E} \int_{r=R_E}^{r=R_E+W_{BL}} \left(1 - \frac{r - R_E}{W_{BL}}\right) \cdot 2\pi r dr dz$$

$$= qp_{n(ebj)} \cdot \pi \cdot W_{BL} D_E \left(R_E + \frac{W_{BL}}{3}\right), \tag{2.31}$$

and the total charge in the Q_{b3} region can be approximated as

$$Q_{b3} = qp_{n(ebj)} \int_{z=D_E}^{z=D_E+W_{BV}} \int_{r=R_E}^{r=R_E+W_{BL}} \left(1 - \frac{z - D_E}{W_{BV}}\right)\left(1 - \frac{r - R_E}{W_{BL}}\right) \cdot 2\pi r dr dz$$

$$= qp_{n(ebj)} \cdot \pi \cdot W_{BL} W_{BV} \left(\frac{R_E}{2} + \frac{W_{BL}}{6}\right). \tag{2.32}$$

The total dynamic minority charge in the base can therefore be calculated from the sum of Q_{b1}, Q_{b2}, and Q_{b3}, which depend only on $p_{n(ebj)}$ and geometrical parameters.

The question remains as to the quantity of the charge which should be attributed to the lateral and vertical components of the transistor. As shown in Figure 2.12, a line has been drawn between two corners of the Q_{b3} region. It has been assumed that charge which lies above this partition, including Q_{b2} and the region labelled as Q_{b3}', can be considered to belong to the lateral device, and that charge which lies below this partition, including Q_{b1} and

the region labelled as Q_{b3}'', can be considered to belong the vertical device. The values of Q_{b3}' and Q_{b3}'' can be calculated by modifying the limits of integration in Eqn. (2.32), and are given by

$$Q_{b3}' = qp_{n(ebj)} \int_{z=D_E}^{z=D_E+W_{BV}} \int_{r=R_E+\left(\frac{z-D_E}{W_{BV}}\right)W_{BL}}^{r=R_E+W_{BL}} \left(1-\frac{z-D_E}{W_{BV}}\right)\left(1-\frac{r-R_E}{W_{BL}}\right)\cdot 2\pi r\,dr\,dz$$

$$= qp_{n(ebj)} \cdot \pi \cdot W_{BL}W_{BV}\left(\frac{R_E}{4}+\frac{7\cdot W_{BL}}{60}\right) \tag{2.33}$$

$$Q_{b3}'' = qp_{n(ebj)} \int_{z=D_E}^{z=D_E+W_{BV}} \int_{r=R_E}^{r=R_E+\left(\frac{z-D_E}{W_{BV}}\right)W_{BL}} \left(1-\frac{z-D_E}{W_{BV}}\right)\left(1-\frac{r-R_E}{W_{BL}}\right)\cdot 2\pi r\,dr\,dz$$

$$= qp_{n(ebj)} \cdot \pi \cdot W_{BL}W_{BV}\left(\frac{R_E}{4}+\frac{W_{BL}}{20}\right) \tag{2.34}$$

The base transit times can then be calculated using equations (2.5) and (2.30) - (2.34), according to the expressions

$$\tau_{F(lateral)} \approx \frac{Q_{b2}+Q_{b3}'}{I_{c(lateral)}}, \qquad \tau_{F(vertical)} \approx \frac{Q_{b1}+Q_{b3}''}{I_{c(vertical)}} \tag{2.35}$$

Using the dimensions given in the Appendix, the values of base transit time can be estimated as 100 ps for the lateral device and 1.3 ns for the vertical device, and these values have been used as the SPICE parameters for the final transistor model.

Note that there are many approximations and assumptions made in the analysis above. In particular, note that the minority charge under the lateral collector to the base contact has not been included in the analysis, and therefore the estimate of τ_F is almost certainly an underestimate. Also note that this sort of derivation makes the assumption that the base is uniformly doped, which is likely not the case for this transistor. Despite these drawbacks, the high-frequency modelling of the transistor was found to be adequate for the circuit designed in this work, as will be discussed in detail in Chapters 3 and 4.

2.2.8 - Parasitic Capacitance Parameters

The final set of parameters which must be discussed are those associated with parasitic capacitances. Since information about the parasitic capacitances is provided by the manufacturer, these model parameters have been adapted from the manufacturer's literature and/or extracted using the available software layout tools. This section will briefly describe the parasitic parameters of interest, and provide a tabulation of the parameters to be used in the transistor model.

The two most important capacitances used to model the frequency response of a bipolar transistor are C_π and C_μ. The value of C_π is defined as the sum of the base charging capacitance C_b, defined previously by Eqn. (2.26), and the parasitic emitter-base junction capacitance C_{je}. The value of C_μ is defined as the parasitic collector-base junction capacitance C_{jc}. These parasitic capacitances are given by the two expressions

$$C_{je} = \frac{C_{jeo}}{\left(1 - \frac{V_{EB}}{V_{je}}\right)^{m_{je}}}, \tag{2.36}$$

$$C_{jc} = \frac{C_{jco}}{\left(1 - \frac{V_{CB}}{V_{jc}}\right)^{m_{jc}}} \tag{2.37}$$

where C_{jeo} and C_{jco} represent the zero bias capacitance across the emitter-base and collector base junctions respectively, V_{EB} and V_{CB} represent the built-in potentials of respective junctions, and m_{je} and m_{jc} represent the grading coefficients of each respective junction. The effect of these parasitic capacitances on the transition frequency of the transistor, f_T, is given in [27] and can be expressed as

$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_\pi + C_\mu} = \frac{1}{2\pi} \cdot \frac{1}{\left(\tau_F + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m}\right)}. \tag{2.38}$$

One additional capacitance which must be included in this model is the gate to base capacitance, C_{gb}, formed by the MOSFET transistor, as shown by M_1 in

Figure 2.1(b) and shown schematically in Figure 2.2(a). This capacitance does not fit in any standard bipolar SPICE model, and will be included as a stand-alone capacitance. The values of each of the parasitic capacitance parameters described above are provided below in Table 2.2.

Table 2.2:Parasitic Capacitance Parameters for the SPICE model

Model Parameter	Lateral Device	Vertical Device
C_{jeo}	3.6 fF	3.6 fF
V_{je}	0.9 V	0.9 V
M_{je}	0.55	0.55
C_{jco}	25 fF	10 fF
V_{jc}	0.9 V	0.55 V
M_{jc}	0.55	0.35
Gate-Base Capacitance: 12 fF		

2.3 - Lateral PNP Transistors: Complete SPICE Model

A complete SPICE model of the lateral PNP transistor has been developed. The parameters described in Section 2.2 have been used for this model, and it will be shown that this set of parameters is sufficient to adequately capture the behaviour of the transistor. This section will present the initial SPICE model, briefly describe the model optimization, and present the final and complete SPICE model for the lateral PNP transistor.

An initial SPICE model has been developed based on the parameter values calculated and measured in Section 2.2, and are summarized in Table 2.3. A comparison of the DC characteristics of the modelled and the experimentally measured response is shown in Figure 2.13. Due to the interaction between the parameters in the combined model, the predicted DC characteristics shown in the figure are not ideal. In particular, there are significant deviations in the model for large values of V_{EB} forward bias,

indicating that high injection effects and parasitic base and emitter resistances have not been modelled accurately.

An optimization of the model has been performed. It was found that the values of I_{KF} for the lateral device did not sufficiently model the roll-off of the lateral collector current. By reducing the value of I_{KF} to that of the vertical device, a much better fit was generated. Since both devices have been observed to interact closely with one another, using a single value of I_{KF} for both devices is reasonable. The final optimized value was 30 μA for both devices.

It was also found that values of R_E and R_B were not sufficiently large to model the roll-off of the base current. Since direct open collector measurements had indicated the value of R_E to be close to 35 Ω, already a large value for emitter resistance, it was the value of base resistance which was increased. A value of R_B equal to 1000 Ω provided the best results.

To further improve the fit, the value of β was decreased to 120 for the lateral device and 15 for the vertical device, closer to the theoretically expected values. To more accurately capture the overall slopes of the collector currents, the values of n_F were increased to 1.25 for the lateral device and 1.10 for the vertical device, and the values of I_S fit accordingly. The parameters V_A, τ_F, and the parasitic capacitances were not adjusted in the optimization.

The optimized parameter values for the final transistor model are summarized in Table 2.4. A comparison of the DC characteristics of the modelled response and the experimentally measured response is shown in Figure 2.14. Note in particular the fit at V_{EB} = 0.7 V, the point about which the optimization has been performed. A linear plot of the modelled and experimentally measured responses has also been included in Figure 2.15 in order to more clearly show the high-bias current agreement.

Table 2.3:Initial values for SPICE lateral PNP Model

SPICE Parameter	Lateral	Vertical	SPICE Parameter	Lateral	Vertical
IS	1.2×10^{-15}	2.7×10^{-18}	TF	1.0×10^{-10}	1.3×10^{-9}
NF	1.19	1.03	CJE	3.6×10^{-15}	3.6×10^{-15}
BETA	150	20	VJE	0.9	0.9
VAF	6.5	40	MJE	0.55	0.55
IKF	1.45×10^{-4}	2.1×10^{-5}	CJC	2.5×10^{-14}	1.0×10^{-14}
RE	35	35	VJC	0.9	0.55
RB	500	500	MJC	0.55	0.35
Gate Base Capacitance: 1.2×10^{-14}					

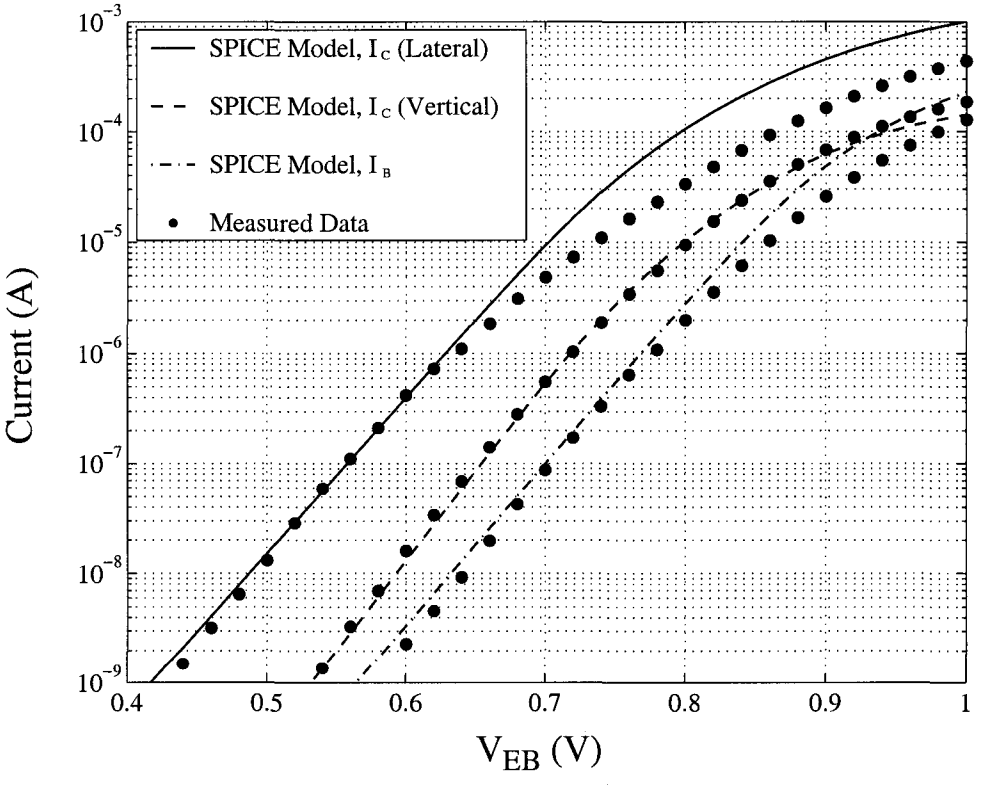


Figure 2.13 Initial DC characteristic curves for lateral PNP SPICE model

Table 2.4:Optimized values for SPICE lateral PNP Model

SPICE Parameter	Lateral	Vertical	SPICE Parameter	Lateral	Vertical
IS	1.8×10^{-15}	1.0×10^{-17}	TF	1.0×10^{-10}	1.3×10^{-9}
NF	1.25	1.10	CJE	3.6×10^{-15}	3.6×10^{-15}
BETA	120	15	VJE	0.9	0.9
VAF	6.5	40	MJE	0.55	0.55
IKF	3.0×10^{-5}	3.0×10^{-5}	CJC	2.5×10^{-14}	1.0×10^{-14}
RE	35	35	VJC	0.9	0.55
RB	1000	1000	MJC	0.55	0.35
Gate Base Capacitance: 1.2×10^{-14}					

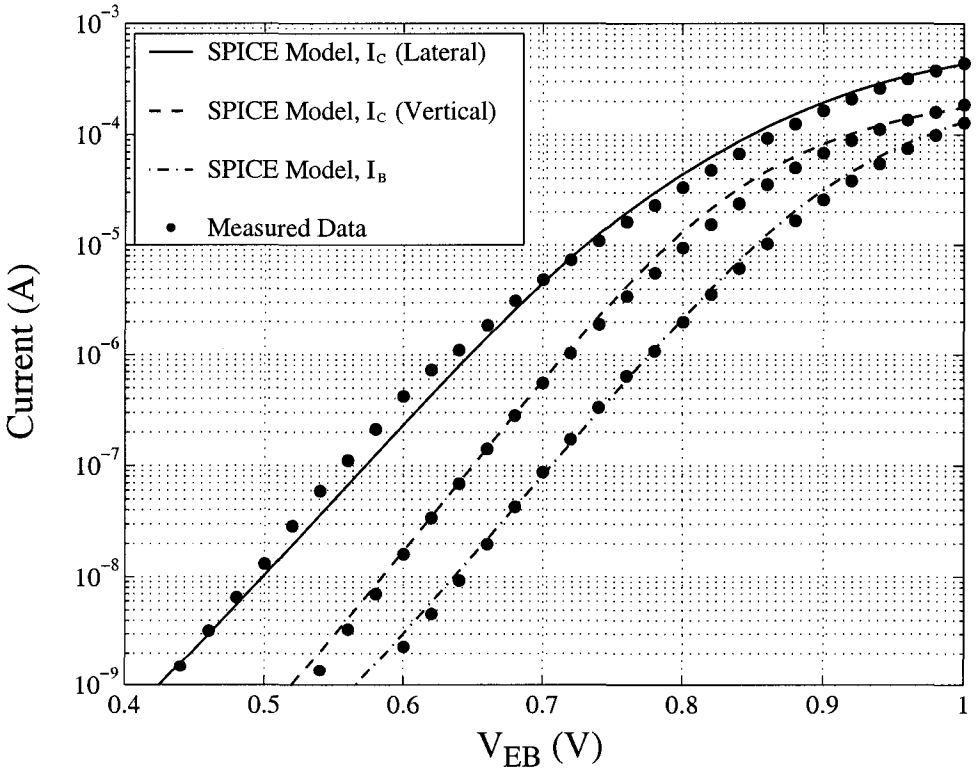


Figure 2.14 Optimized DC characteristic curves for lateral PNP SPICE model

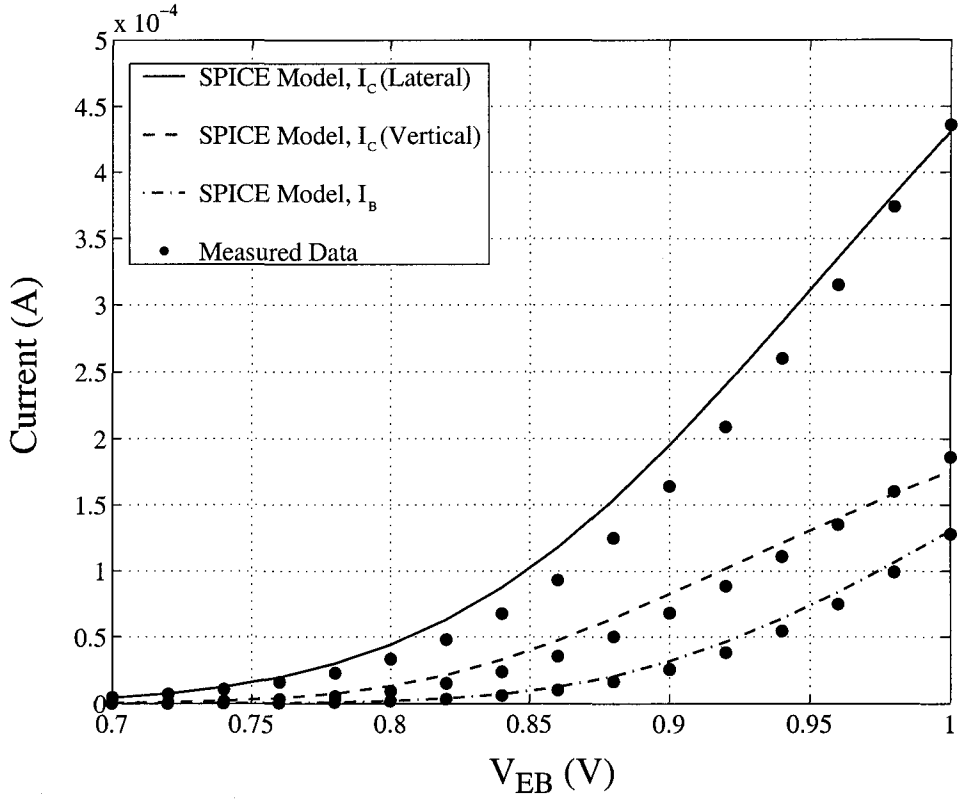


Figure 2.15 Linear plot of DC characteristic curves for lateral PNP SPICE model

Since the high frequency performance of these devices was not directly measured, no optimization or comparison of the high frequency performance was undertaken. Furthermore, the evaluation of parameters such as the transition frequency, f_T, are somewhat difficult to define, since the base current of the lateral and vertical transistors are connected through a common terminal. However, if the effective current gain is defined as

$$\beta_{eff} = I_{C(lateral)} / I_{B(lateral+vertical)} \tag{2.39}$$

then a number similar in nature to the transition frequency f_T can be calculated. In simulation, the value of this modified value of f_T was found to be 320 MHz at 10 μA, and 490 MHz at 100 μA. While these values would appear to overestimate of the performance of these lateral PNP devices, it will be demonstrated in Chapter 3 and 4 that log-domain filter circuits which make use these devices can operate at frequencies at over 10 MHz. It

has previously been shown that log-domain filters can be made to operate up to frequencies of approximately 1/10 of the f_T of the slowest transistors [5]. If this were the case in this work as well, it would suggest that the effective f_T of the lateral PNP transistors would be on the order of 100 MHz or higher, well within a factor of ten of the effective f_T values above from simulation. Therefore, while the lateral PNP model can be expected to overestimate frequency performance (due in large part to an underestimation of τ_F), the modelled transistor frequency response is still reasonable, based on experimental measurements from working log-domain circuits.

In conclusion, a SPICE compatible model has been developed for a lateral PNP transistor fabricated in 0.35μ CMOS technology. The model requires only fifteen parameters in total, each of which can be estimated based on physical considerations, extracted from straightforward device measurements, or adopted from standard information provided by the manufacturer. The model is sufficiently simple that it can be readily developed in any CMOS technology.

This model will form the basis for all the designs and simulations of the log-domain filter circuits described in the subsequent chapters, and will be used to demonstrate the feasibility of implementing circuits using the lateral PNP transistor in CMOS technology.

Chapter 3 - The Design of a Log-Domain Integrator in CMOS Technology

In the previous chapter, it has been shown that lateral PNP transistors with promising characteristics can be fabricated in CMOS technology. These transistors can be used to implement a log-domain integrator, a circuit which serves as a fundamental building block for log-domain filter designs. In this chapter, a log-domain integrator, developed in 0.35μ CMOS technology, will be presented.

Several important designs for log-domain integrators have been described in the literature [1]. Of these, some can be implemented using only NPN transistors in the signal path. Such implementations are of particular interest, since these circuits can be mapped directly in CMOS technology using the lateral PNP transistor. However, as is the case whenever a circuit design is mapped into a new technology, there are several considerations which must be taken into account. This chapter will describe the process of developing the log-domain integrator in CMOS technology.

The outline of this chapter is as follows: the first section will provide the theoretical background required to describe the operation of a log-domain integrator. The second section will describe the methodology of mapping the log-domain integrator into

CMOS technology, as well as describing the required interface circuitry. The final section will present both simulated results and experimental measurements of the log-domain integrator, demonstrating both the capabilities and limitations of this new log-domain filtering approach.

3.1 - Fundamentals of Log-Domain Integrator Design

The following section will provide the background required to describe the first-order operation of a log-domain integrator. A method of mathematical notation will be introduced and applied to a simple, all-bipolar log-domain integrator circuit. In addition, an important variation of the circuit, the damped log-domain integrator, will be described. The damped integrator circuit will be used for simulations and experimental measurements of the integrator performance provided later in this chapter.

3.1.1 - The Log-Domain Cell and the LOG(x) and EXP(x) Operators

A basic log-domain cell is shown below in Figure 3.1. Only two PNP transistors are required for the cell, yet it forms the heart of all the log-domain circuitry to be presented in this chapter. To derive the transfer function for this cell for the general case, the circuit can be treated as a translinear loop. The sum of the voltages around this loop can be expressed as

$$V_1 - V_{EB1} + V_{EB2} - V_2 = 0 \quad . \tag{3.1}$$

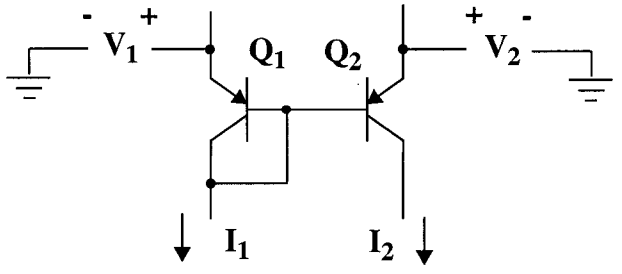


Figure 3.1: The basic two-transistor log-domain cell

By expressing I_C as an exponential function of V_{EB}, and neglecting the effects of β, V_A, and n_F, Eqn. (3.1) can be rearranged to give

$$V_2 = V_1 - v_T \cdot \ln\left(\frac{I_1}{I_2}\right) \tag{3.2}$$

where I_1 and I_2 are as shown in Figure 3.1. Equation (3.2) can also be re-arranged as

$$I_2 = I_1 e^{\frac{V_2 - V_1}{v_T}} . \tag{3.3}$$

Two special cases of this cell are shown below in Figure 3.2. From Eqn. (3.2), the output voltage V_{out} for the circuit in Figure 3.2(a) can be expressed as

$$V_{out} = -v_T \cdot \ln\left(\frac{I_o + I_{in}}{I_o}\right) \tag{3.4}$$

while from Eqn. (3.3), the current I_{out} for the circuit in Figure 3.2(b) can be expressed as

$$I_{out} = I_o e^{\frac{-V_{in}}{v_T}} - I_o . \tag{3.5}$$

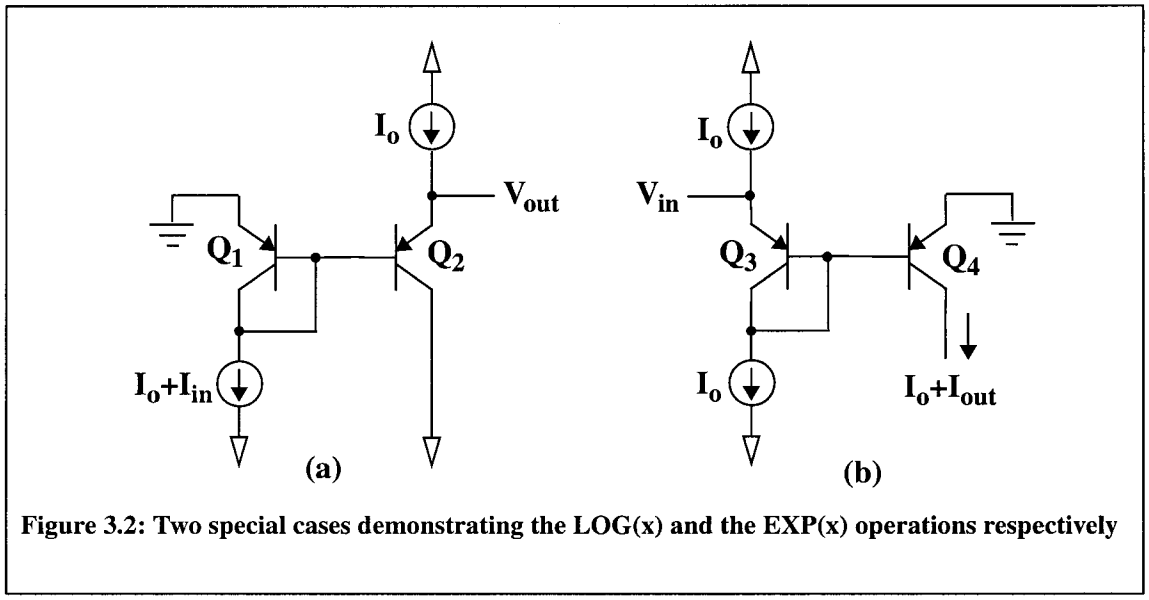


Figure 3.2: Two special cases demonstrating the LOG(x) and the EXP(x) operations respectively

From these, two complementary mathematical operators can be defined:

$$LOG(x) = -v_T \cdot \ln\left(\frac{I_o + x}{I_o}\right), \tag{3.6}$$

and

$$EXP(x) = I_o e^{\frac{-x}{v_T}} - I_o . \tag{3.7}$$

These functions imitate logarithmic and exponential operations, and can be implemented directly using the circuitry shown in Figure 3.2. In fact, the circuit in Figure 3.2(a) will be used to directly implement a logarithmic compression stage, and the circuit in Figure 3.2(b) will be used to directly implement an exponential expansion stage, each as shown in the block diagram of Figure 1.2 in Chapter 1. Note also that the operations defined in Eqns. (3.6) and (3.7) will be used throughout the next two chapters, and will form the mathematical language used to describe and develop log-domain circuits throughout this work.

With the LOG(x) and EXP(x) functions and associated circuitry defined, the development of a log-domain integrator can now be described.

3.1.2 - The Log-Domain Integrator

A PNP-only log-domain integrator is shown below in Figure 3.3. The cell has been adapted from a low voltage NPN-only integrator described in [1], [11]. The circuit below has two inputs, labelled as $\hat{V}_p$ and $\hat{V}_n$, and an output labelled as $\hat{V}_{out}$[1]. The integrator is implemented using two translinear loops. The first loop (from $\hat{V}_p$ to $\hat{V}_{out}$) is formed by Q_1 and Q_2, while the second loop (from $\hat{V}_n$ to $\hat{V}_{out}'$) is formed by Q_3 and Q_4. A simple voltage buffer from $\hat{V}_{out}$ to $\hat{V}_{out}'$ is formed by Q_5 and Q_6, while the current pulled into the $\hat{V}_{out}'$ node is mirrored into the $\hat{V}_{out}$ node by Q_7 and Q_8. A more detailed analysis of the circuit is provided below.

1. The "^" mark has been used to designate voltages that represent signals which have undergone logarithmic compression.

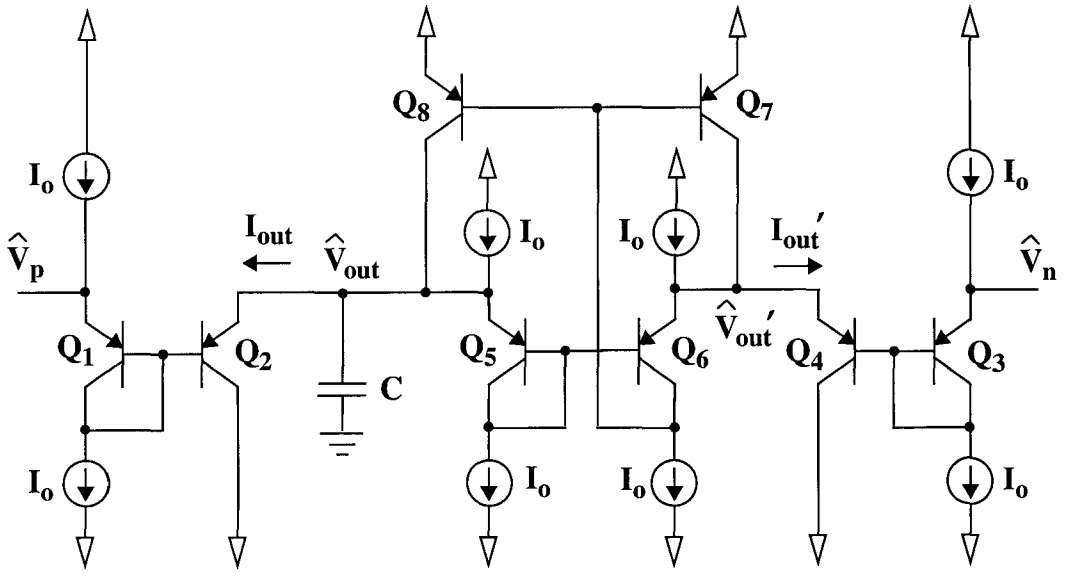


Figure 3.3: A PNP-only log-domain integrator

To derive the transfer function of the circuit, an expression relating the voltages around each translinear loop must be determined. For the first loop the output current can be expressed in terms of Eqn. (3.3), given by

$$I_{out} = I_o e^{\frac{\hat{V}_{out} - \hat{V}_p}{v_T}} \tag{3.8}$$

where I_o is the bias current in Q_1 and I_{out} is the bias current in Q_2, as shown in Figure 3.3. For the second loop, a similar expression can be derived, given by

$$I_{out}' = I_o e^{\frac{\hat{V}_{out}' - \hat{V}_n}{v_T}} . \tag{3.9}$$

A voltage buffer, formed by Q_5 and Q_6, has been inserted between the two loops. Each transistor is biased with a constant current such that each V_{EB} is fixed. The signal $\hat{V}_{out}$ at the emitter of Q_5 will be level shifted the base of Q_5 and Q_6, and then replicated at the emitter of Q_6, $\hat{V}_{out}'$. Therefore the voltage $\hat{V}_{out}'$ will be equal to $\hat{V}_{out}$. This is achieved without loading the node $\hat{V}_{out}$.

A current mirror, formed by Q_7 and Q_8, provides a means of subtracting the two output currents I_{out} and I_{out}'. The current drawn from the $\hat{V}_{out}'$ by Q_4 will be pulled from Q_7, and since transistor Q_8 has the same V_{EB} voltage as Q_7, the current will be mirrored, with a sign inversion, into the node $\hat{V}_{out}$. Note that the bases of Q_7 and Q_8 are connected to the collector of Q_6, ensuring that the voltages at collectors of Q_7 and Q_8 are both floating and free to follow the voltages at the $\hat{V}_{out}$ and $\hat{V}_{out}'$ nodes.

Combining the voltage buffering and current mirroring of transistors Q_5-Q_8, the sum of the currents flowing at the output node, $\hat{V}_{out}$, can be expressed as

$$-C \cdot \frac{d\hat{V}_{out}}{dt} = I_o e^{\frac{\hat{V}_{out}-\hat{V}_p}{v_T}} - I_o e^{\frac{\hat{V}_{out}-\hat{V}_n}{v_T}} . \tag{3.10}$$

Applying the chain rule, the derivative term can be expanded, and the equation rewritten as

$$C \cdot \frac{v_T}{I_o} \cdot e^{\frac{\hat{V}_{out}}{v_T}} \cdot \frac{d}{dt}\left(I_o e^{\frac{-\hat{V}_{out}}{v_T}} \right) = I_o e^{\frac{\hat{V}_{out}-\hat{V}_p}{v_T}} - I_o e^{\frac{\hat{V}_{out}-\hat{V}_n}{v_T}} . \tag{3.11}$$

By multiplying through by $e^{\frac{-\hat{V}_{out}}{v_T}}$ and then subtracting the term I_0 from each exponential expression, the equation can be written in form

$$C \cdot \frac{v_T}{I_o} \cdot \frac{d}{dt}\left(I_o e^{\frac{-\hat{V}_{out}}{v_T}} - I_o \right) = \left(I_o e^{\frac{-\hat{V}_p}{v_T}} - I_o \right) - \left(I_o e^{\frac{-\hat{V}_n}{v_T}} - I_o \right) . \tag{3.12}$$

Using the mapping defined in Eqn. (3.7), the expression can be rewritten as

$$EXP(\hat{V}_{out}) = \frac{I_o}{v_T} \cdot \frac{1}{C} \cdot \int \{EXP(\hat{V}_p) - EXP(\hat{V}_n)\} dt . \tag{3.13}$$

Therefore, in terms of the logarithmic and exponential operations defined in the previous section, the circuit in Figure 3.3 can be used to implement a log-domain integrator.

3.1.3 - The Damped Log-Domain Integrator

An important variation of the above log-domain integrator is the damped integrator, which can be implemented by connecting the output of the standard integrator, $\hat{V}_{out}$, to the negative input, $\hat{V}_n$. A symbolic representation for the standard integrator and the damped integrator are shown Figure 3.4(a) and (b) respectively. The circuit equation for a damped integrator, as given by Eqn. (3.10), can be simplified to

$$C \cdot \frac{d\hat{V}_{out}}{dt} = I_o e^{\frac{\hat{V}_p - \hat{V}_{out}}{v_T}} - I_o \ . \tag{3.14}$$

Notice that the damped integrator circuit can be realized by replacing transistors Q_3-Q_8 in Figure 3.3 by a constant current source, I_0, as shown in Figure 3.4(c). The transfer function of the damped integrator can be described by

$$EXP(\hat{V}_{out}) = \frac{I_o}{v_T} \cdot \frac{1}{C} \cdot \int \{EXP(\hat{V}_p) - EXP(\hat{V}_{out})\} dt \ , \tag{3.15}$$

which will be stable at all frequencies, unlike an undamped integrator, which is theoretically unstable in the presence of a DC input. The damped integrator circuit will be used for simulations and experimental measurements of the integrator performance provided later in this chapter.

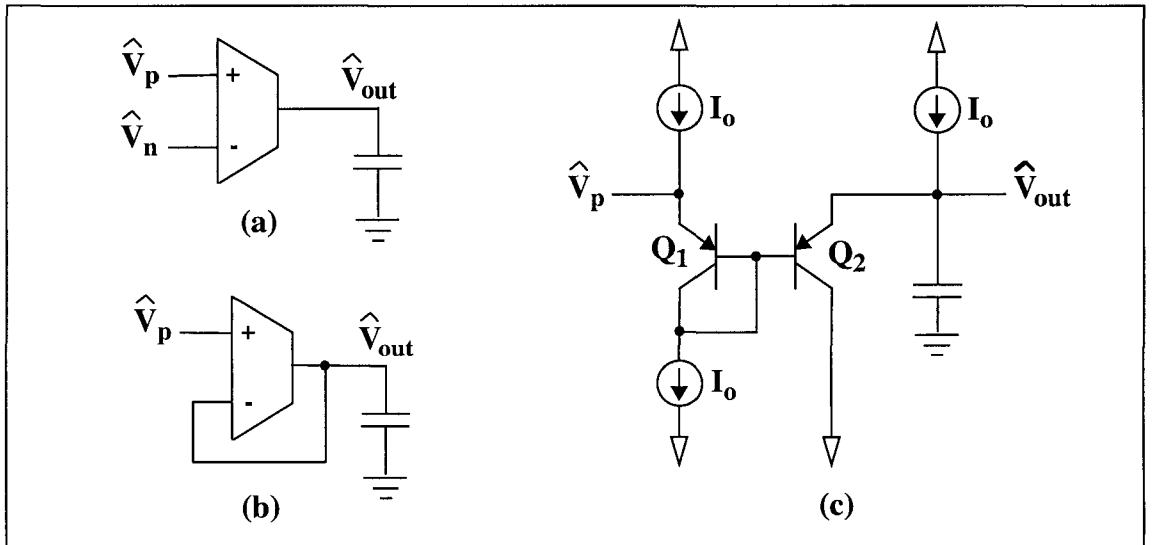


Figure 3.4: (a) Symbolic representation of an integrator (b) Symbolic representation of a damped integrator (c) A reduced realization of a PNP-only damped integrator circuit

3.2 - The CMOS Log-Domain Integrator

The following section will describe the methodology used in mapping the bipolar log-domain integrator into a CMOS process. Several considerations, including issues surrounding the increase in circuit complexity and the circuit power consumption, will be discussed. In addition, the supporting circuitry including logarithmic compression and exponential expansion circuitry will be described at the end of this section.

3.2.1 - Mapping the Log-Domain Integrator in CMOS Technology

In order to develop a log-domain integrator in CMOS technology, first note that the lateral PNP transistors could be used to directly implement the PNP-only integrator presented in Section 3.1. This circuit, included here for comparative purposes, is shown in Figure 3.5(a).

To improve upon this design, observe that only the translinear loops (Q_1, Q_2, Q_3 and Q_4) need to be implemented with bipolar transistors, and that PMOS transistors (operating in strong inversion) could be used to implement remaining circuitry. It follows that when working in a CMOS process which has been optimized for MOS performance (and which provides rigorous MOSFET models), PMOS transistors should be used in place of lateral PNP transistors when possible. In addition, since the Early voltage of the lateral PNP devices is relatively low, PMOS transistors can be used to provide cascoding, which has been shown through simulation to significantly improve the integrator performance. Further improvements can also be realized by placing level shifting PMOS transistors in the diode-connected devices (Q_1, Q_3, and Q_6 in Figure 3.5(a)), which serve not only to keep cascode transistors from operating in triode, but also to provide DC beta compensation for the bipolar devices in each of the translinear loops. The improved log-domain integrator is shown in Figure 3.5(b).

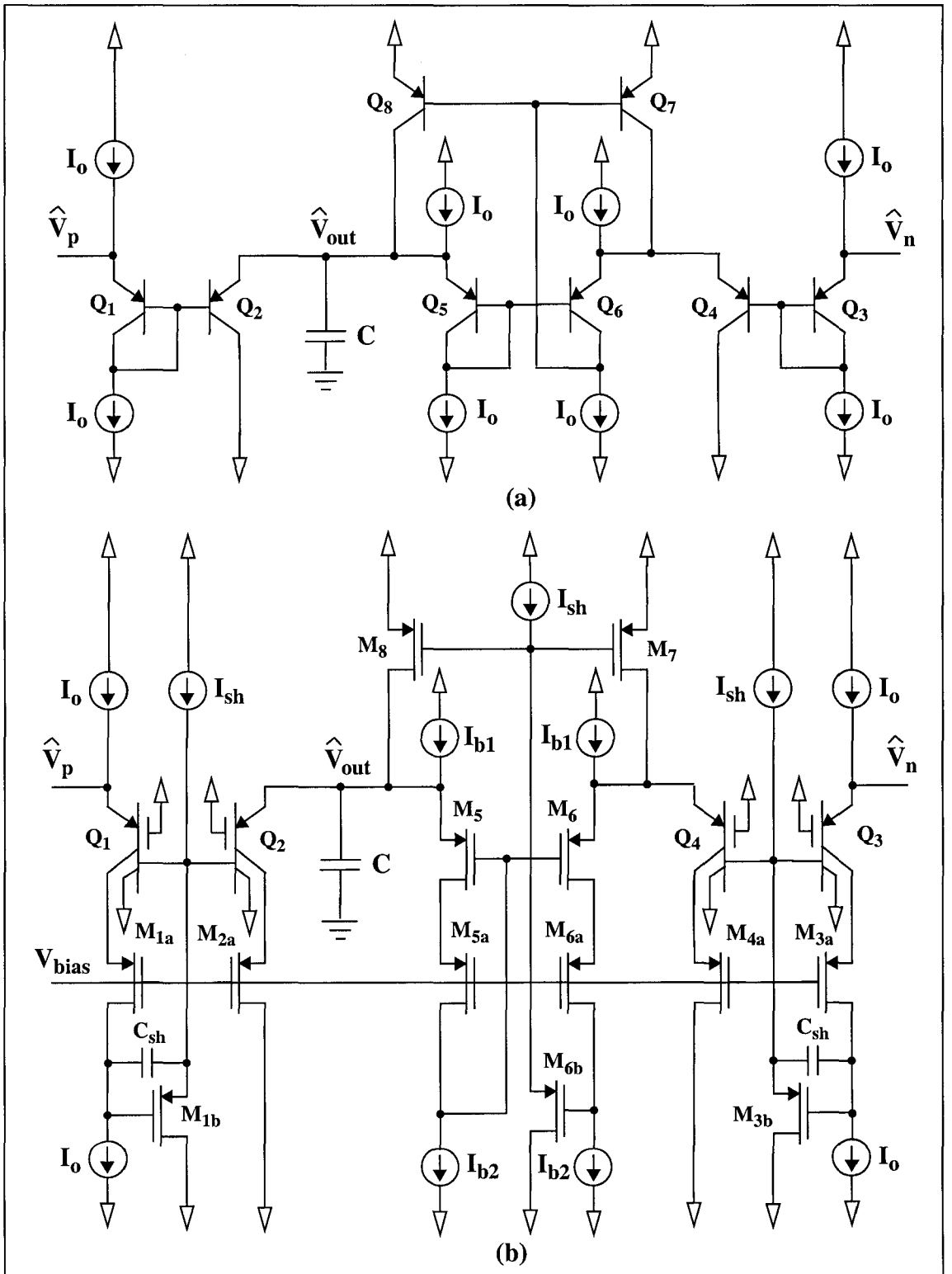


Figure 3.5: (a) Original implementation of a log-domain integrator
(b) A CMOS implementation of a log-domain integrator

While the original circuit in Figure 3.5(a) was biased with a universal value of current, designated by I_o, the improved circuit in Figure 3.5(b) has been biased with four independent currents, designated by I_o (the bias current for the translinear loop), I_{b1} and I_{b2} (the bias current of the voltage/current buffer) and I_{sh} (the bias current for the level shifter). The reason for this change stems from the replacement of bipolar transistors by MOSFETs in the improved design. While the lateral bipolar transistors can operate over a range of several decades of current, the MOSFET transistors (particularly those associated with Q_5 - Q_8) have not been intended to be biased at low levels of current, at which point they enter the subthreshold mode of operation. For this reason, I_{b1} and I_{b2} are generally not dropped below a few microamps, and need to be controlled independently when the translinear loop bias current is dropped to 1μA and below. In addition, the difference between these bias currents (I_{b2} - I_{b1}) can be used to ensure a constant current bias of a few microamps in M_7 and M_8. Finally, the remaining bias current I_{sh} is used to control the gate-source voltage of the level shifting transistors associated with Q_1, Q_3, and Q_5. This current is generally kept at a bias value of a few microamps. Note that the bias currents themselves have been generated using current mirrors implemented entirely with MOSFET transistors.

Circuit complexity issues aside, the most significant drawback to the modifications made to the integrator in Figure 3.5(b) come in the form of increased power consumption. The increase is due to two factors: firstly, because of the use of cascoding and the relatively large threshold voltage of the PMOS transistors (approximately 0.8 V in the 0.35μ CMOS process used in this work) the circuit must operate from a higher voltage supply than in the initial implementation. While its original bipolar technology counterpart was capable of operation down to 1 V [8], the circuit in Figure 3.5(b)has been designed to operate from a 2.5 V supply, and was found not to perform well at supplies below 2.2 V. The second factor leading to increased power consumption stems from the fact that the values of I_{b1}, I_{b2}, and I_{sh} are not generally not scaled in proportion to I_o for low levels of bias current, as has been described above. Therefore, the circuit in Figure 3.5(b) is not as efficient as its predecessor for low-power applications.

An additional comment should be made regarding the capacitance C_{sh} , as shown in Figure 3.5(b). At low levels of I_o, a resonance in the integrator response can occur due to feedback in the loop formed by Q_1, M_{1a}, and M_{1b} in the level shifting circuitry (and similarly for Q_3, M_{3a} and M_{3b}). The resonance can be reduced or eliminated by inserting a small additional capacitance ($\leq$ 1 pF) into this loop, as shown by C_{sh}, without reducing the bandwidth of the integrator. The inclusion of this capacitance, though not strictly required, can improve the ideality of the frequency response of the integrator at the expense of additional layout area. This trade-off could be a particularly important consideration if capacitances as large as 1 pF are used for each C_{sh}. The circuitry described in the experimental results section of this work utilized C_{sh} = 1 pF. No such capacitance was included in the MOS-only loop formed by M_6, M_{6a}, M_{6b}, and M_7.

The final design of the log-domain integrator, implemented in 0.35μ CMOS technology, is shown in Figure 3.5(b) with transistor dimensions as given in Table 3.1. All devices were reduced to the minimum gate length in order maximize the potential operating speed of the circuit, with the exception of M_7 and M_8, which were kept at a gate length of 0.8μ since these devices were not cascoded.

The integrator conforms to the integrator equation given by Eqn. (3.13) and the simulated and measured responses will be discussed in detail in Section 3.3. Before presenting these results, a description of the logarithmic compression and exponential expansion circuitry will be provided.

Table 3.1: Transistor Dimensions in CMOS Log-Domain Integrator Circuit

Transistor	Transistor Dimensions
Q_1, Q_2, Q_3, Q_4	2 x unit size lateral PNP transistor (shown in Figure 2.3)
M_{1a}, M_{2a}, M_{3a}, M_{4a}	4 x (3μ x 0.35μ)
M_{1b}, M_{3b}	4 x (12μ x 0.35μ)
M_5, M_{5a}, M_6, M_{6a}	4 x (6μ x 0.35μ)
M_{6b}	8 x (12μ x 0.35μ)
M_7, M_8	4 x (12μ x 0.8μ)

3.2.2 - Input Compression / Output Expansion and Interface Circuitry

In order to interface log-domain filter circuits to the outside (linear, as opposed to logarithmic) world, additional supporting circuitry is required. First, since log-domain filters are essentially current-mode circuits, a means must be provided to convert linear currents into the logarithmically compressed voltages, and in turn to convert logarithmically compressed voltages to linear currents. In addition, since it is most convenient to interface filters to test equipment using voltages rather than currents, a means should be included to provide linear voltage to current (V/I) conversion at the filter input and linear current to voltage (I/V) conversion at the filter output. Each of these four functions can be realized in a simple and compact manner using the circuitry described in this section.

A CMOS implementation of the logarithmic compression circuit, originally given in Figure 3.2(a), is shown below in Figure 3.6(a). In this circuit, the emitter of Q_1 is grounded and an input current, I_{in}, is introduced at the drain of M_{1a}. The input current is pulled through Q_1 and is logarithmically compressed in the form of the voltage at the emitter of Q_2, as was previously derived in Eqn. (3.4). This voltage can be expressed in mathematical notation, according to the operator defined in Eqn. (3.6), as $\hat{V}_i = LOG(I_{in})$. Note also that this circuitry can be implemented directly in place of the positive (or negative) translinear loops of the log-domain integrator itself.

A CMOS implementation of the exponential expansion circuit, is shown in Figure 3.6(b). In this circuit, the emitter of Q_4 is grounded and a logarithmically compressed input voltage is introduced at the emitter of Q_3. The difference in voltages at the emitters of Q_3 and Q_4 lead to an output current, I_{out}, which represents an exponential expansion of the applied input voltage, as was previously derived in Eqn. (3.5). This current can be expressed in mathematical notation, according the operator defined in Eqn. (3.6), as $I_{out} = EXP(\hat{V}_i)$. In addition, by including a current source at the emitter of Q_3, as shown in Figure 3.6(b), the circuit can be used to exponentially expand the voltage at any node without loading the node itself. The transistor dimensions for both the input compression and output expansion circuits are as given previously in Table 3.1

It is important to note that the two circuits shown in Figure 3.6 can be used within any portion of the implementation of a log-domain filter or circuit. In fact, as will be seen in Chapter 4, the derivation of both biquadratic and LC-ladder based log-domain filters are based upon the original assumption that each integrator block is preceeded by a logarithmic compression stage and immediately followed by an exponential expansion stage. However, as will become apparent when a signal flow graph approach is applied, a natural cancellation of the logarithmic and exponential operations can be made to occur during the filter design process, leaving the entire filter with only a single compression stage at its input and a single expansion stage at its output. The filter will therefore conform to the block diagram presented in Figure 1.2 in Chapter 1, in which only single compression and expansion stages are present.

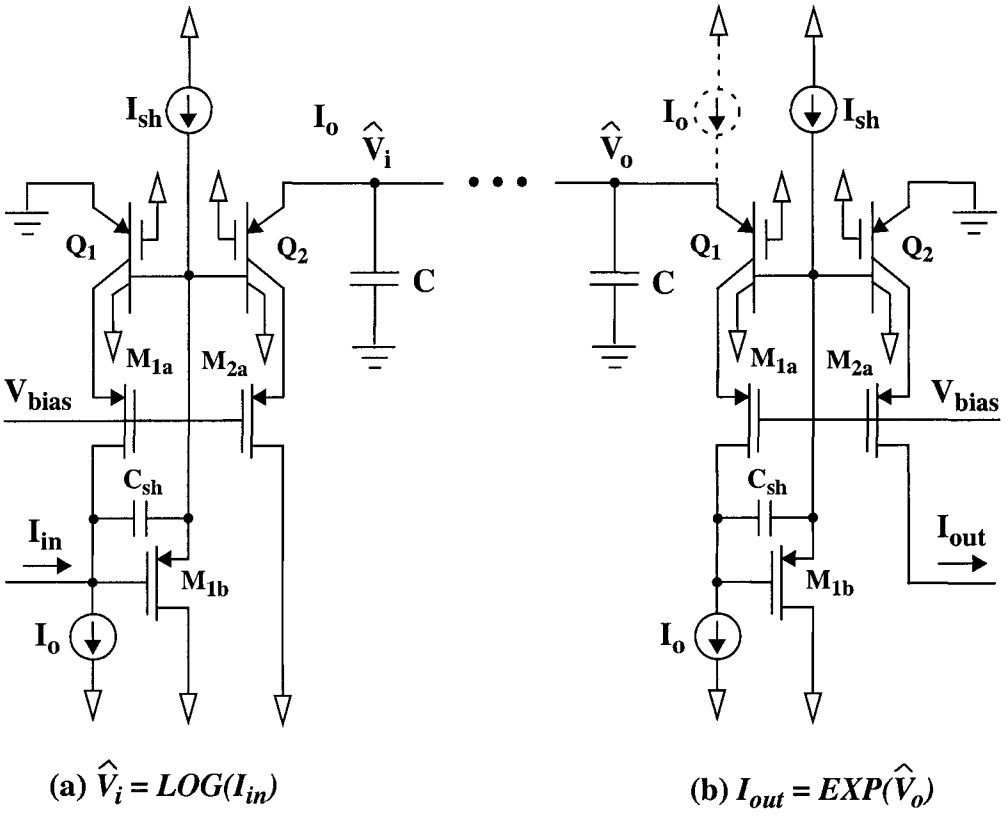


Figure 3.6: (a) A CMOS implementation of a logarithmic compression circuit (b) A CMOS implementation of an exponential expansion circuit

A compact all-CMOS implementation of a V/I converter, adapted from [11], is shown in Figure 3.7. In this circuit, transistors M_1 and M_2 are each biased with a constant current I_{vi}, while the diode connection between the gate of M_2 and the drain of M_{2a} provide a reference voltage to the gate of M_1. This arrangement ensures that the source of M_1 will be biased to DC ground. Furthermore, the feedback path formed by transistors M_1, M_{1a}, M_3 (and the DC level shifter M_4) serve to decrease the impedance seen at the source of M1 such that the node also serves as a virtual signal ground. This allows the V/I conversion to be implemented with a resistor, R_1, as shown in the figure.

To deliver this current to the desired log-domain circuit, note that the signal at the input will be first shunted through M_3, then replicated by M_5. The current will be forced through M_{5a}, reaching the output node at the drain of M_{5b}. The impedance of this node is high due to the use of cascoding, and the DC voltage at the node is compatible with the input logarithmic compression stage shown in Figure 3.6.

In this way, a simple circuit can be used to provide the required input V/I conversion at the input of the filter. Since the constant of voltage conversion is directly set by R_1, the input current can be readily scaled to an appropriate level. In addition, the output I/V conversion can be implemented in a very simple manner by connecting the exponential expansion stage, as shown in Figure 3.6(b), to a resistor R_2 at its output. In this case, the overall gain of the filter can be conveniently set using the ratio (R_2/R_1). The dimensions for the transistors shown in Figure 3.7 are provided below in Table 3.2.

Table 3.2: Transistor dimensions for compression and expansion circuits

Transistor	Transistor Dimensions
M_1, M_{1a}, M_2, M_{2a}, M_{4a}, M_{4b}	4 x (6μ x 0.35μ)
M_3, M_4	8 x (12μ x 0.8μ)
M_5	8 x (12μ x 0.35μ)

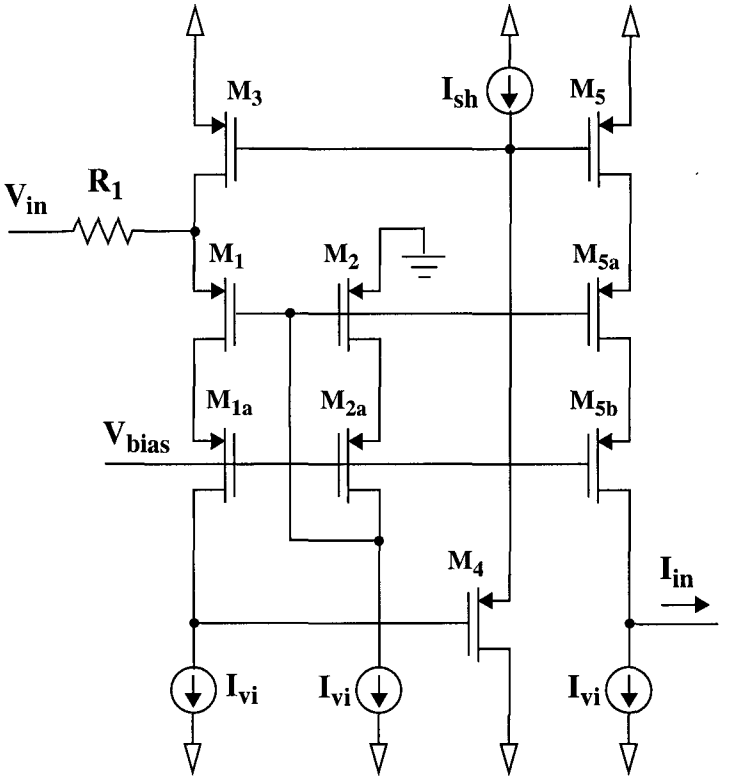


Figure 3.7: (a) A CMOS compatible V/I converter

The circuitry presented in this section can be used to implement a complete log-domain integrator, and the remainder of the chapter will be devoted to the simulated and experimental characterization of this integrator. It will be demonstrated that these circuits have promising performance characteristics, and by extension that the lateral PNP transistor can be used to implement useful circuits in CMOS technology.

3.3 - Simulated and Experimental Results

The final section of this chapter will discuss the simulated and experimental performance of a log-domain integrator fabricated in 0.35μ CMOS technology. Three categories of tests have been used to characterize the integrator performance: frequency response, linearity and distortion performance, and noise performance. Each will be described in detail, and a summary of performance will be provided at the end of the chapter. The section will begin with a description of the damped integrator circuit itself.

3.3.1 - Description of the Log-Domain Integrator Test Circuit

The log-domain circuit under test is shown in Figure 3.8(a). Transistors used as cascode devices and level shifters have been omitted from the diagram for visual clarity, though all simulations and measurements have been made using the complete circuit implementations originally shown in Figures 3.5 - 3.7. The circuit is composed of an input V/I stage (M_1, M_3, M_4 and R_1), a combined input compression and damped log-domain integrator stage (Q_1, Q_2, and C), an output compression stage (Q_3 and Q_4) and a I/V converter (implemented with R_2). As previously mentioned, the damped integrator circuit, rather than a two input integrator, was used for testing owing to its stability over all frequencies, unlike a standard integrator which is theoretically unstable in the presence of a DC input. Note that this circuit configuration does not allow for direct testing of the voltage/current buffer (transistors M_5 - M_8 in Figure 3.5) within the integrator itself. However, initial simulations have clearly indicated that this portion of the circuitry does not impose significant limitations on the frequency response, linearity, or noise performance of the overall integrator. A symbolic representation of the test circuit is shown in Figure 3.8(b). The input compression stage in the diagram has incorporated into the integrator, as indicated in the figure.

In the testing which follows, integrating capacitors of 10 pF (on chip), 100 pF and 1 nF (placed off chip) were used, and the input and output resistors were set to 500 Ω. The current sources were implemented using PMOS and NMOS current mirrors, and the values of I_o, I_{vi}, and I_{sh} could be independently controlled with off-chip references. For current biases from I_o = 10μA to 100 μA, the value of I_{vi} was set to be equal to I_o, but for current biases with I_o < 10 μA, I_{vi} was kept fixed at 10 μA. A value of I_{sh} = 5 μA was used in all tests described in this section.

The power supplies used for the simulation and testing of this circuit were nominally set to V_{DD} = 2.5 V, AGND (analog ground) = 2.0 V, and V_{SS} = 0 V. The measured frequency response of the log-domain filters was often found to be slightly improved by lowering V_{DD} to 2.35 V to 2.45 V, and most measurements were taken from this slightly lowered voltage. The bias voltage for the cascodes in both the integrator and the V/I circuit could be independently controlled, but was kept at 0.55 V above V_{SS} for all tests which are described here.

The log-domain circuit was manufactured in 0.35μ CMOS technology. All circuit simulations were performed using HSPICE and made use of the lateral PNP model developed in Chapter 2 as well as the 0.35μ models MOS provided by the manufacturer. All measurements were made using a Hewlett Packard 3588A Spectrum Analyzer, a Tektronix TDS800 Oscilloscope, and Hewlett Packard 3314A Function Generator. An off-chip unity-gain buffer (an AD817 Op-Amp) was used between the filter output and the various test equipment.

A microphotograph of the chip is shown in Figure 3.9(a). The total die area for a single integrator (not including current sources) was 220μ x 110μ, while the total area for on-chip (poly/poly) capacitors in this technology was $1700\mu^2$ / pF. The circuit board used for testing is shown in Figure 3.9(b).

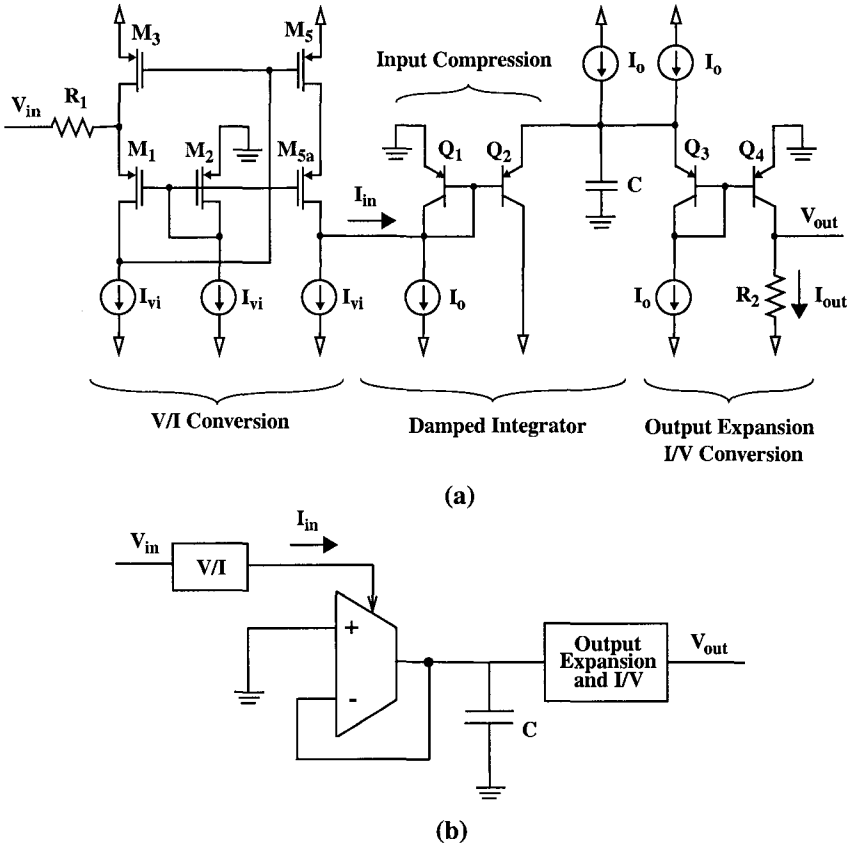
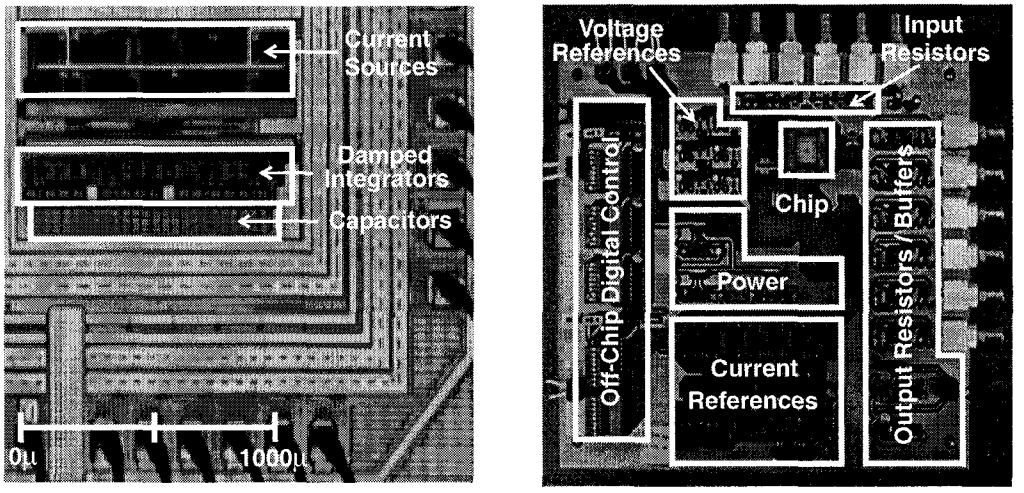


Figure 3.8: (a) A simplified schematic of the damped integrator circuit under test (b) A symbolic representation of the damped integrator circuit under test



(a) (b)

Figure 3.9: (a) A microphotograph of the damped integrators under test and associated circuitry (b) Photograph of the printed circuit board used to test the damped integrator

3.3.2 - Frequency Response

The first tests performed on the log-domain integrator measured the frequency response. Simulated and experimentally measured frequency responses for the integrator are shown in Figures 3.10 and 3.11. In the first figure, a constant capacitance of 10 pF was used while the bias current I_o was varied from 1 µA to 100 µA. In the second figure, a constant current of I_o = 100 µA was used while the capacitance was varied from 10 pF to 1 nF. A summary of frequency performance of the integrator is provided in Table 3.5.

As previously mentioned, the damped integrator is, in effect, a first order low-pass filter. The proportionality between the 3-dB frequency and the bias current I_o, and the inverse proportionality between the 3-dB frequency and the integrating capacitor C, is clearly demonstrated. These figures provide a verification that this CMOS integrator follows the log-domain relationships given by Eqn. (3.13) and (3.15) and further indicates that this CMOS lateral PNP transistor behaves in the manner expected of traditional bipolar devices.

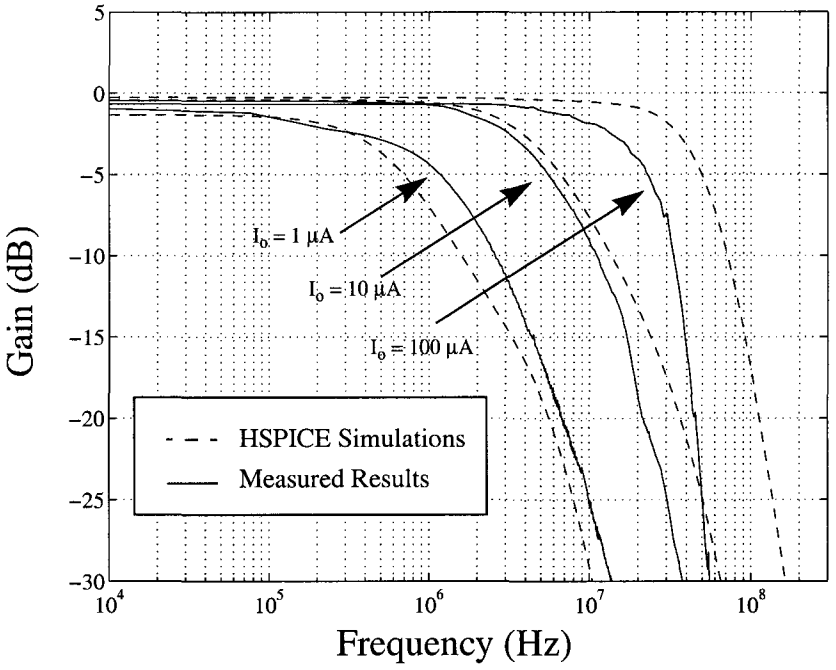


Figure 3.10: Frequency response of the log-domain integrator, C = 10 pF.

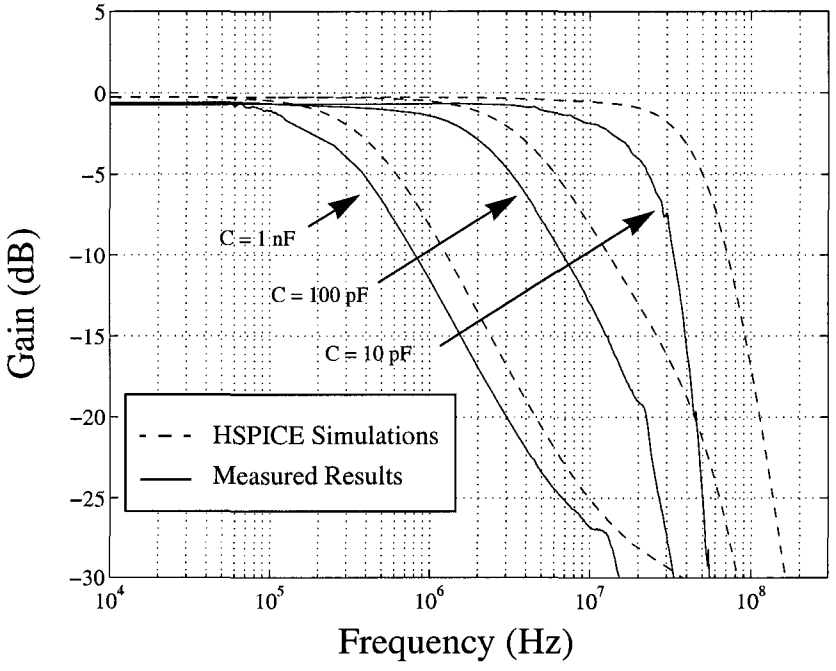


Figure 3.11: Frequency response of the log-domain integrator, I_o = 100 μA.

The most significant deviations between the simulated and measured responses occurred at high bias levels and at high frequencies. At a bias current level of I_0 = 100 μA, a significant drop in the measured frequency response was observed, and can be seen in both figures. Also note the increased slope of filter attenuation at high frequencies and high currents, reflecting the fact that the simulations did not adequately account for parasitic capacitances, both on the chip and on the circuit board. This deviation also points to the possibility that the frequency performance (specifically, the base transit time) of the lateral bipolar transistor has been underestimated during the device modelling.

These issues aside, it has been demonstrated that the 3-dB frequency of the filter can be tuned by almost two decades, and that an experimentally measured 3-dB frequency of 15 MHz or higher can be achieved with these devices.

3.3.3 - Linearity and Distortion Performance

All log-domain filter circuits suffer from distortion, due to part to non-idealities of the bipolar transistor being used. In the case of this CMOS log-domain integrator, distortion measurements are of particular interest since they provide an evaluation of the quality of the CMOS lateral bipolar transistors themselves. The distortion of this integrator has been measured in terms of two types of quantities: total harmonic distortion (THD), and the input and output third order intercept points (IIP3 and OIP3). A plot showing the simulated and experimental THD is shown in Figure 3.12 and a measurement demonstrating the calculation of the input and output intercept points is shown in Figure 3.13. Both measurements have been taken with I_0 = 10 μA, and with an input signal of 100 kHz. Additional measurements were made with I_0 = 50 μA, and the distortion performance from both sets of measurements is summarized in Table 3.3. Note that only single-tone distortion tests have been performed.

For the case where I_0 = 10μA, the experimentally measured THD at $I_{in} = 0.5I_0$ was -44.3 dB. In general for $I_{in} < I_0$, the experimentally measured THD was close to, though a few decibels higher than, the THD predicted by simulation. At an increased bias current of I_0 = 50 μA, the experimentally measured THD at $I_{in} = 0.5I_0$ was -30.1 dB, in close agreement with simulations values, but showing a significant drop from the 10 μA case.

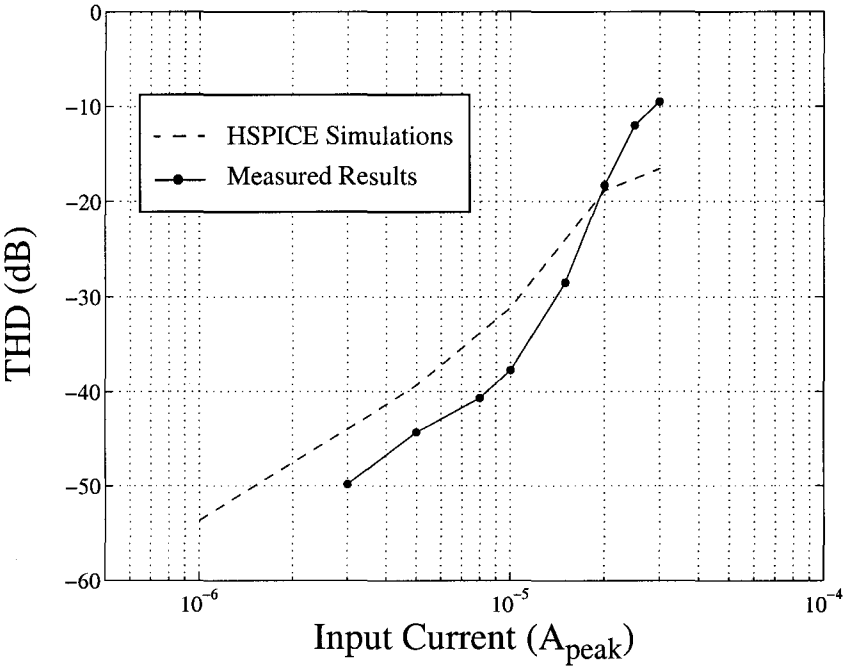


Figure 3.12: Total Harmonic Distortion, I_o = 10μA, I_{in} = 100 kHz

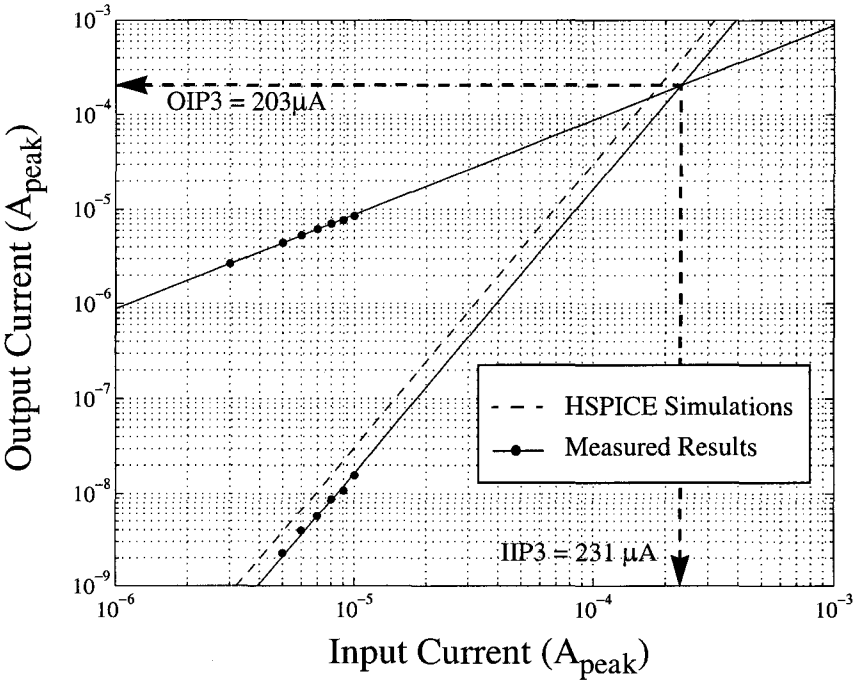


Figure 3.13: Third order intercept points, I_o = 10μA, I_{in} = 100 kHz

Table 3.3: Simulated and Measured Distortion Performance

Parameter	Bias Current	Simulation Results	Experimental Results
Total Harmonic Distortion ($I_{in} = 0.5\ I_o$)	$I_o = 10\ \mu A$	-39.4 dB	-44.3 dB
	$I_o = 50\ \mu A$	-32.0 dB	-30.1 dB
Third Order Intercept (OIP3)	$I_o = 10\ \mu A$	180 μA_{peak}	203 μA_{peak}
	$I_o = 50\ \mu A$	670 μA_{peak}	439 μA_{peak}

Further simulations have indicated that for bias currents above 50μA, the circuit distortion increases significantly, since under such conditions the collector current begins to roll off due to high injection effects (see Figure 2.14) and therefore the transistors behave less like ideal exponential devices. For the case of I_o = 10μA, the experimentally measured input and output third order intercepts were 231 μA_{peak} and 203 μA_{peak} respectively. As seen in Figure 3.13, these measurements are again close to, though slightly more favourable than, those predicted by simulation. At an increased bias of I_o = 50 μA, the experimentally measured input and output intercepts were 467 μA_{peak} and 439 μA_{peak} respectively, in this case slightly lower than the intercept points predicted by simulation.

In summary, the log-domain integrator exhibits reasonable linearity at low values of bias current, though distortion may place limitations on the maximum bias current levels (and therefore the bandwidths) at which the filter may be most useful.

3.3.4 - Noise Performance

The noise performance of the integrator is the final characteristic which has been examined. The noise performance of the CMOS integrator has been measured in terms of two quantities: the signal to noise ratio (SNR) and output noise current. Measurements of both quantities have again been made for I_o = 10 μA and I_o = 50 μA. The SNR (as well as the THD) for the case I_o = 10 μA has been plotted in Figure 3.14.

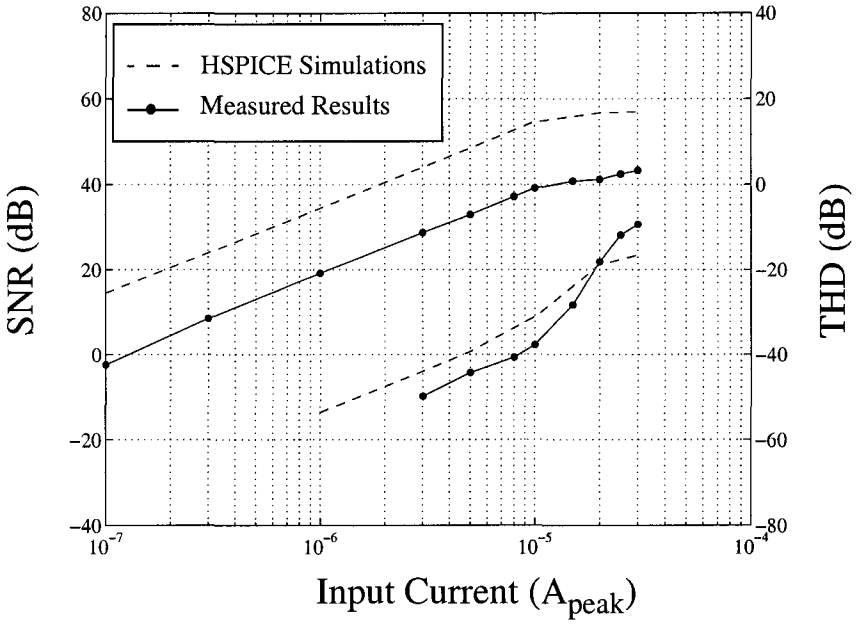


Figure 3.14: SNR (top curves) and THD (bottom curves) for I_0 = 10μA

In measuring both SNR and output noise current, a damping capacitance of 100 pF was used, and the bandwidth was chosen based on the theoretical 3-dB frequency of the circuit. For bias currents of I_0 = 10 μA and 50 μA, the measurement bandwidths were set to 640 kHz and 3.2 MHz respectively, each exceeding the experimentally measured bandwidths by more than 100 kHz. The input signal was used for measuring SNR was set to 100 kHz, as was the case for THD measurements.

From the measurement of SNR and the harmonic distortion, a third important parameter, the dynamic range can be determined. The dynamic range has been defined as the entire range over which the signal to noise and distortion ratio (SNDR) is greater than unity. The lower end of this range is shown in the figure as the point at which SNR is equal to 0 dB, while the upper end of this range at occurs when the output signal begins to clip, as shown in the figure by the significant increase in THD when $I_{in} > I_o$. The values of dynamic range, SNR, and output noise current measured for the log-domain integrator are each summarized in Table 3.4.

Table 3.4: Simulated and Measured Noise Performance

Parameter	Bias Current	Simulation Results	Experimental Results
Maximum SNR	I_o = 10 μA	57.0 dB	43.4 dB
	I_o = 50 μA	60.8 dB	44.9 dB
Total Noise Current	I_o = 10 μA	10.3 nA_{rms}	90.0 nA_{rms}
	I_o = 50 μA	37.5 nA_{rms}	176 nA_{rms}
Dynamic Range	I_o = 10 μA	59.7 dB	39.1 dB
	I_o = 50 μA	62.5 dB	45.6 dB

The maximum experimentally measured values for SNR and dynamic range each exceeded 40 dB. However, these values are approximately 15 dB lower than predicted by HSPICE simulations, most likely indicating that the experimental test set-up was far from optimal from a noise perspective. All measurements shown here have been made within a Faraday cage, an environment virtually free from electromagnetic interference. However, several possible sources of noise, including the large resistances (10 kΩ - 100 kΩ) used in generating off-chip current references, have likely contributed to the observed degradation. It is likely that the SNR and dynamic range measurements of these filters could be further improved.

An additional note regarding the noise measurements should be made. The circuit board used for measurements, as shown in Figure 3.9(b), was observed to suffer from low-frequency oscillations. An output spectrum which clearly shows this behaviour is given in Figure 3.15. For this plot, I_o = 50 μA, I_{in} = 30 μA_{peak} at 200 kHz, and the resolution bandwidth used was 18 Hz. Though the source of the oscillations was not precisely determined, the behaviour was not found to be correlated to the operation of the circuits under test, and as such the oscillations need not be included in the spectral noise measurement. To minimize the impact of these oscillations in the noise calculations, the effective bandwidths used to measure SNR, output noise, and dynamic range were taken starting from 100 kHz. Therefore, at a resolution of 10 kHz, the first ten frequency

samples were omitted from calculations. This omission is reasonable, particularly given that upper bandwidth for all measurements exceeded the experimental integrator 3-dB frequency by 100 kHz or more, as mentioned above. The input signal, set to 100 kHz for SNR and dynamic range measurements, was therefore placed at the lower edge of the measurement bandwidth.

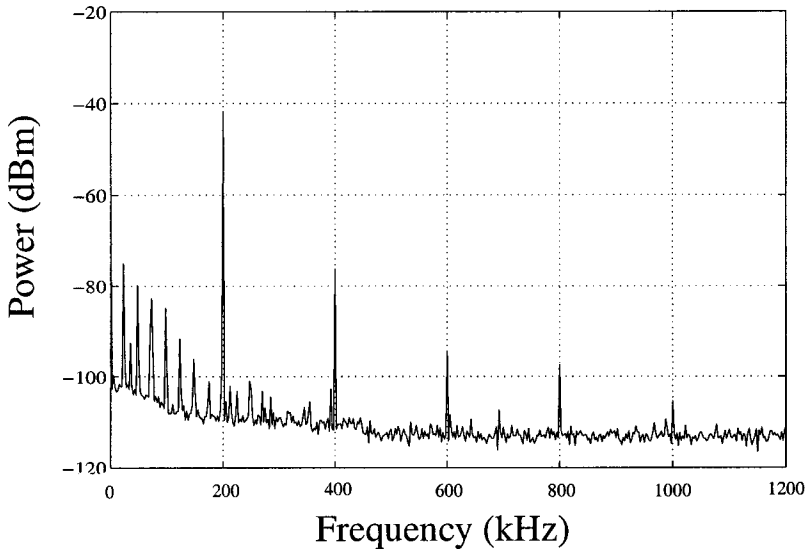


Figure 3.15: Typical output spectrum for I_0 = 50μA, I_{in} = 30μA_{peak} at 200 kHz

Overall, the maximum SNR and the dynamic range of the integrator were measured to be above 40 dB and the integrator output noise currents were measured to be between 45 nA_{rms} to 88 nA_{rms}. This measured performance can likely be further increased through improvements to the experimental test set-up.

3.3.5 - Summary of the Damped Integrator Performance

A summary of the damped integrator performance is given in Table 3.5. The measured characteristics demonstrate that the integrator is capable of operation at 10 MHz and above, that the total harmonic distortion (just before the onset of clipping) has been measured at over -40 dB for moderate levels of bias current, and that an SNR and dynamic range of over 40 dB can be achieved. Agreement between the simulated and experimentally measured results is reasonable, indicating that the model developed in Chapter 2 can be a useful tool in the design of bipolar circuity in CMOS technology.

Table 3.5: A summary of the damped integrator performance

Parameter	Bias Current	Conditions	Simulation Results	Experimental Results
Frequency Range (f_{3dB})	I_o = 1μA - 100 μA	C = 10pF	400 kHz - 38 MHz	530 kHz - 15 MHz
	I_o = 100 μA	C = 10pF - 1 nF	400 kHz - 38 MHz	220 kHz - 15 MHz
THD (I_{in} = 0.5 I_o)	I_o = 10 μA	100 kHz Input Signal	-39.4 dB	-44.3 dB
	I_o = 50 μA		-32.0 dB	-30.1 dB
Third Order Intercept (OIP3)	I_o = 10 μA	100 kHz Input Signal	180 μA_{peak}	203 μA_{peak}
	I_o = 50 μA		670 μA_{peak}	439 μA_{peak}
Maximum SNR	I_o = 10 μA	BW = 640 kHz	57.0 dB	43.4 dB
	I_o = 50 μA	BW = 3.2 MHz	60.8 dB	44.9 dB
Total Noise Current	I_o = 10 μA	BW = 640 kHz	10.3 nA_{rms}	90.0 nA_{rms}
	I_o = 50 μA	BW = 3.2 MHz	37.5 nA_{rms}	176 nA_{rms}
Dynamic Range	I_o = 10 μA	BW = 640 kHz	59.7 dB	39.1 dB
	I_o = 50 μA	BW = 3.2 MHz	62.5 dB	45.6 dB
Power *	I_o = 10 μA	-	229 μW	-
	I_o = 100 μA		1.47 mW	-

* Power listed above includes input V/I and output I/V conversion circuitry

The characteristics of this log-domain integrator compare well against subthreshold CMOS integrator implementations, and a comparison between filters designed using this integrator and other CMOS log-domain filters in the literature will be provided at the conclusion of Chapter 4. Before presenting this comparison, however, a description of a biquadratic and a third order log-domain filter will be provided. The implementation of higher order filters, based upon the CMOS log-domain integrator described above, will be the subject of the next chapter.

Chapter 4 - The Design of Bipolar Log-Domain Filters in CMOS Technology

In the previous chapters, it has been established that a lateral PNP transistor with promising characteristics can be fabricated in 0.35μ CMOS technology and that a log-domain integrator capable of operation at 10 MHz and above can be implemented using these transistors. Having performed these device-level and circuit-level investigations, attention can now be turned to a system-level implementation of log-domain filter circuits in CMOS technology.

The outline of this chapter is as follows: the first section will present the necessary theoretical background to synthesize second and higher-order filters based upon on the log-domain integrator. The second section will provide an overview of the design of a second order low pass biquadratic filter and a third order low pass elliptic filter. The next section will describe in detail the experimentally measured characteristics of the biquadratic and elliptic filters, focusing on frequency response, circuit linearity, and noise performance. The final section will compare the characteristics of the CMOS log-domain filters developed in this chapter to other log-domain filter implementations described in the literature. The comparison will demonstrate that the performance of these 0.35μ

CMOS log-domain filters is on par with the performance which could be achieved in a semicustom bipolar process, and will also demonstrate that these 0.35μ CMOS log-domain filters compare well with other CMOS log-domain filter implementations.

4.1 - Fundamentals of Log-Domain Filter Design

The following section will provide the background required to synthesize high-order log-domain filters. First, a design technique known as the operational simulation of LC ladders will be introduced. Using this technique, a signal flow graph representations of LC ladder filters can be generated, and it will be shown that the log-domain integrator of Chapter 3 can used with this representation. The design technique will be used in Section 4.2 to generate biquadratic and third order elliptic log-domain filters. Further information on the methods presented in this section can be found in [1], [6].

4.1.1 - An Overview of the Operational Simulation of LC Ladders

The operational simulation of LC ladders is a common technique for synthesizing high order active filters. The objective of this design technique is to develop a circuit which simulates each of the voltages and currents that define the behaviour of an LC (inductor-capacitor) ladder circuit. The generation of LC ladder filters is a well understood and well documented process, and by using LC ladders as prototype filters, many of the desirable characteristics of these filters, notably their low sensitivity to component variation, can be retained in an active circuit implementation (in this case, a log-domain implementation). An overview of the technique is provided below.

A general third-order low-pass LC-ladder filter is shown in Figure 4.1(a). The first step in the synthesis procedure is the development of a system of equations which completely describe the operation of the LC ladder prototype. This can be achieved by writing expressions for the voltage across each capacitor, the current in each inductor, and then applying the Kirchoff's equations to each loop and node in the LC ladder circuit. For the prototype LC shown in Figure 4.1(a), these equations can be expressed as

$$v_1 = \frac{1}{c_1} \cdot \int \left(\frac{v_i - v_1}{r_S} - i_2 \right) dt \ , \tag{4.1}$$

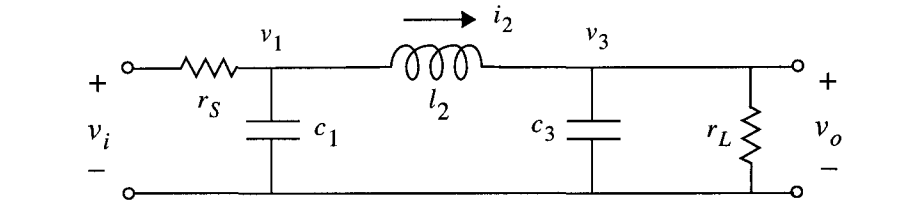
$$i_2 = \frac{1}{l_2} \cdot \int (v_1 - v_3) dt \ , \tag{4.2}$$

and

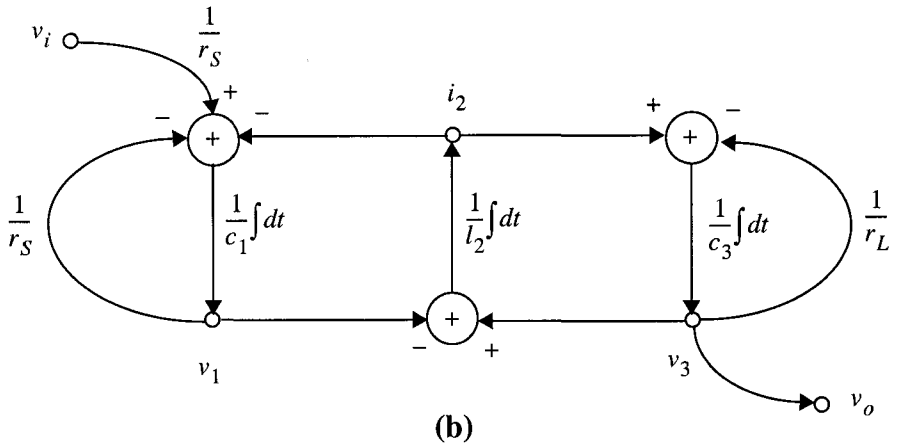
$$v_3 = \frac{1}{c_3} \cdot \int (i_2 - v_3) dt . \tag{4.3}$$

Once a system of equation has been determined, a signal flow graph representation of the filter can be constructed. For the third order low pass filter, the signal flow graph is shown in Figure 4.1(b). Note that the behaviour of the original LC prototype has now been completely described in terms of integration blocks and summing nodes. These two types of components can be realized by a variety of methods which include active-circuit implementations. Such an implementation is shown in Figure 4.1(c). (In this case, r_S and r_L have been set to unity for simplicity.) Of obvious interest here is the fact that the circuit in Figure 4.1(c) can be realized using the log-domain integrator described in the previous chapter.

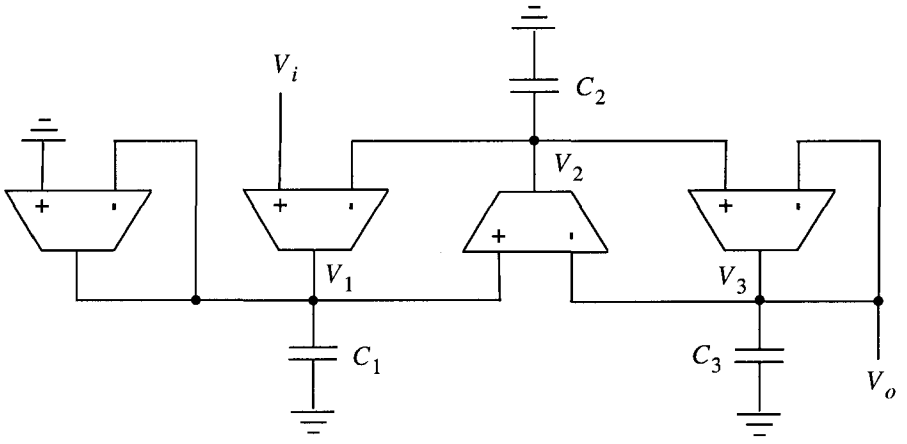
Once a circuit representation for the LC ladder has been created, the variables from the prototype filter can be mapped to the final circuit implementation. In this case, there is a direct correspondence between nodes v_1, i_2, and v_3 in Figure 4.1(b) and nodes V_1, V_2, and V_3 in Figure 4.1(c), and therefore a relationship can be derived between c_1, l_2, and c_3 in the prototype and C_1, C_2, and C_3 in the final implementation. Once this correspondence is found, the filter design is complete. However, in the case of the synthesis of a log-domain filter, some additional design steps are required in order that the non-linear nature of the log-domain integrator be taken into account. A signal flow graph representation for the log-domain integrator, which could be included in the above analysis, is discussed next.



(a)



(b)



(c)

Figure 4.1: (a) A third order low pass LC ladder filter. (b) The corresponding signal flow graph. (c) An active filter implementation based on operational simulation of original LC ladder.

4.1.2 - Operational Simulation for Log-Domain Filters

The general structure of a log-domain cell, whether it be an integrator or an entire log-domain filter, is shown in Figure 4.2(a). The EXP(x) and LOG(x) operators defined in Eqn. (3.6) and (3.7) have been explicitly shown with symbols in the figure. The diagram is simple, and yet demonstrates an important point: that the input and output signals of this cell are logarithmically compressed, though the function being implemented, denoted by h(t), has a linear representation. Conceptually, the cell can be thought of as performing the operation h(t) by first exponentially expanding the signal at the cell input, implementing the desired linear function, and then logarithmically compressing the signal at the cell output. A signal flow graph representation for a log-domain integrator which demonstrates this order of operations is shown in Figure 4.2(b). Note that this signal flow graph conforms to the log-domain integrator equation defined in Eqn. (3.13).

To continue with the example of the third order low pass filter of the previous section, the original signal flow graph can now be modified to include the log-domain integrator. This modification is shown in Figure 4.3(a). Observe that a natural cancellation of the majority of LOG(x) and EXP(x) operators naturally occurs, simplifying the filter

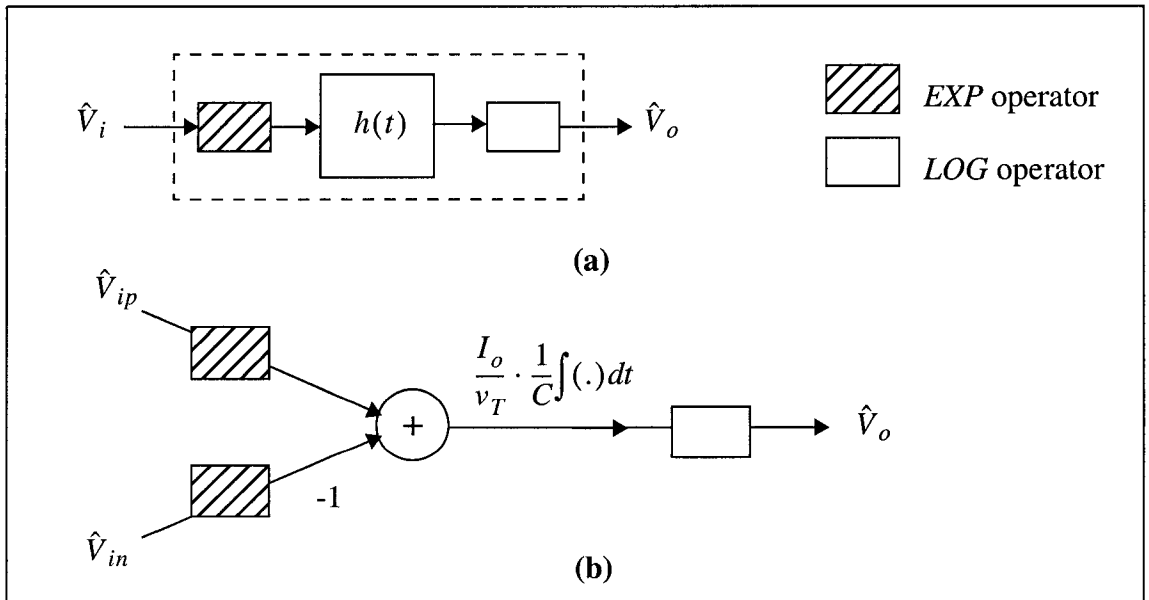


Figure 4.2: (a) A signal flow graph representation for a general log-domain cell. (b) A signal flow graph representation of the log-domain integrator.

design considerably. Due to cancellation, an entire log-domain filter can in general be implemented using only a single logarithmic compression circuit at the filter input and a single exponential expansion circuit at the filter output, and as shown by the circled LOG(x) and EXP(x) blocks in Figure 4.3(a). A circuit implementation of this signal flow graph is given in Figure 4.3(b).

Once a log-domain circuit representation for the original prototype LC ladder has been created, the variables from the LC prototype filter can be mapped to the final circuit implementation. Finding this correspondence represents the final step in the synthesis of a log-domain filter. The details of mapping the variables from the prototype to the final circuit are best demonstrated by example, as will be provided in the next section.

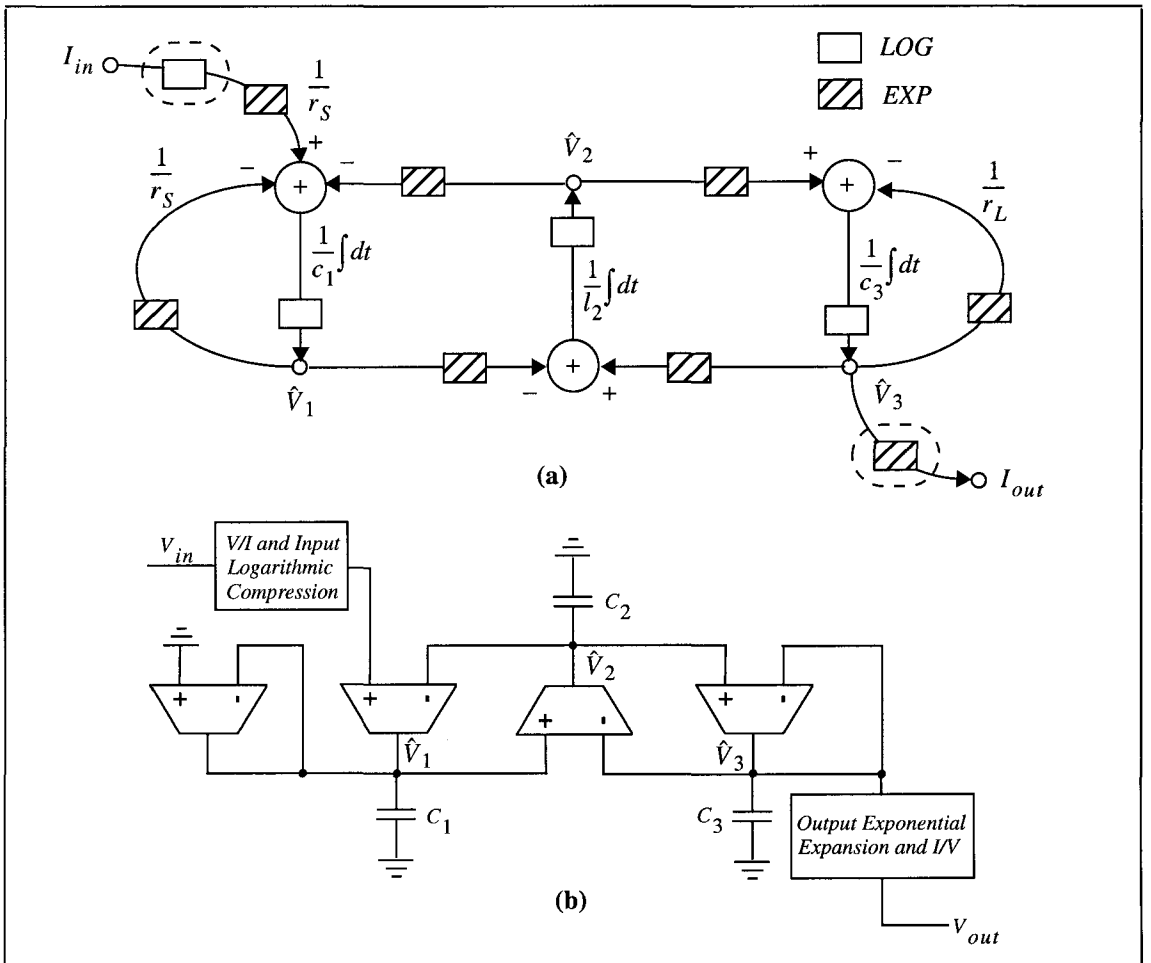


Figure 4.3: (a) A third order low pass filter log-domain signal flow graph. (b) A log-domain filter implementation of the signal flow graph.

4.2 - The Design of Second and Third Order Log-Domain Filters

The following section will provide an overview of the synthesis of a biquadratic and a third order elliptic filter. Each of the filters designed in this section will be the subject of the experimental tests presented later in this chapter. The material presented here has been adapted from [1], which provides further details on the derivation and synthesis of these filters.

4.2.1 - A Low Pass Biquadratic Log-Domain Filter

A low pass biquadratic filter can be designed starting with the LC prototype filter shown in Figure 4.4(a). This circuit has a transfer function which can be expressed as

$$\frac{V_o(s)}{V_i(s)} = \frac{1/(lc)}{s^2 + s/(rc) + 1/(lc)}. \tag{4.4}$$

By comparing this equation with the standard biquadratic form,

$$H(s) = \frac{k \cdot \omega_o^2}{s^2 + (\omega_o/Q)s + \omega_o^2}, \tag{4.5}$$

expressions for the natural frequency, ω_o, the quality factor, Q, and the gain, k, of the LC circuit can be determined, and are given by

$$\omega_o = \frac{1}{\sqrt{lc}}, \quad Q = r \cdot \sqrt{\frac{c}{l}}, \quad k = 1. \tag{4.6}$$

To simplify matters, the resistance, r, will be set to unity for the analysis which follows.

The set of equations which completely define the operation of the biquadratic prototype filter can be expressed as

$$I_1 = \frac{1}{l} \cdot \int (V_i - V_2)dt \tag{4.7}$$

and

$$V_2 = \frac{1}{c} \cdot \int (I_1 - V_2)dt. \tag{4.8}$$

A signal flow graph can be generated from these equations, as shown in Figure 4.4(b). By adding LOG(x) and EXP(x) cells to the diagram, and by mapping the variables names V_i, I_1 and V_2 to I_{in}, $\hat{V}_1$ and $\hat{V}_2$, a corresponding log-domain signal flow graph can be generated, as shown in Figure 4.4(c). In this case, the set of equations can be rewritten as

$$EXP(\hat{V}_1) = \frac{1}{l} \cdot \int \{I_{in} - EXP(\hat{V}_2)\} dt \tag{4.9}$$

and

$$EXP(\hat{V}_2) = \frac{1}{c} \cdot \int \{EXP(\hat{V}_1) - EXP(\hat{V}_2)\} dt. \tag{4.10}$$

A log-domain circuit implementation of the signal flow graph is shown in Figure 4.4(d). Note that the input compression stage has been combined with the first integrator and is implemented in a manner similar to that shown previously in Figure 3.8(b) for the damped integrator. The circuit equations at nodes $\hat{V}_1$ and $\hat{V}_2$ can be expressed as

$$EXP(\hat{V}_1) = \frac{I_o}{v_T} \cdot \frac{1}{C_1} \cdot \int \{I_{in} - EXP(\hat{V}_2)\} dt \tag{4.11}$$

and

$$EXP(\hat{V}_2) = \frac{I_o}{v_T} \cdot \frac{1}{C_2} \cdot \int \{EXP(\hat{V}_1) - EXP(\hat{V}_2)\} dt. \tag{4.12}$$

From a comparison of Eqns. (4.9) to (4.12), the relationship between l, c, C_1, and C_2 can be expressed as

$$C_1 = \frac{I_o}{v_T} \cdot l \ , \quad C_2 = \frac{I_o}{v_T} \cdot c \tag{4.13}$$

Finally, combining these equations with those listed in Eqn. (4.6), the natural frequency, quality factor and gain of the filter of the log-domain filter can be determined to be

$$\omega_o = \frac{I_o}{v_T} \cdot \frac{1}{\sqrt{C_1 C_2}} \ , \qquad Q = \sqrt{\frac{C_2}{C_1}} \ , \qquad k = 1 \ . \tag{4.14}$$

By selecting I_o, C_1, and C_2, the design of the log-domain filter is complete. A simplified circuit schematic for the complete biquadratic filter is shown in Figure 4.5.

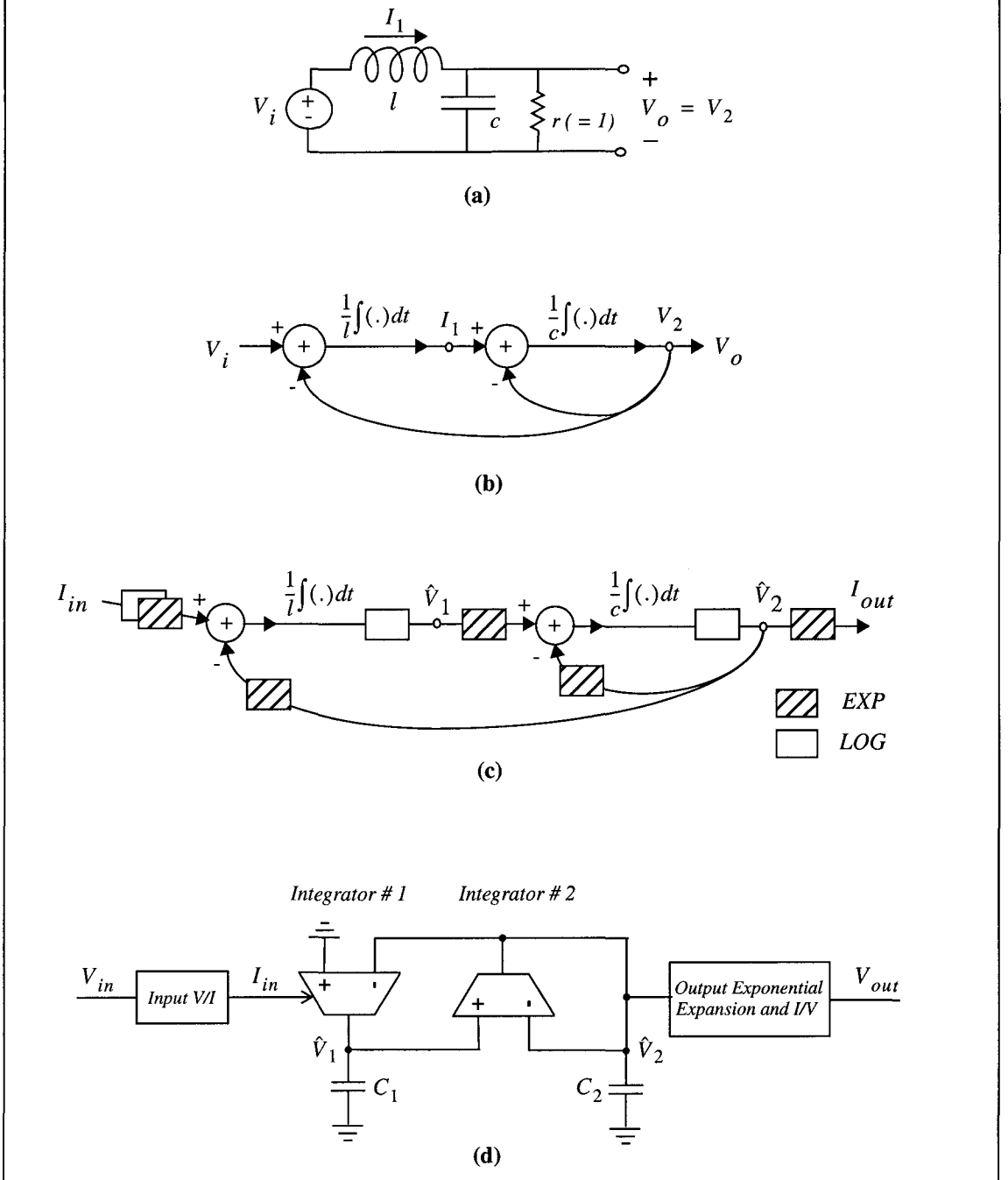


Figure 4.4: (a) The prototype biquadratic LC filter. (b) The prototype signal flow graph. (c) The log-domain signal flow graph. (d) The log-domain circuit implementation.

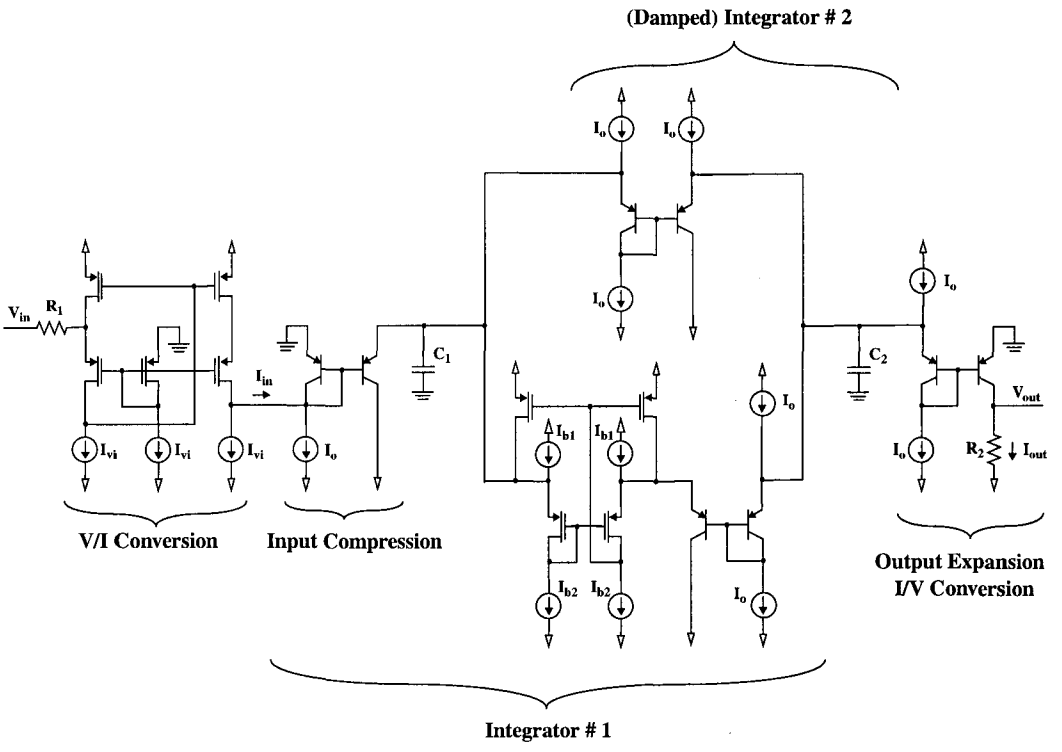


Figure 4.5: A simplified schematic of the final biquadratic filter implementation.

4.2.2 - A Low Pass Third Order Elliptic Log-Domain Filter

A low pass third order elliptic filter can be designed starting with the LC ladder prototype filter shown in Figure 4.6(a). Once again, to simplify the analysis, the values of the input and output resistance in the prototype have been set to unity. The set of equations which completely define the operation of the filter can be expressed as

$$V_1 = \frac{1}{c_1} \cdot \int \left\{ V_i - V_1 - I_2 - c_4 \frac{d}{dt}(V_1 - V_3) \right\} dt \ , \tag{4.15}$$

$$I_2 = \frac{1}{l_2} \cdot \int \{ V_1 - V_3 \} dt \ , \tag{4.16}$$

and

$$V_3 = \frac{1}{c_3} \cdot \int \left\{ I_2 - V_3 + c_4 \frac{d}{dt}(V_1 - V_3) \right\} dt \ . \tag{4.17}$$

These equations can be manipulated in order to simplify the derivative terms, resulting in

$$V_1 = \frac{1}{c_1 + c_4} \cdot \int \left\{ V_i - V_1 - I_2 + c_4 \frac{d}{dt}(V_3) \right\} dt \ , \tag{4.18}$$

$$I_2 = \frac{1}{l_2} \cdot \int \{ V_1 - V_3 \} dt \ , \tag{4.19}$$

and

$$V_3 = \frac{1}{c_3 + c_4} \cdot \int \left\{ I_2 - V_3 + c_4 \frac{d}{dt}(V_1) \right\} dt \ . \tag{4.20}$$

A signal flow graph can be generated from these equations, as shown in Figure 4.6(b). By adding LOG(x) and EXP(x) cells to the diagram, and by mapping the variables names V_i, V_1, I_2, V_3 and V_{out} to I_{in}, $\hat{V}_1$, $\hat{V}_2$, $\hat{V}_3$, and I_{out}, a corresponding log-domain signal flow graph can be generated, as shown in Figure 4.6(c). In this case, the set of equations can be rewritten as

$$EXP(\hat{V}_1) = \frac{1}{c_1 + c_4} \cdot \int \left\{ I_{in} - EXP(\hat{V}_1) - EXP(\hat{V}_2) + c_4 \frac{d}{dt}(\hat{V}_3) \right\} dt \ , \tag{4.21}$$

$$EXP(\hat{V}_2) = \frac{1}{l_2} \cdot \int \{ EXP(\hat{V}_1) - EXP(\hat{V}_3) \} dt \ , \tag{4.22}$$

and

$$EXP(\hat{V}_3) = \frac{1}{c_3 + c_4} \cdot \int \left\{ EXP(\hat{V}_2) - EXP(\hat{V}_3) + c_4 \frac{d}{dt}(\hat{V}_1) \right\} dt \ . \tag{4.23}$$

Note that the log-domain filter cannot be directly implemented from the above equations, since we do not have a functional block analogous to a log-domain differentiator. However, as is the case in other active filter technologies, the realization of the differentiator can be approximated by placing a single capacitor placed between the $\hat{V}_1$ and $\hat{V}_3$, nodes of the circuit [1]. (Indeed, a floating capacitor placed between the V_1 and V_3 nodes was used to generate the zero in the transfer function of the original LC ladder prototype.) The corresponding log-domain filter implementation is shown in Figure 4.6(d).

The circuit equations[1] generated from this figure are given by

$$EXP(\hat{V}_1) = \frac{I_o}{v_T} \cdot \frac{1}{C_1 + C_4} \cdot \int \left\{ I_{in} - EXP(\hat{V}_1) - EXP(\hat{V}_2) + \frac{v_T C_4}{I_o} \cdot \frac{d}{dt}(EXP(\hat{V}_3)) \right\} dt \ , \quad (4.24)$$

$$EXP(\hat{V}_2) = \frac{I_o}{v_T} \cdot \frac{1}{C_2} \cdot \int \{ EXP(\hat{V}_1) - EXP(\hat{V}_3) \} dt \ , \quad (4.25)$$

and $$EXP(\hat{V}_3) = \frac{I_o}{v_T} \cdot \frac{1}{C_3 + C_4} \cdot \int \left\{ EXP(\hat{V}_2) - EXP(\hat{V}_3) + \frac{v_T C_4}{I_o} \cdot \frac{d}{dt}(EXP(\hat{V}_3)) \right\} dt \ . \quad (4.26)$$

From a comparison of Eqns (4.21) to (4.26), the relationship between the circuit elements can be expressed as

$$\{C_1, C_2, C_3, C_4\} = \frac{I_o}{v_T} \cdot \{c_1, l_2, c_3, c_4\} \quad (4.27)$$

As the final step, the values of the capacitors and inductors for the prototype filter would be determined based on the desired filter specifications. For an elliptic filter, these can be read from filter tables [35] or determined with computer-aided design tools. Once these values have been mapped to the log-domain filter implementation according to Eqn. (4.27), the filter design is complete. A simplified circuit schematic for the complete third order elliptic filter is shown in Figure 4.7.

The biquadratic and elliptic filters described above have been fabricated and tested, and an experimental characterization of these filters will be provided in the next section. It will be demonstrated that filters with desired responses can be generated using the synthesis methods presented above.

1. These equations have been generated using an approximation that $e^{\hat{V}_1/v_T} = e^{\hat{V}_3/v_T}$, as described in detail in [1], and is the reason why the realization of the differentiator function is only "approximate".

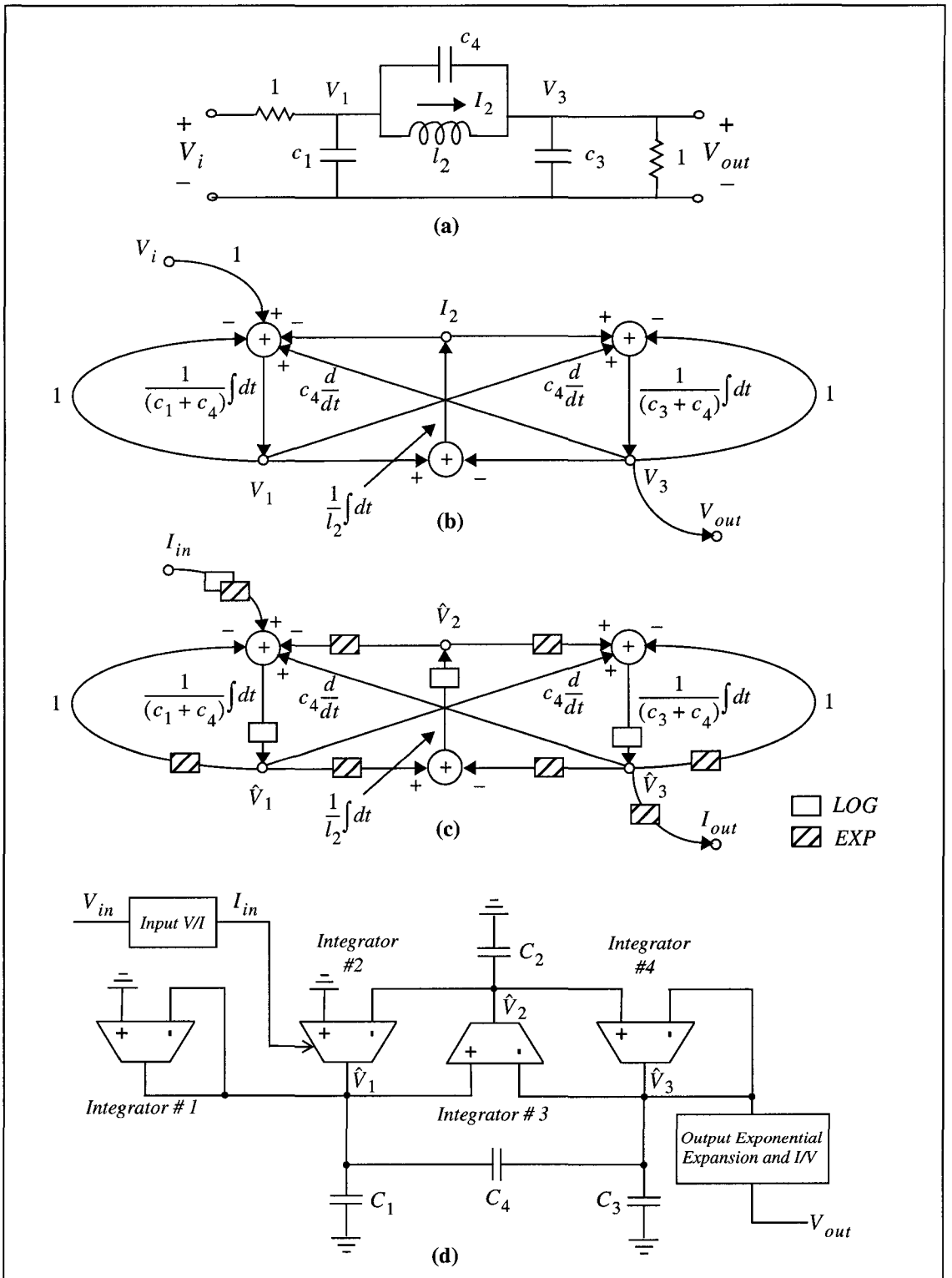


Figure 4.6: (a) The prototype elliptic LC ladder filter (b) The prototype linear signal flow graph (c) The log-domain signal flow graph (d) The log-domain-circuit implementation

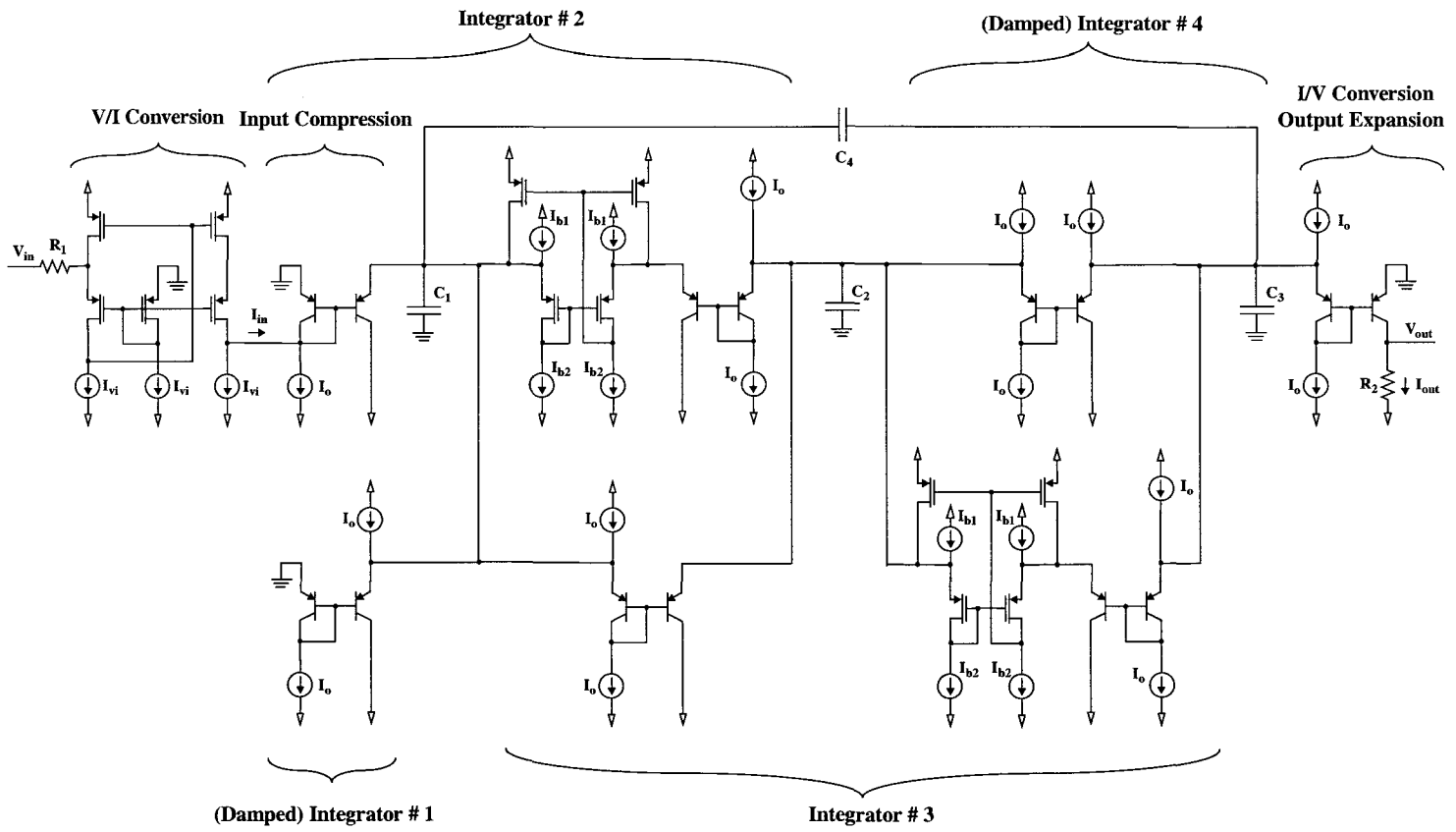


Figure 4.7: A simplified schematic of the final elliptic filter implementation

4.3 - Experimental Results

This section will discuss the experimental performance of biquadratic and elliptic low pass filters fabricated in 0.35μ CMOS technology. The three categories of tests have been used to characterize the filter performance: frequency response, linearity, and noise performance. In the final section of this chapter, a comparison between the measured performance versus other filters described in the literature will be provided. First, the circuit under test and the test conditions will be described.

4.3.1 - Description of the Log-Domain Filter Test Circuits

The biquadratic and elliptic filters used in testing are shown in Figures 4.5 and 4.7. These circuit diagrams have been simplified for visual clarity, though all measurements have been made using the complete integrator circuitry shown in Figures 3.5 to 3.7.

Several different ranges of capacitor values for both types of filters were used, and are listed in Table 4.1. The theoretical cut-off frequencies (based on ideal transfer functions) for bias currents of I_o = 100 μA have been listed in each case. The biquadratic filters (Filter #1 - #3) have been designed to have a constant quality factor of $\sqrt{2}$, and were implemented with external capacitors. The elliptic filters (Filters #4 - #6) have each been designed to have a maximum passband ripple of 1 dB and a stopband attenuation of 30 dB. Filters #5 and #6 were implemented with integrated capacitors, while Filter # 4 was implemented with external capacitors.

The input and output resistors for the biquadratic filter were set to 500 Ω, while the input and output resistors for the elliptic filter were set to 500 Ω and 1 kΩ respectively. The doubled value of output resistance of the elliptic filter was used to compensate for the 6 dB passband attenuation present in original LC ladder prototype filter.

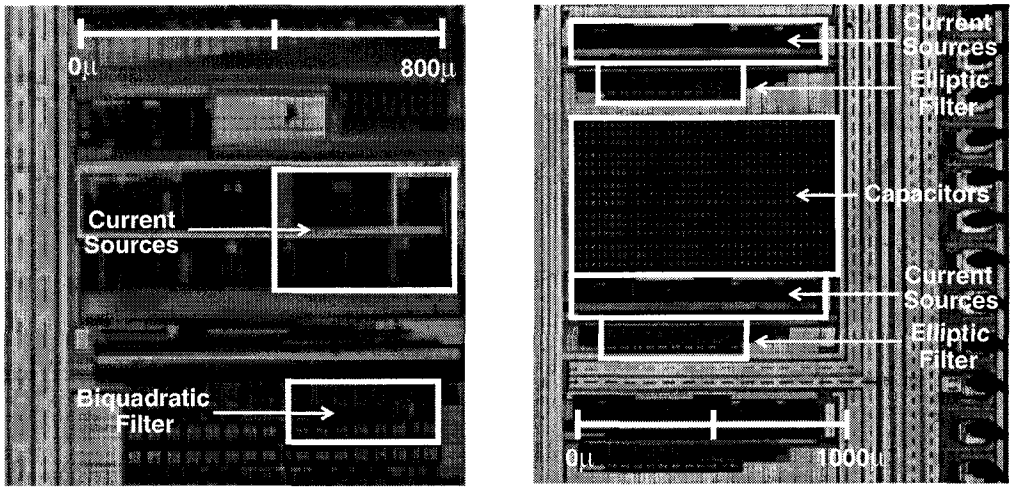
The values of I_o, I_{b1}, I_{b2}, I_{vi}, and I_{sh} could be independently controlled with off-chip references. For current biases from I_o = 10 μA to 100 μA, the values of I_{b1}, I_{b2} and I_{vi} were set to be equal to I_o, but for current biases with I_o < 10 μA, I_{b1} I_{b2}, and I_{vi} were kept fixed at 10 μA. A value of I_{sh} = 5 μA was used in all tests described in this section.

Table 4.1 - Capacitor values used for biquadratic and elliptic filter testing

	Filter Type	Capacitor Values	Theoretical Cut-Off Frequency (I_o = 100μA)
Filter # 1	Biquadratic	C_1 = 200 pF, C_2 = 100pF	4.5 MHz
Filter # 2		C_1 = 100 pF, C_2 = 50 pF	9.0 MHz
Filter # 3		C_1 = 50 pF, C_2 = 25pF	18 MHz
Filter # 4	Elliptic	C_1 = 275 pF, C_2 = 125 pF, C_3 = 275 pF, C_4 = 50 pF	4.0 MHz
Filter # 5		C_1 = 110 pF, C_2 = 50 pF, C_3 = 110 pF, C_4 = 20 pF	10 MHz
Filter # 6		C_1 = 44 pF, C_2 = 20 pF, C_3 = 44 pF, C_4 = 8 pF	25 MHz

The power supplies used in testing the circuit were V_{DD} = 2.5 V, AGND (analog ground) = 2.0 V, and V_{SS} = 0 V. The frequency response was once again found to be slightly improved by lowering the V_{DD} to between 2.35 V and 2.45 V, and most measurements were taken from this slightly lowered voltage. The bias voltage of the cascoded transistors within the integrator were kept at 0.55 V above V_{SS} for all tests described here.

The log-domain filters were manufactured in 0.35μ CMOS technology. A microphotograph of the biquadratic and elliptic filters are shown in Figure 4.8. The total die areas for the biquadratic and elliptic filter (not including current sources) were 340μ x 110μ and 515μ x 110μ respectively, and the total area for on-chip (poly/poly) capacitors in this technology was 1700μ^2 / pF. All measurements were made using a Hewlett Packard 3588A Spectrum Analyzer, a Tektronix TDS800 Oscilloscope, and Hewlett Packard 3314A Function Generator. The circuit boards used for testing were similar to that shown previously in Figure 3.9(b).



(a) (b)

Figure 4.8: (a) A microphotograph of the biquadratic filter and associated circuitry (b) A microphotograph of the elliptic filter and associated circuitry

4.3.2 - A Biquadratic Low Pass Filter

This section will describe the measured performance of a low pass biquadratic log-domain filter, and will begin with an examination of the filter frequency response. The experimentally measured response of the filter is shown in Figures 4.9 and 4.10. In the first figure, the filter capacitance has been held constant while the bias current I_o has been varied from 1 μA to 100 μA. In the second figure, a constant current of I_o = 50 μA has been used, while the filter capacitor values have been varied. The simulated response has been included in the figure for comparison.

The frequency response was very well predicted by simulation, the most significant deviation being the small amount of peaking observed when large currents and relatively small capacitances were used for the filter. Though relatively large off-chip capacitors were used for these tests, a maximum 3-dB frequency of 5.0 MHz was observed, and the ability to tune this cut-off frequency of the filter by almost two decades using the bias current, I_o, is clearly demonstrated in Figure 4.9.

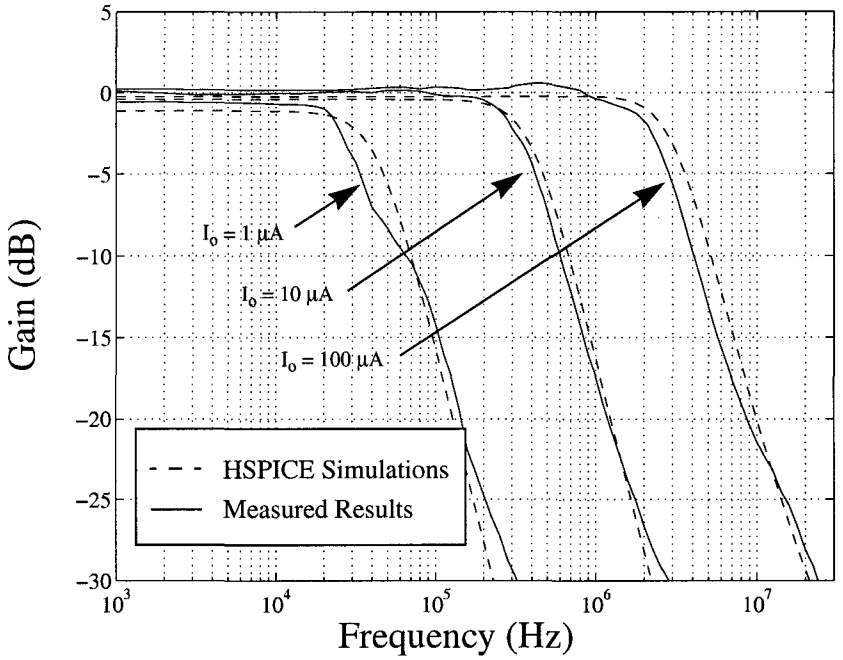


Figure 4.9 Frequency response of biquadratic filter # 1, I_o = 1 μA = 100 μA.

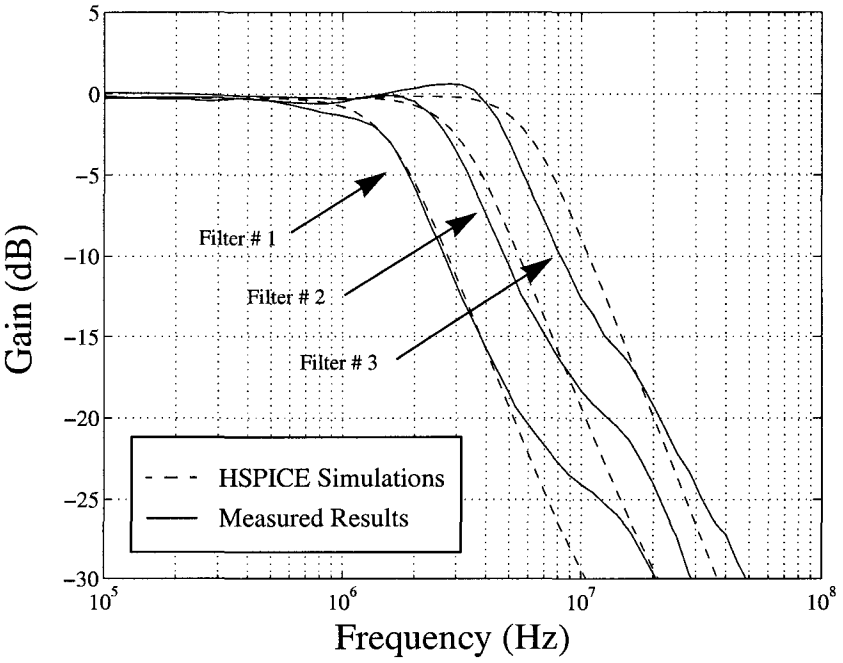


Figure 4.10 Frequency response of biquadratic filter # 1 - # 3, I_o = 50 μA

The overall linearity of the filter was characterized using measurements of both total harmonic distortion and third order intercept points, and the results of these tests are shown in Figures 4.11 and 4.12. A bias current of I_o = 10 μA and an input signal of 100 kHz was used in each case. The THD of the filter at $I_{in} = 0.5I_o$ was -43.1 dB and the output third order intercept point was measured to be 149 μA_{peak}. Both values are close to, though slightly lower than, the corresponding values measured for the single damped integrator in Chapter 3, a result which reasonable since the filter order and circuit complexity have been increased.

The noise performance of the filter was characterized using measurements of SNR, dynamic range, and output noise current. The SNR of Filter # 2, with I_o set to 10 μA and with a measurement bandwidth of 800 kHz, is shown in Figure 4.11. The maximum value of SNR was 39.6 dB, and the total dynamic range, as defined in Chapter 3, was 35.2 dB. The total output noise current over the measurement bandwidth was 121 nA_{rms}. By increasing the bias current to 50μA, both the SNR and dynamic range could be improved by several decibels. However, as in the case of the damped integrator, the measured noise-related performance is significantly lower than anticipated, suggesting that there may be significant room for improvement in the test and measurement set-up. A summary of all biquadratic filter measurements is given in Table 4.2.

An important note should be made with regard to difficulties which arose from the presence of multiple operating points within these filter circuits. As described in [17], CMOS log-domain filters which contain some form of positive feedback loops within their topologies can suffer from this effect, which can take the form of several circuit nodes settling to unintended states. This behaviour has been observed experimentally in both the biquadratic and elliptic filters described in this work. Specifically, for circuits in which capacitances were placed off-chip (in which internal circuit nodes were directly accessible) the voltages at these capacitive nodes were often observed to settle to undesired voltages. Under such conditions, the filter is inoperable.

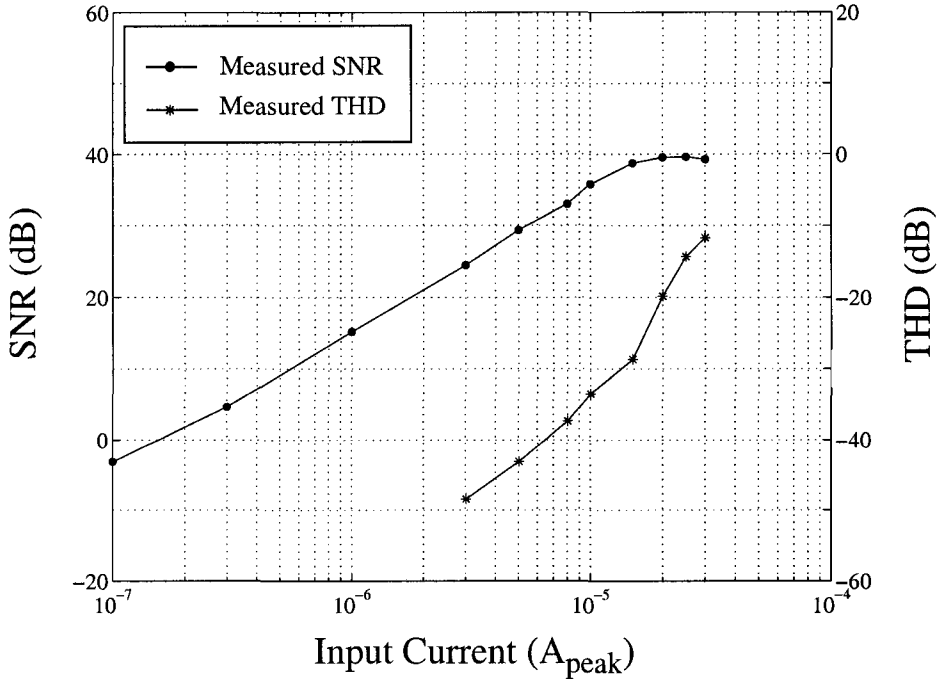


Figure 4.11: SNR and THD for filter # 2, I_o = 10μA, I_{in} = 100 kHz, BW = 800 kHz

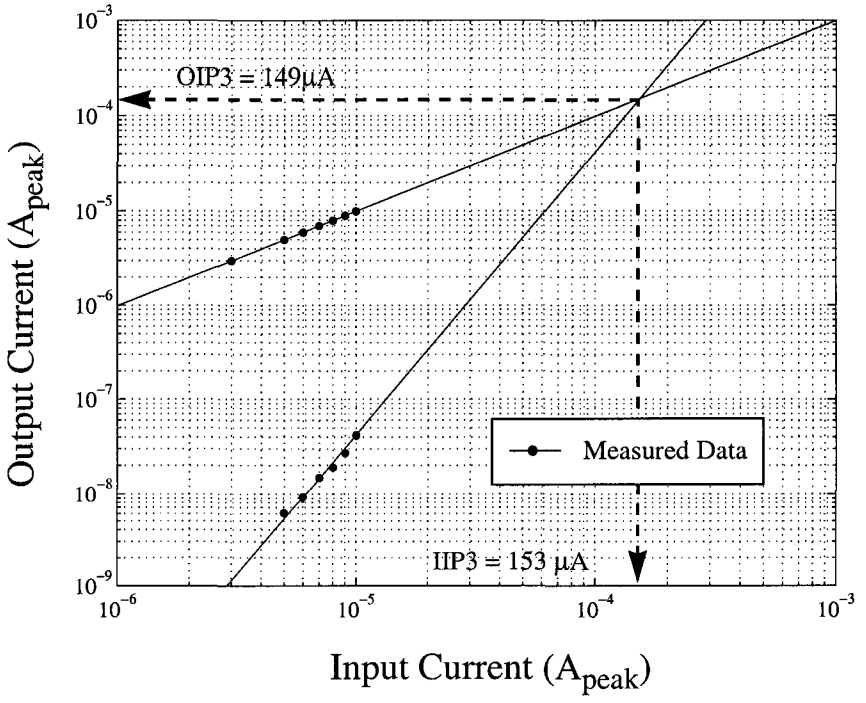


Figure 4.12 Third order intercept points for filter #1, I_o = 10μA, I_{in} = 100 kHz

Table 4.2 - A summary of the biquadratic filter performance

Parameter	Bias Current	Conditions	Experimental Results
Frequency Range (f_{3dB})	I_o = 1μA - 100 μA	Filter #1	26 kHz - 2.2 MHz
	I_o = 50 μA	Filter #1 - #3	1.6 MHz - 5.0 MHz
THD	I_o = 10 μA	Filter # 1, I_{in} = 0.5 I_o at 100 kHz	-43.1 dB
Third Order Int.	I_o = 10 μA	Filter # 1, I_{in} = 100 kHz	149 μA_{peak}
Maximum SNR	I_o = 10 μA	Filter # 2, BW = 800 kHz	39.6 dB
	I_o = 50 μA	Filter # 1, BW = 2.0 MHz	43.5 dB
Noise Current	I_o = 10 μA	Filter # 2, BW = 800 kHz	121 nA_{rms}
Dynamic Range	I_o = 10 μA	Filter # 2, BW = 800 kHz	35.2 dB
	I_o = 50 μA	Filter # 1, BW = 2.0 MHz	43.9 dB
Power per pole (simulated)	I_o = 10 μA	Filter # 1	191 μW
	I_o = 100 μA		2.09 mW

Two methods were used in an attempt to alleviate the problem: first, the switching or cycling of various filter bias currents could be used to push the filter through various states, eventually leading to the desired operating point. This method does not appear to lend itself to any fixed start-up procedure and requires a great deal of patience. However, for all but the lowest levels of current biasing, circuits could be successfully started using this method. The second method, which was implemented on the most recent chip submissions, involved the inclusion of switches which could be used to temporarily force various internal nodes to predetermined voltages. This method was not found to be very effective, since the filters could not function with switches turned on, and would generally return to previous undesired states once switches were turned off. The first of the two methods was generally found to be preferable.

A detailed investigation of the locations and origins of the multiple operating points of these biquadratic and elliptic filters was not undertaken, though it would be strongly recommended that this issue be examined if research using this CMOS circuit topology is continued in the future. A method for determining the existence of multiple operating points is described in [17], and a technique which may possibly eliminate such operating points is described in [36].

4.3.3 - A Third Order Elliptic Low Pass Filter

This section will describe the experimentally measured performance of a low pass elliptic log-domain filter, and will begin with the filter frequency response. The experimentally measured response of the filter is shown in Figures 4.13 and 4.14. In each plot, the bias current has been held constant at 10 μA and 100 μA respectively while the filter capacitance has been varied. The simulated elliptic frequency responses have been included for comparison.

The overall response of the elliptic filter was far less ideal than in either the damped integrator or the biquadratic filter cases shown previously. First, it should be mentioned that the elliptic filter was not observed to function at low values of bias current due to the existence of multiple operating points as described in the previous section. In addition, there was an unexpected peak in the response at approximately 20 MHz which has masked the location of the zero in the elliptic transfer function for I_0 = 100 μA (though based on the slope of the response, the zero must have been present). The measured stopband attenuation, designed for 30 dB, was measured to be between only 16 and 28 dB. There is also significant peaking in the response near the cut-off frequency, though such peaking can be significantly reduced simple using simple techniques such as resistive lead compensation.

Despite these issues, the two plots demonstrate that an elliptic filter can be implemented using the circuitry and methods described in this work, and that the filter can be tuned by means of bias current or filter capacitance as expected. The implementation of an elliptic function is significant, since it verifies that both the poles and zeros can be accurately placed, a testament to the potential of this CMOS filter design approach and technique. Also note that the measured maximum cut-off frequency of the filter was 10 MHz, a figure very difficult to achieve using subthreshold MOSFET devices.

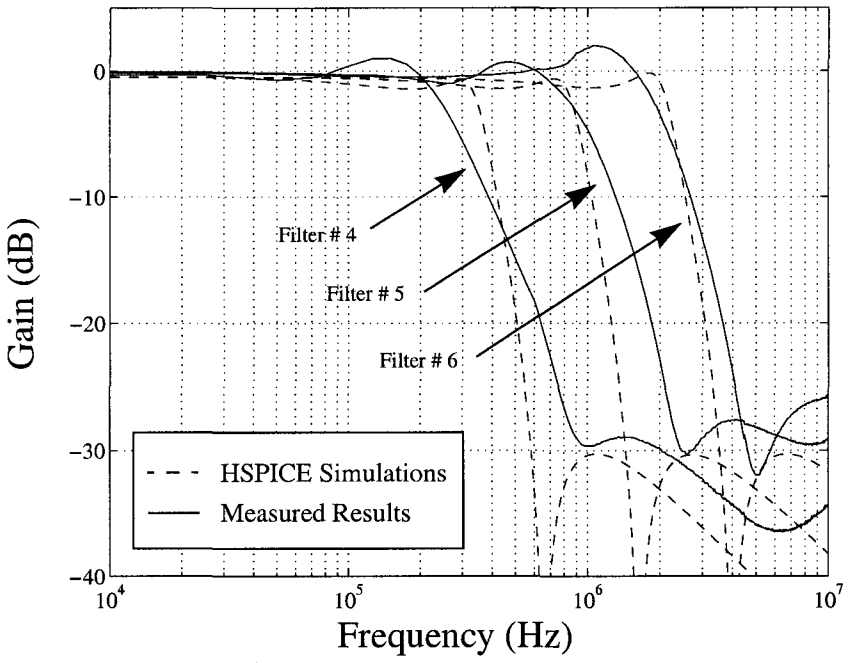


Figure 4.13 Frequency response of elliptic filter # 4- # 6, I_0 = 10 μA

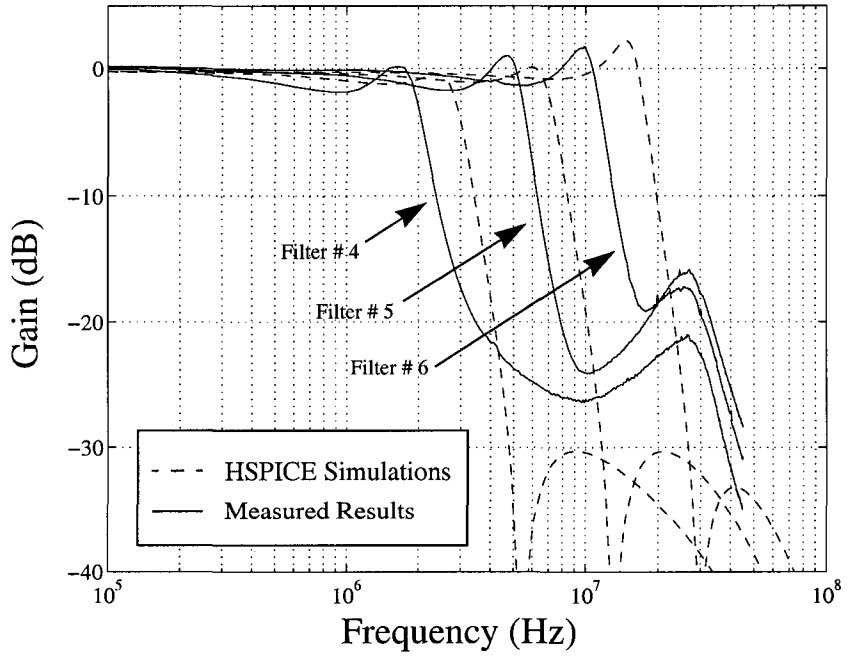


Figure 4.14 Frequency response of elliptic filter # 4 - # 6, I_0 = 100 μA

Next, the overall linearity of the filter was characterized using measurements of both the total harmonic distortion and the third order intercept points, and the results of each of these tests are shown in Figures 4.15 and 4.16. A bias current of I_o = 10 μA and an input signal of 100 kHz was used in each case. The THD of the filter at $I_{in} = 0.5I_o$ was measured to be -39.6 dB and the input and output third order intercept points were measured to be 116 μA_{peak} and 55 μA_{peak} respectively (the difference between the input and output points reflecting the fact that the output current gain of the filter is approximately 0.5). Both the THD and input third order intercept points show a slight reduction from the biquadratic filter measurements, as should be expected.

The noise performance of the filter was characterized using measurements of SNR dynamic range, and output noise current. The SNR of Filter # 6, with I_o set to 10 μA and a measurement bandwidth of 1.5 MHz, is shown in Figure 4.15. The maximum value of SNR was 31.2 dB, and the dynamic range was 34.1 dB. The output noise current over the measurement bandwidth was 134 nA_{rms}. The total noise current was slightly increased with respect to the noise current for the biquadratic filter, and as a result the measured values of SNR and dynamic range show a reduction from those given in the previous section. The value of SNR has been further reduced from the biquadratic case due to the elliptic filter current gain of being 0.5 rather than unity. By increasing the bias current to 50μA, the SNR and dynamic range could once again be improved by several decibels. As in previous cases, the measured noise-related performance is significantly lower than anticipated, and there may be significant room for improvement in the test and measurement set-up. A summary of the elliptic filter measurements are listed in Table 4.3.

The performance of the biquadratic and elliptic filters have been characterized, and a comparison to the performance of other log-domain filters described in the literature will now be provided.

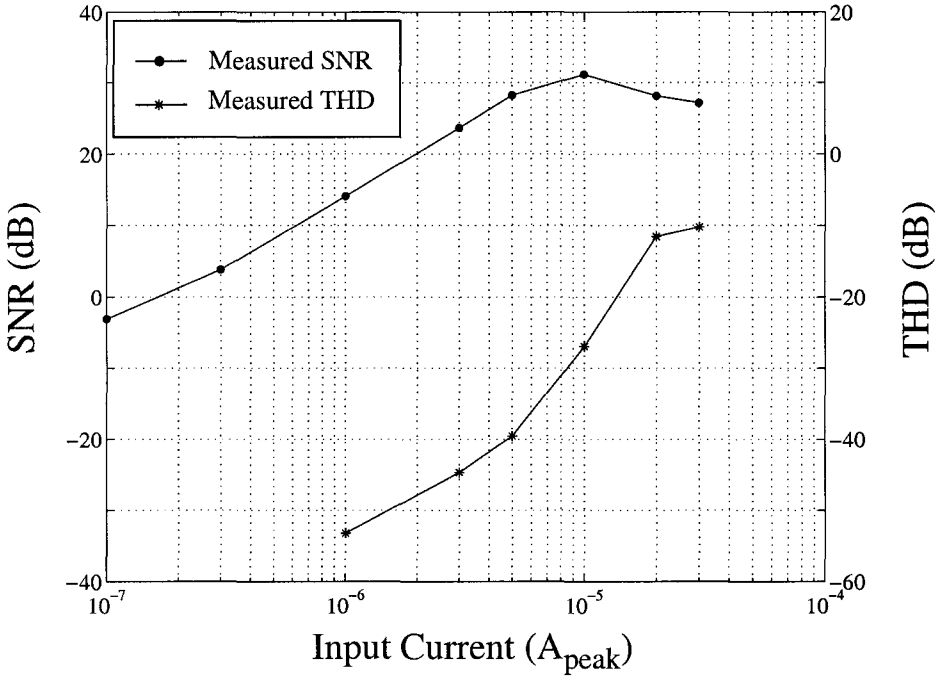


Figure 4.15: SNR and THD for filter # 6, I_o = 10μA, I_{in} = 100 kHz, BW = 1.5 MHz

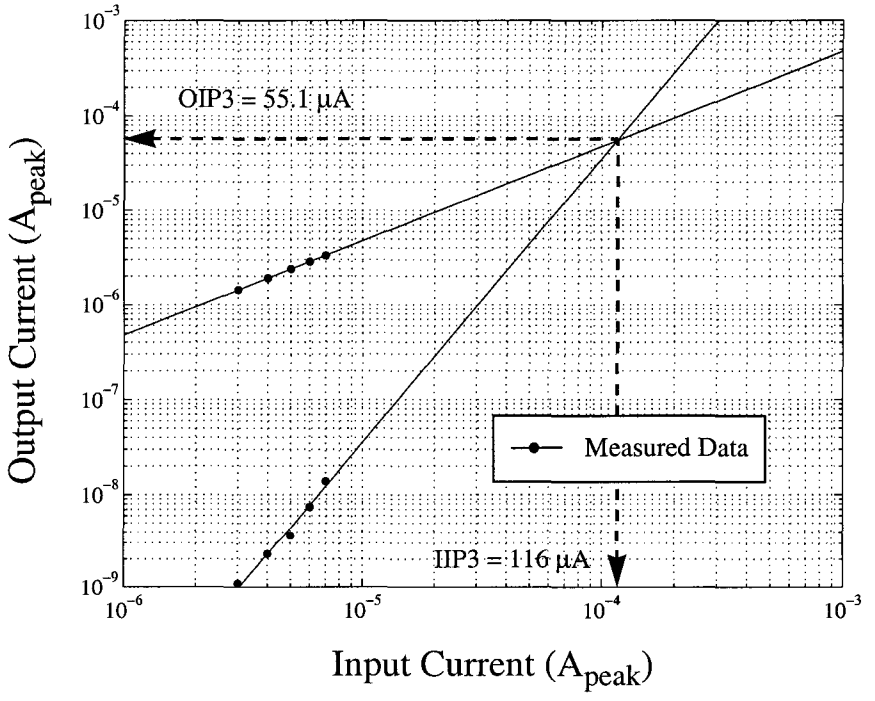


Figure 4.16 Third order intercept points for filter # 6, I_o = 10μA, I_{in} = 100 kHz

Table 4.3 - A summary of elliptic filter performance

Parameter	Bias Current	Conditions	Experimental Results
Frequency Range (f_{1dB})	I_o = 10μA - 100 μA	Filter #6	1.5 MHz - 10 MHz
	I_o = 100 μA	Filter #4 - #6	1.8 MHz - 10 MHz
THD	I_o = 10 μA	Filter # 6, I_{in} = 0.5 I_o	-39.6 dB
Third Order Int.	I_o = 10 μA	Filter # 6	55 μA_{peak}
Maximum SNR	I_o = 10 μA	Filter # 6, BW = 1.5 MHz	31.2 dB
	I_o = 50 μA	Filter # 6, BW = 7.5 MHz	35.7 dB
Noise Current	I_o = 10 μA	Filter # 6, BW = 1.5 MHz	134 nA_{rms}
Dynamic Range	I_o = 10 μA	Filter # 6	34.1 dB
	I_o = 50 μA		38.7 dB
Power per pole (simulated)	I_o = 10 μA	Filter # 6	183 μW
	I_o = 100 μA		2.25 mW

4.4 - A Comparison of Filter Performance

This section will provide a comparison of the performance of the log-domain filters designed in this work versus other log-domain filter implementations. First, a comparison will be provided between this CMOS implementation and the original bipolar implementation from which these circuits were developed. Second, a comparison will be provided between this filter implementation and all other experimentally measured CMOS implementations. It will be demonstrated that these filters compare well to other CMOS filters described in the literature.

The CMOS integrator described in this work have been mapped from an all NPN bipolar integrator described in [8]. A third order Chebychev filter was used to verify the operation of this integrator, which was implemented using Gennum GA911 technology, an inexpensive semicustom bipolar process. The measured performance specifications for this filter provide a useful benchmark for the CMOS filters described in this work. A comparison of the bipolar and CMOS filter performance is provided in Table 4.4.

Table 4.4 - Comparison of original bipolar and CMOS filter performance

Filter Type	Bipolar Implementation, Third Order Chebychev [8]	CMOS Implementation, Damped Integrator	CMOS Implementation, Biquadratic Filter	CMOS Implementation, Elliptic Filter
Filter Order	3	1	2	3
Ibias	25 μA	10 μA	10 μA	10 μA
Integrating Capacitors	22pF, 10pF, 22 pF	100 pF	100 pF, 50 pF	44pF, 20pF, 44pF, 8 pF
Cut-off Frequency	1.5 MHz	400 kHz	640 kHz	1.5 MHz
THD	-	-44.3 dB	-43.1 dB	-39.6 dB
3rd Order Int.	85 μA_{peak}	203 μA_{peak}	149 μA_{peak}	55 μA_{peak}
Maximum SNR	42.3 dB	43.4 dB	39.6 dB	31.2 dB
Output Noise Current	52.6 nA_{rms}	90 nA_{rms}	121 nA_{rms}	134 nA_{rms}
Dynamic Range	40.5 dB *	39.1 dB	35.2 dB	34.1 dB
Supply Voltage	1.2 V	2.5 V	2.5 V	2.5 V
Power / Pole	282 μW	229 μW	191 μW	183 μW

* -40 dB HD3 Measurement

Overall, the CMOS implementation shows remarkably similar performance to the original bipolar implementation. The achieved cutoff frequencies, distortion, and power consumption per pole for the CMOS filters are on par with the original bipolar implementation. The SNR, output noise current, and dynamic range compare somewhat less favourably, directly linked to the higher noise power measured in the CMOS implementation. However, simulations indicate that noise performance observed for the CMOS filters is far from the optimal performance which can be theoretically achieved. An improved circuit board for testing, specifically one which uses lower resistances (or some other means) to implement current references, could be used to improve the noise performance. If the output noise current could by reduced by a factor of two, the experimental SNR and dynamic range of the CMOS filters would be comparable to the original bipolar implementation.

While the relative performance of these CMOS filters is encouraging, it is important to point out that further implementations which make use of the bipolar integrator in [8] have been fabricated in more advanced bipolar processes, and operating frequencies from 30 - 100 MHz have been reported [11]. Such filter cut-off frequencies are likely beyond the range which can be achieved in CMOS technology using lateral PNP devices. However, the results listed in Table 4.4 are very important, since they suggest that the performance of an inexpensive bipolar-only process can be achieved in standard submicron CMOS technology by making use of the lateral PNP devices. This is perhaps the most significant finding of this work.

It is also useful to compare the performance of the filter described in this chapter to other CMOS implementations in the literature. Although many papers have been devoted to the subject of log-domain filters in CMOS technology, very few provide experimental results. Experimentally measured filter specifications reported in the literature can be found in [13]-[19] and are summarized in Table 4.5. The results published by Python and Enz [18] and Krishnapura and Tsividis [19] deserve particular attention.

Almost all log-domain filter research in CMOS technology makes use of MOS devices operating in the subthreshold regime, such as described in the work by Python and Enz, which provides a detailed characterization of a second order filter. The authors report very low distortion, excellent noise performance, and an extremely high dynamic range of 110 dB (due to class AB operation) from their circuit. The filter was designed for a micropower application and had a cut-off frequency of 45 kHz and a power consumption of 6μW / pole. Transistors were reported to enter into moderate inversion for currents over 2 μA, though the filter was shown to operate at frequencies of over 2 MHz for a bias current of 20 μA. No data on distortion or noise performance was provided for this level of bias current. The reported filter specifications at a bandwidth of 45 kHz are compared to the CMOS bipolar filter of this chapter in Table 4.5.

Table 4.5 - Comparison of experimental CMOS filter performance reported in the literature

Reference	Germanovix, Toumazou [13], [14]	Himmelbauer, Andreou [15]	D. Masmoudi et. al. [16]	Python, Enz [18]	Krishnapura, Tsividis [19]	This Work
Technology	2μ CMOS	2μ CMOS	1.6μ CMOS	0.35μ CMOS	0.25μ CMOS	0.35μ CMOS
Filter Order	-	1, 2	2	2	2	3
Ibias	~ 10 nA	10 nA	200 nA	200 nA	0.5 μA	10 μA
Integrating Capacitors	-	3.3 pF	20 pF, 200pF	30pF, 30 pF	180 pF, 180 pF	44pF, 20pF, 44pF, 8 pF
Cut-off Freq.	~ 20 kHz	15 kHz	13 kHz	45 kHz	22 kHz	1.5 MHz
THD ($I_{in} = 0.5\ I_o$)	< -40 dB		< -34 dB	< -55 dB	-45 dB	-39.6 dB
Max. SNR				62 dB		31.2 dB
Max. SNDR					44.9 dB	27.9 dB
Equivalent. Input Noise				0.20 nA_{rms}		281 nA_{rms}
Output Noise					0.25 nA_{rms}	134 nA_{rms}
Dyn. Range			57 dB*	110 dB **,†	56.1 dB **	34.1 dB
Voltage			1.2 V	1.5 V	1.5 V	2.5 V
Power / pole			2.5 μW	6 μW	2.05 μW	183 μW

* -34 dB (2%) HD3 Measurement

** -40 dB (1%) HD3 Measurement

† Class AB Operation

A recent contribution by Krishnapura and Tsividis [19] describes a log-domain filter implemented with lateral PNP devices, similar to that used in this work. The filter was also designed for micropower applications and had a cut-off frequency of 22 kHz (with a maximum cut-off frequency of 41 kHz). The design approach in the paper differed from the one described in this work, since the authors used an enhanced mode of lateral PNP operation, in which the voltage at the gate terminal was used to increase the effective beta of the transistor and significantly decrease base current, as described in [24] and [30]. Operating in this regime allows for excellent filter linearity and is very suitable for low

power applications, as indicated by the specifications given in Table 4.5. The reported noise performance was also very good. However, note that this enhanced mode of lateral PNP operation is confined to relatively low values of V_{EB}, and therefore to low currents, similar to the case of CMOS-subthreshold filters.

Several important conclusions can be drawn from the comparison in Table 4.5 and from the discussion above. In the realm of linearity and noise performance, the CMOS-subthreshold approach currently holds an advantage over the CMOS-bipolar approach described in this work. However, in terms of bandwidth, the bipolar based approach described in this work holds a performance advantage. Furthermore, since filter bandwidth is proportional to I_o / C, it is reasonable to assume that, for equal capacitance, a CMOS-bipolar based filter can always be expected to be capable of operation at significantly higher frequencies, at the obvious expense of increased power consumption. Also note that since the CMOS-bipolar filter in [19] reported significantly better noise performance and somewhat less distortion than the filters described in this chapter, and therefore it is reasonable to assume that the CMOS-bipolar circuits described in this work possess the potential for improved performance, particularly in terms of noise performance.

In summary, the performance characteristics of a second and a third order CMOS log-domain filter have been described. A comparison with the results with a bipolar-only filter implementation indicate that the performance of filters designed with lateral PNP transistors in 0.35μ CMOS technology are on par with the performance of filters which have be designed in an inexpensive bipolar process. When compared with other CMOS log-domain filter implementations, the filters described here represent the highest bandwidth CMOS log-domain filters reported to date. In addition, it is reasonable to assume that there is still significant room for improvement in several areas of the filter performance.

Chapter 5 - Conclusions

5.1 - Summary and Discussion

The development of log-domain filters in CMOS technology using lateral bipolar transistors has been the subject of this dissertation. Many significant findings have been made, and are discussed below.

In Chapter 2, a SPICE compatible model for a lateral PNP transistor fabricated in 0.35μ CMOS technology was presented. The behaviour of the overall transistor was modelled using two individual transistors representing the desired lateral device and a parasitic vertical device. The overall model has been intended to be sufficiently simple that it could be readily developed in any CMOS technology. The model required only fifteen parameters in total, each of which could be estimated based on physical considerations, extracted from straightforward device measurements, or adopted from standard information provided by the manufacturer. The model was optimized with respect to the experimentally measured DC voltage and current characteristics, and was demonstrated to be quite adequate for the purposes of simulating the responses of log domain circuits in subsequent chapters.

Note that at high frequencies, the measured filter bandwidths were somewhat lower than those predicted by SPICE circuit simulations. While this may be attributed in part to experimental setup which was not included in simulations, it may also indicate that the model parameters which affect frequency response of the lateral bipolar transistor, and in particular the base transit time, τ_f, may have been underestimated. Nonetheless, it should be

clearly stated that having the ability to work from a transistor model which accurately described the behaviour of the lateral and parasitic vertical devices, even if only at relatively low frequencies, was invaluable in the development and understanding of the behaviour of these log-domain circuits.

In Chapter 3, a log-domain integrator was designed and characterized. The integrator which made use of both lateral PNP transistors and MOSFET transistors operating in strong inversion was developed from an existing bipolar design. Many of the considerations involved in the mapping from bipolar to CMOS technology were described, and the design of the supporting circuitry was also discussed. Experimental results indicate that the integrator was capable of operation at 10 MHz and above, that the total harmonic distortion at a modulation index of 50% was better than -40 dB for moderate levels of bias current, and that the maximum SNR and dynamic range of the filter were on the order of 40 dB each. The integrator could operate from a 2.5 V supply, and consumed 229 μW of current when a bias current of 10 μA was used.

A direct comparison of simulated and experimental values was made for all measurements of the integrator. The agreement was reasonable for all measurements except for those related to the noise performance. The noise floor, calculated over a bandwidth of 640 kHz, was simulated and experimentally measured to be 10.3 nA_{rms} and 90 nA_{rms} respectively, indicating that the experimental setup was likely far from optimal. The suggests that significantly higher SNR and dynamic range can still be achieved through improvements to this experimental setup.

In Chapter 4, a biquadratic low pass filter and a third-order elliptic low pass filter were each designed and characterized. Methods of signal flow graphs and the operational simulation of LC ladders were used to design these filters, and it was verified experimentally that such methods could indeed be used to accurately synthesize the desired filter responses, including the positioning of both poles and zeros, a significant result. Experimental results indicate that the elliptic filter was capable of operation at 10 MHz, that the total harmonic distortion at a modulation index of 50% was just under -39.6 dB for moderate levels of bias current, and that the maximum SNR and dynamic range of the filter were 31.2 dB and 34.1

dB respectively. The filter could also operate from a 2.5 V supply and consumed 183 μW / pole when a bias current of 10 μA was used.

As was previously mentioned in Chapter 4, one of the significant contributions of this work is the demonstration that log domain filters in CMOS technology can be designed to operate at cut-off frequencies of up to 10 MHz and above, a figure very difficult to achieve using weakly-inverted devices. When compared with other CMOS implementation in the literature, these filters represent the highest bandwidth CMOS log-domain filters reported to date. The capacitances used in this work were in many cases placed off-chip, and in general were not the minimum size capacitors which could have been used. It is reasonable to assume that these filters could operate at higher frequencies than reported here. In addition, as in the case of the integrator, the discrepancy in simulated and measured noise performance suggest that significantly higher SNR and dynamic range could be achieved through improved experimental setup.

Also as mentioned in Chapter 4, another significant contribution of this work is the demonstration that circuit performance similar to that of a semicustom bipolar-only process could be achieved in standard submicron CMOS technology though the use of lateral PNP devices. The use of these devices is not often described in the literature, and semiconductor manufacturers generally do not provide models for such devices, yet their performance has been shown to be quite adequate for this mid-frequency application. In addition, since the overall performance of lateral bipolar transistors can be expected to improve as the dimensions of CMOS technology are reduced, such devices hold significant potential and may find a variety of uses and applications in the future.

The characteristics of a first, second, and third order log-domain filter have been thoroughly investigated. The comparison of the relative performance of the three is of great value, since it provides insight into the performance (or degradation in performance) which can be expected as further high-order filters are implemented. Overall, the measured performance is very encouraging, and it has clearly been indicated that log-domain filters can be successfully implemented in standard CMOS technology using the methods described in this work.

5.2 - Directions for future work

Since the log-domain filtering still represents a new frontier in the realm of filter design, there are several directions which this research might take in the future. To begin, it should be reiterated that measured performance reported in this work may not represent the limit of performance which can be achieved with these circuits or in this technology, and that further investigations of these limits would be of great interest. However, in more general terms, several potential directions of future research are described below.

First, since the overall performance of lateral PNP transistors can be expected to generally improve as the dimensions of CMOS technology are reduced, the implementation of such filters in 0.18μ or 0.13μ CMOS technologies would be a logical progression of this work. Note however that the improvement in performance in any particular technology cannot be taken for granted, since a vast number of variables, such as the doping levels within the process, can affect the lateral bipolar performance. Implementation of these filters in a triple-well CMOS process would also open up many new possibilities, since NPN transistors as well as PNP transistors could then be implemented. In addition, a high frequency characterization of these devices, in 0.35μ CMOS or any other submicron CMOS process, would provide both useful information for device modelling and further insight into the potential for these filters.

Secondly, an investigation of other integrator circuit topologies would be of great value. As a straightforward extension, the integrator and filters described here could be implemented using differential or class-AB structures, which could lead to significant improvements in the THD and dynamic range which could be attained with these filters. Also note that there are other integrator structures in the literature which could also be implemented in standard CMOS technology, including those in [10] and [19]. A detailed investigation of such structures could ultimately lead to the implementation of entirely new circuit topologies which best take advantage of the capabilities of CMOS processes.

Finally, if the ultimate goal in implementing log-domain filters in CMOS technology, rather than bipolar technology, is to make this filter design technique more

applicable to industry, then a thorough investigation of many practical implementation issues must be addressed. It would be of great value to examine the effects of circuit non-idealities on performance of these CMOS log-domain filters, in a similar manner to that described in [32]. It would also be crucial to obtain a full understanding of the multiple operating points which have been observed to arise in these filters, as described in [17]. Though undertaking such topics is perhaps less glamourous than many other aspects of log-domain filter design, the contribution of such investigations would be significant.

In conclusion, this dissertation has established that log-domain filters can be successfully implemented in standard CMOS technology using the lateral bipolar transistors. The CMOS log-domain filters developed in this work have the highest bandwidth of any CMOS log-domain filters reported to date. The potential for the lateral bipolar device, fabricated in standard submicron CMOS technology has also clearly been demonstrated.

Plaudite, amici, res finita est.

Appendix

A table of values which have been used in the calculation of the theoretical first-order lateral PNP model in Chapter 2 are provided below.

Table A.1: Parameter values for the lateral PNP transistor in 0.35μ CMOS technology

Parameter Descrption		Variable	Value
Emitter Doping		N_E	$1x10^{20}$ cm^{-3}
Emitter Radius		R_E	0.65 μm
Emiiter Depth		D_E	0.15 μm
Effective Emitter Width	lateral	W_E	0.65 μm
	vertical	W_E	0.25 μm
Emitter Base Junction Area	lateral	A_{EB}	0.87 μm^2
	vertical	A_{EB}	0.87 μm^2
	total	A_{EB}	1.74 μm^2
Emitter Intrinic Concentration		n_{ie}	$1.68x10^{11}$ cm^{-3}
Emitter Minority Diffusion Coefficient		D_n	6.0 cm^2 / s
Base Doping	bulk n-well	N_B	$4.0x10^{16}$ cm^{-3}
	channel region	N_B	$8.5x10^{16}$ cm^{-3}
Effective Base Width	lateral	W_B	0.30 μm
	vertical	W_B	1.3 μm
Base Intrinsic Concentration		n_i	$1.5x10^{10}$ cm^{-3}
Base Minority Diffusion Coefficient		D_p	12.5 cm^2 / s
Collector Doping	lateral	N_C	$1x10^{20}$ cm^{-3}
Base Collector Junction Area	lateral	A_{CB}	20 μm^2
	vertical	A_{CB}	92 μm^2
Base Collector Junction Capacitance	lateral	C_{BC}	10 fF
	vertical	C_{BC}	25 fF

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