Fast-Settling CMOS Operational Amplifiers with Negative Conductance Voltage Gain Enhancement

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ABSTRACT

Negative conductance voltage gain enhancement techniques which substantially increases the dc gain of an operational amplifier without degrading speed are discussed. Three fully differential CMOS op amps using the negative conductance gain enhancement technique are presented. Simulations show that for a 0.35um CMOS technology with a power supply of 3V, a dc gain of more than 94dB is achievable with the proposed amplifiers. Settling measurements with a feedback factor of $\beta = ½$ show fast settling behavior and a settling accuracy of better than 0.1% for a 1.2V input step.

INTRODUCTION

Op amps play an important role in many analog and mixed-signal systems. As device feature sizes have been reduced, the realization of high-gain amplifiers with large Gain-Bandwidth-Products (GBW) in processes with decreasing supply voltages has become challenging.

With a very high dc gain needed for precision applications, two approaches for gain enhancement have received considerable attention for many years. One is based upon gain multiplication achieved by cascading two or more lower gain stages. Although high dc gains are achievable with cascading, the accompanying excess phase shift introduces serious compensation requirements which limit the high frequency performance of cascaded amplifiers in feedback applications. The second approach achieves gain enhancement by increasing the output impedance of a basic gain stage. This approach has proven most effective at achieving high gains and high GBW with favorable power dissipation.

Three approaches for output impedance enhancement have been used. One uses cascading and a second uses both cascoding and gain boosting[1]. A third is based upon negative impedance compensation. Cascode topologies that exploit "stacking" of transistors were widely used in the past to achieve a high DC gain but they suffer from a limited output swing. As the feature sizes are reduced into the deep submicron region, the supply voltages are also being decreased. As the supply voltage is reduced, a key limitation that arises is a significant reduction in the number of devices that can be stacked between the power supply rails. For low supply processes, traditional gain enhancement techniques exploiting cascoding are becoming unviable. Very high gains are achievable with the gain-boosting/cascading approach [1] but this approach still requires one level of stacking of devices thereby making it challenging to operate with low supply voltages. The negative impedance compensation approach offers potential for the most gain enhancement with low power dissipation, low voltage operation and excellent high frequency performance however, the technique is seldom used commercially because of the high sensitivity of the gain to the negative compensating impedance inherent in existing negative impedance gain ehhancement schemes.

In this paper, we present three fully differential CMOS op amps and exploit the negative impedance gain enhancement technique with an approach that significantly reduces the gain variability to the compensating impedance.

NEGATIVE IMPEDANCE GAIN ENHANCEMENT

The basic well-known concept of gain enhancement by negative impedance compensation is shown in Fig.1a. Negative resistor R_n is placed in parallel with the output impedance of the basic amplifier. It follows from the small signal equivalent circuit of Fig.1b that the dc gain of the amplifier is

$$A_V = \frac{V_o}{V_i} = \frac{-g_{m1}}{g_{ds1} + 1/R + 1/R_n} \quad (1)$$

$$\frac{1}{R_n} = -\left(\frac{1}{R} + g_{ds1}\right) \quad (2)$$

If R_n satisfies (2), then the DC gain becomes, theoretically, infinite. Since the DC gain enhancement approach does not introduce additional internal nodes, it does not adversely reduce

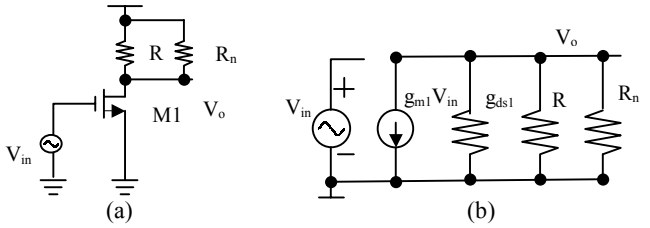

Fig. 1 Basic concept of gain enhance by negative resistance a) Basic amplifier stage b) small signal equivalent circuit

the high-frequency response of the basic amplifier so wide bandwidth can be realized. Several researchers have proposed negative impedance gain enhancement circuits. One method of implementing the negative impedance discussed by Allstot is shown in Fig 2 [2]. It uses a cross-drain-coupled differential pair to generate the negative impedance. Assuming the circuit is symmetrical and matched, a small signal analysis of this circuit gives the gain equation

$$A_d = \frac{V_o^+ - V_o^-}{V_i^+ - V_i^-} = \frac{g_{m1}}{g_{ds1} + g_{ds3} + g_{ds6} + g_{m3} - g_{m6}} \approx \frac{g_{m1}}{g_{m3} - g_{m6}} \quad (3)$$

Since the transconductance g_m of each transistor is quite sensitive to temperature and process variations, any mismatches between g_{m3} and g_{m6} may cause the gain to vary dramatically or actually cause gain sign reversal. If the gain reversal occurs, the stage will operate as a cross-coupled latch. Conventional approaches to

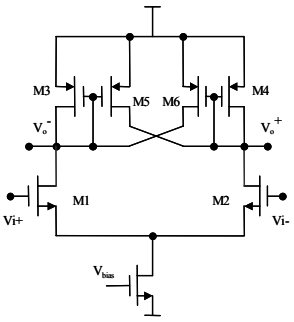

Fig. 2 Drain-coupled differential pair

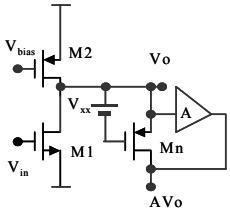

Fig. 3 Amplifier with the negative conductance

amplifier design usually avoid such operation. As such, it has been suggested that a reasonable ratio between g_{m3} and g_{m6} is 0.75 which only increases the gain by a factor of 4 [3]. Although it may appear from (3) that the major challenge for this gain enhancement technique requires matching of two transconductances, the larger challenge is actually to match a negative transconductance to the sum of a transconductance and several output conductance terms.

Nauta applied negative resistance to a simple inverter transconductor in order to increase the DC gain of the transconductor. [4-5]. In the Nauta circuit, the negative resistance is generated by applying differential output signals to matched inverters. The negative resistance is proportional to $1/\Delta g_m$. A DC gain of 46dB with a 10V power supply was reported. In [6], positive feedback was applied to generate an effective negative load conductance which is given by g_m*A+g_{ds}, where A denotes the amount of feedback applied to the gate. Although a gain of 80dB was reported in [6] with a 10V power supply voltage, the gain-bandwidth-product is only 12MHz for a 5pF capacitor load. The structure in [6] requires a high frequency, high differential gain stage to achieve conductance cancellation. This gain stage introduces internal nodes and thus limits the high-frequency response of the amplifier.

These structures all share a common characteristic, a negative transconductance is used to compensate for positive output conductances and/or transconductances and, in these approaches, achieving large gain enhancement requires the precise negative transconductance compensation for the positive output conductance. The major drawback of using negative transconductance($-g_m$) to compensate for the output conductance g_{ds} is the inability to accurately match these terms thus making large gain enhancement difficult to achieve. Also, both g_m and g_{ds} are sensitive to bias current, process and temperature but in much different ways [7]. Therefore, using a negative g_m to compensate for the positive output conductance g_{ds} offers little potential for practical applications when very high dc gains are required.

Recently, a new negative impedance gain enhancement circuit was proposed that generates a negative conductance that is only the function of g_{ds} and is not related to g_m [8]. Fig. 3 shows the concept of the negative conductance gain enhancement technique proposed by [8]. A PMOS transistor Mn is placed at the output of the basic amplifier. A low gain stage A is connected between the drain and the source of Mn. Transistor Mn is biased in the saturation region and its gate-source voltage is AC shorted. Body effects can be ignored if an n-well CMOS process is used. If the gain of the low gain stage A is larger than 1, then a negative conductance of $(1-A).g_{dsn}$ will be presented in parallel with the output conductance of the basic amplifier. The small signal dc gain of this circuit is given by the expression (4)

$$A_v \approx \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{dsmn}(1-A)} \tag{4}$$

If $g_{ds1}+g_{ds2} = (A-1).g_{dsmn}$, the gain of the amplifier will be infinite.

A simulated DC gain of 83dB and a unit-gain bandwidth of 133MHz for a 2pF capacitor load were report in [8]. This technique significantly reduces the gain variability to the negative compensating impedance and offers potential to practically achieve a very large gain enhancement with low power supply voltages while maintaining a high gain- bandwidth-product.

FULLY DIFFERENTIAL CMOS OP AMPS

Fig. 4(a) shows the transistor-level schematic diagram of a single-stage fully differential operational amplifier designed using the negative conductance gain enhancement technique. The amplifier, designated as OA1, consists of the basic differential amplifier, the low gain stage A1, the negative g_{ds} generator transistors and the biasing circuits. The common-mode- feedback (CMFB) circuit is not shown in Fig. 4(a). Transistor M16 is connected to the CMFB circuit to adjust the output common–mode voltage. The basic amplifier is composed of transistors M1-M4 and M15, M16. It is a differential-input, differential-output gain stage. The low gain stage A1 shown in Fig. 4b consists of transistors Ma1-Ma8. It is a common–source differential stage with diode-connected loads. Ma5 and Ma7 form a source-follower for voltage level shifting. The negative g_{ds} generator transistors are M7 and M8. M5, M6, M11and M12 provide biasing current for M7 and M8. M9, M10, M13 and M14 provide biasing gate-source voltage for M7 and M8. The overall DC gain of the OA1 can be derived as

$$A_{vd1} \approx \frac{g_{m1}}{gds1 + g_{ds3} + g_{ds5} + (1-A1)g_{ds7}} \tag{5}$$

where

$$A1 = \frac{g_{ma1}}{g_{ma3}} \bullet \frac{g_{ma5}}{g_{ma5} + g_{mba5}} \tag{6}$$

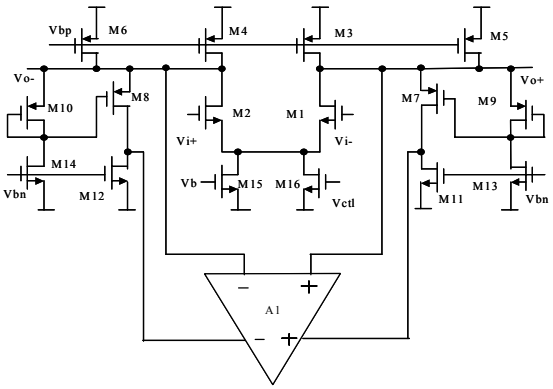

Fig. 4 (a) Schematic of the operational amplifier OA1

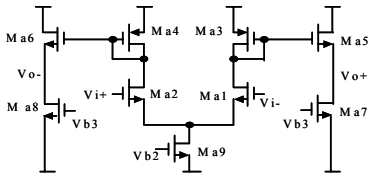

Fig. 4 (b) Schematic of the low gain stage A1

Simulation results for an implementation in a 0.35u CMOS process affirmed that Amplifier OA1 can achieve a very high open-loop dc gain at a given operating point. The amplifier was simulated in a closed-loop feedback configuration using an ideal feedback network with a feedback factor β of ½. Although the resultant feedback amplifier exhibited excellent settling performance for small input steps, it did not reach the 0.1% settling accuracy level for larger input steps because the dc gain of the amplifier OA1 is signal level dependent. Due to the non-linearity of the basic differential stage and the low gain stage, the magnitude of the overall dc gain decreases when a large input step is applied.

In order to reduce the gain sensitivity to the signal level, the modifications designated as OA2 and OA3 are shown in Fig. 5 and Fig. 6 were considered. In amplifier OA2, the low gain stage was modified from the fully differential amplifier A1 to a single-ended amplifier A2. Thus reduces the non-linearity of the low gain stage and will enhance the output signal range over which the overall gain remains very large. Correspondingly, the feedback amplifiers will achieve better settling performance for large input steps. The overall DC gain of the amplifier (II) can be derived as

$$A_{vd\,2} \approx \frac{g_{m1}}{g_{ds1} + g_{ds3} + g_{ds5} + (1 - A2)g_{ds7}} \tag{7}$$

where

$$A2 = \frac{g_{ma10}}{g_{ma11}} \bullet \frac{g_{ma12}}{g_{ma13}} \bullet \frac{g_{ma14}}{g_{ma14} + g_{mba14}} \tag{8}$$

Amplifier OA3 is a two-stage amplifier. Most of the dc gain is contributed by the first stage while the second stage only provides a gain of 2 to 3. The output signal of the first stage is reduced by a factor of 2 to 3 by adding the second stage. This circuit maintains a large overall voltage gain over a wider range

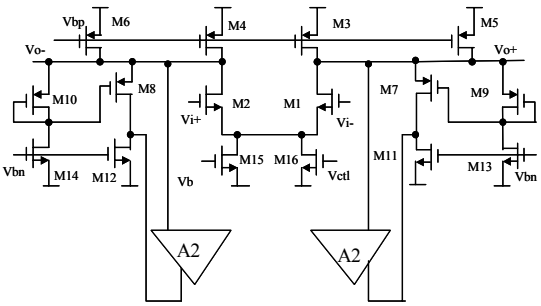

Fig. 5 (a) Schematic of the operational amplifier OA2

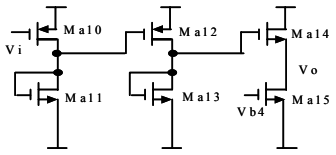

Fig. 5 (b) Schematic of the low gain stage A2

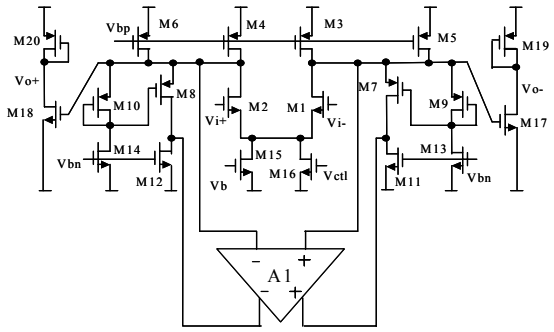

Fig. 6 Schematic of the operational amplifier OA3

of output voltages than is achievable with the other amplifiers. It thus has better settling performance for larger input step when used to build a feedback amplifier. The overall DC gain of the amplifier OA3 is given by

$$A_{vd\,3} \approx \frac{g_{m1}}{g_{ds1} + g_{ds3} + g_{ds5} + (1 - A1)g_{ds7}} \bullet \frac{g_{m17}}{g_{m19}} \tag{9}$$

where

$$A1 = \frac{g_{ma1}}{g_{ma3}} \bullet \frac{g_{ma5}}{g_{ma5} + g_{mba5}} \tag{10}$$

For two-stage amplifiers, compensation capacitors are usually needed to provide adequate phase margins. Adding compensation capacitors reduces the bandwidth resulting in a deterioration of the settling time. For amplifier OA3, since the output impedance of the first stage is very high, pole-splitting can be used to compensate the amplifier by shifting more of the power from the first stage to the second stage without adding extra compensation capacitors.

SIMULATION RESULTS

Three op amps were designed in a 0.35um CMOS process and simulated with HSPICE. BSIM II models were used and parasitic effects of all transistors were included in the simulation.

Without negative impedance compensation, the basic differential amplifier achieved a DC gain of only 42 dB. Fig. 7 shows the plot of overall open-loop AC response of the high gain amplifiers OA1, OA2 and OA3. Simulation results indicated a DC gain of more than 94dB is achievable.

The amplifiers have been simulated in a closed-loop feedback configuration using an ideal feedback network with a feedback factor of β of ½. The settling behavior is measured by applying a differential step at the inputs vi+ and vi-. Fig. 8 shows

transient step response of the feedback network using OA1 for the operational amplifier. The transient step response of the feedback

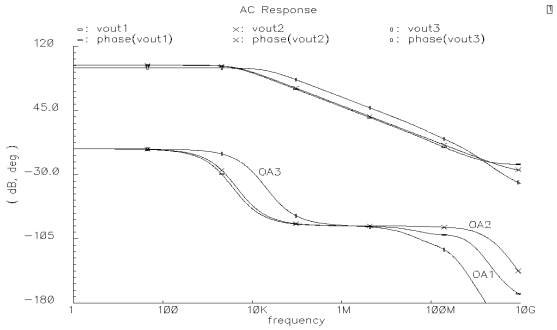

Fig. 7 AC response

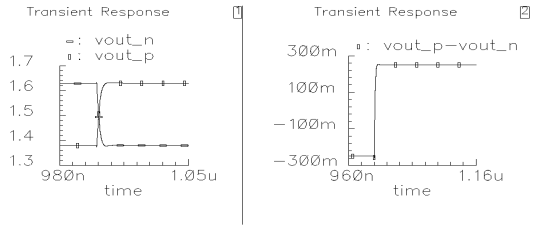

Fig. 8 Transient response of OA1 for 0.5 V step

structure using amplifiers OA2 and OA3 are shown in Fig. 9 and Fig. 10. With a 1.2V differential step input, the OA3-based circuit settles to the ideal final value at 0.1% accuracy in 7.1ns.

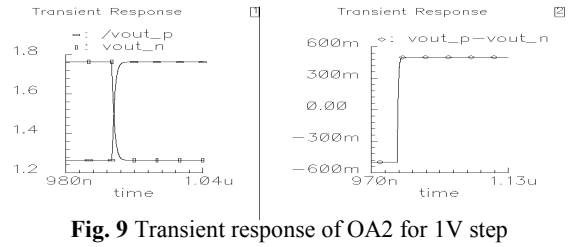

Fig. 9 Transient response of OA2 for 1V step

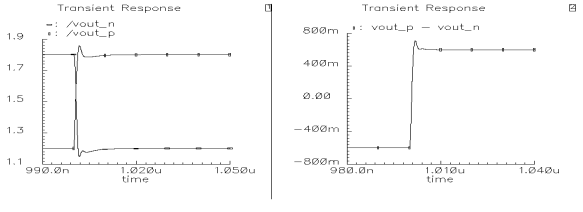

Fig. 10 Transcient response of OA3 for 1.2V step

The performance of proposed amplifiers is summarized in Table 1.

TABLE 1. Performance of the designed op amps

Op amp	OA1	OA2	OA3
DC Gain (dB)	98.1	97.7	94.6
Power dissipation (mW)	4.88	5.17	21.4
Unity-gain frequency (MHz) (C_{Load}=1pF)	241.9	335.6	554.6
Phase margin(degree) (β=1/2)	82	89	53
Settling time (200mV step)	9.9ns (0.1%)*	6.4ns (0.1%)*	7.4ns (0.1%)*
Settling time (500mV step)	8.5ns (0.2%)*	6.5ns (0.1%)*	7.3ns (0.1%)*
Settling time (1V step)	N/A	7.5ns (0.1%)*	7.2ns (0.1%)*
Settling time (1.2V step)	N/A	7.1ns (0.2%)*	7.1ns (0.1%)*

* Settling accuracy

CONCLUSION

Three fast-settling low-voltage fully differential CMOS op amps using negative conductance voltage gain enhancement have been introduced. Simulation results showed more than 50dB of gain enhancement is achievable with these structures. With a single 3V power supply voltage, settling measurements for a unity gain feedback configuration with a feedback factor of ½ show a settling time of 7.1ns to 0.1% settling accuracy for a 1.2V input step for an amplifier that dissipates 22mW of power.

ACKNOWLEDGEMENTS

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