BACKGROUND DIGITAL ERROR CORRECTION TECHNIQUE FOR PIPELINED ANALOG-DIGITAL CONVERTERS

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ABSTRACT

This paper describes a technique for digital error correction in pipelined analog-digital converters. It makes use of a slow, high resolution ADC in conjunction with an LMS algorithm to perform error correction in the background during normal conversion. The algorithm will be shown to correct for errors due to capacitor ratio mismatch, finite amplifier gain and charge injection within the same framework.

1. INTRODUCTION

Pipelined ADCs have been shown to work at very high speeds but their resolution is limited by component mismatches, op-amp gain error, offsets, charge injection errors and component non-linearities. Self calibration and background calibration techniques have been developed to correct for these non-idealities[1],[2],[3],[4]. One method for background calibration is to employ an extra pipeline stage that is used to substitute the stage being calibrated [4]. The disadvantage of this technique is that it results in fixed pattern noise due to periodic substitution of stages. Another proposed background calibration scheme inplemented for time-interleaved ADC requires the addition of a calibration signal to the input [5]. Such techniques result in a reduction of the useful dynamic range of the converter. A background error correction technique using a skip-and-fill algorithm has also been proposed in [3]. But it needs to bandlimit the signal below the nyquist rate. Moreover, none of the error correction techniques mentioned above correct for all the systematic non-idealities in a pipelined ADC within a single framework.

This paper describes a true background error correction technique for a one-bit per stage pipelined ADC using a slow, high-resolution ADC (SHADC) in conjunction with an LMS algorithm [6]. The idea can also be extended to a multi-bit per stage pipelined converter.

2. ONE-BIT PER STAGE PIPELINE A/D CONVERTER

A simplified block diagram of an ideal N-stage, 1-bit per stage, A/D converter is shown in figure 1. The most significant bits are resolved by the stages earlier in the pipeline. A most conventional switched capacitor implementation of a pipeline stage is shown in figure 2 [7]. A single ended circuit is shown for simplicity. V_{refp} is the positive reference voltage and V_{refn} is a negative reference voltage. $V_{refp} - V_{refn}$ defines the resolvable range of the A/D converter. Each

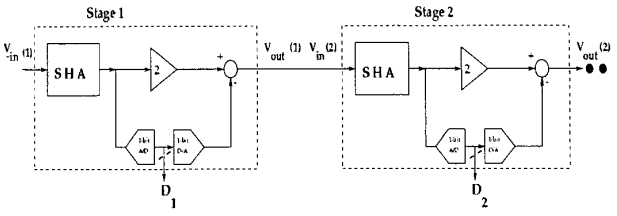

Figure 1: N-stage 1-bit per stage pipelined ADC prototype

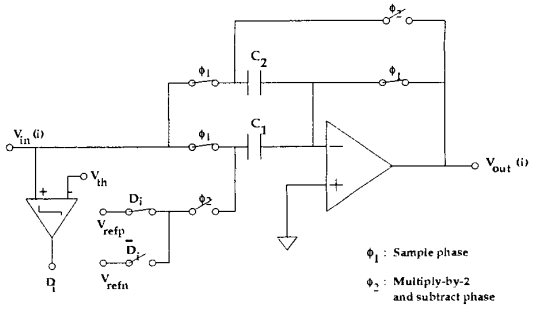

Figure 2: Switched capacitor 1-bit pipeline stage

stage consists of two nominally equal capacitors C_1 and C_2, an operational amplifier, and a comparator. During the sampling phase φ_1, the comparator produces a digital output D_i:

$$D_i = \begin{cases} 1 & \text{if } V_{in}(i) \geq V_{th} \\ 0 & \text{if } V_{in}(i) < V_{th} \end{cases} \quad (1)$$

where, V_{th} is the threshold voltage defined midway between V_{refp} and V_{refn}.

During the multiply-by-2 and subtract phase, the above cir-

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cuit generates a residue voltage $V_{out}(i)$ given by:

$$V_{out}(i) = K\left[\left(1+\frac{C_1}{C_2}\right)V_{in}(i) + \frac{C_1}{C_2}\left(-D_i V_{refp} - \bar{D}_i V_{refn}\right)\right] + \delta$$
$$K = \frac{A_0}{1+\frac{C_1}{C_2}+A_0} \quad (2)$$

where, the parameter K is an op-amp gain error coeffecient (ideally unity) and A_0 is the finite op-amp gain. Differential charge injection has been included in the above expression as an additive error term δ. Ideally, we expect the residue voltage to be:

$$V_{out}(i) = 2V_{in}(i) - D_i V_{refp} - \bar{D}_i V_{refn} \quad (3)$$

This output residue voltage is then passed to the next stage $i+1$, and the same operation continues.

3. PROPOSED DIGITAL ERROR CORRECTION SCHEME

The basic idea of the proposed digital error correction scheme is to correct for the residue errors in a non-ideal pipeline stage using a suitable set of parameters which are determined by comparing it's residue output with the ideal estimate generated using a slow high-resolution ADC(SHADC) [6]. Every stage needing error correction has an associated set of parameters. For practical values of the capacitor ratio mismatch and other non-idealities in the present technologies, error correction is usually required only for the first few stages in the pipeline. Error correction proposed in this paper involves two steps. The first step is the parameter estimation step shown in the figure 3. In this figure, the pipelined

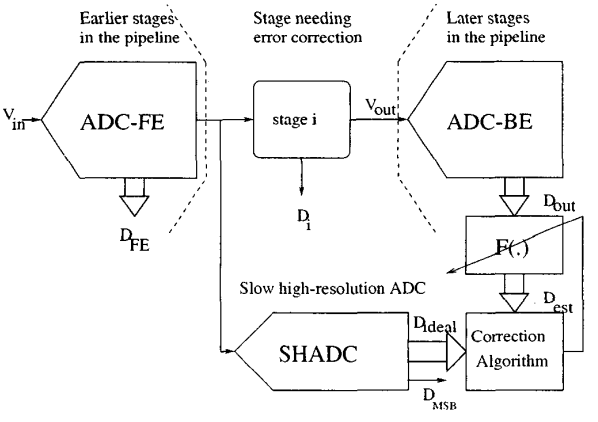

Figure 3: Basic idea of the calibration algorithm

ADC of figure 1 is represented as a combination of an ADC Front-End(ADC-FE), the stage needing error correction and an ADC Back-End(ADC-BE). ADC-FE and ADC-BE are used to represent the stages in the pipeline, before and after the stage needing error correction(calibration). The slow, high-resolution ADC (SHADC) is connected in parallel to the stage under correction. The digital output of the ADC-BE, D_{out} is processed digitally by a function F, given by:

$$D_{est} = F(D_{out}) = \alpha D_{out} + \beta \quad (4)$$

If the values of the parameters, α and β are chosen appropriately, D_{est} can be made as close to the ideal value of D_{ideal} as possible. D_{est} can now be used instead of D_{out} for the final computation of the digital output. Once the parameters for the present stage are estimated, we can start the parameter estimation for the next stage needing calibration. Parameter estimation starts with the least significant stage needing error correction till the most significant stage.
Once the parameters α, β for all the stages needing calibration are known, the second step is to compute the final digital output of the ADC. This is discussed in section 5. Another issue is to implement the correction algorithm to determine the parameter set (α, β). We use a Least-Mean-Squares approach to estimate these parameters. The algorithm is summarized below:

1. Initialize the parameter set (α, β).
2. Compute Error $\epsilon = D_{ideal} - D_{est}$ and ϵ^2
3. Modify α and β as:

$$\alpha_{new} = \alpha_{old} - \mu\frac{\partial \epsilon^2}{\partial \alpha} = \alpha_{old} + \mu\epsilon D_{out}$$
$$\beta_{new} = \beta_{old} - \mu\frac{\partial \epsilon^2}{\partial \beta} = \beta_{old} + \mu\epsilon \quad (5)$$

The μ is the update step size for the LMS algorithm. The above algorithm gives a unique desired solution for the parameter set (α, β). For ease of implementation and to get rid of multipliers, a modified sign implementation of the gradient descent algorithm can be used.

$$\alpha_{new} = \alpha_{old} + \mu sgn(\epsilon)\ sign(D_{out})$$
$$\beta_{new} = \beta_{old} + \mu sgn(\epsilon) \quad (6)$$

where, $sgn(\epsilon) = 0$ if $\epsilon = 0$, otherwise $sgn(\epsilon) = 1$ if ϵ is positive and $sgn(\epsilon) = -1$ if ϵ is negative [8], [9].

4. CORRECTION OF NON-IDEALITIES

It can be shown that D_{out} of the ADC-BE in figure 3 is an exact digital representation of the residue output V_{out} of the stage under calibration, if the following stages constituting the ADC-BE are ideal. This is a reasonable assumption for the practical values of the non-idealities in the circuit, when we use a few extra stages of pipeline at the end [6]. Similarly D_{ideal} will give an accurate digital representation of the ideal residue output (V_{ideal}) of the same stage (under calibration) for the same input. The parameter estimation described in the previous section essentially drives the V_{out} to be as close to V_{ideal} as possible. Let's assume

$V_{ref_p} = -V_{ref_n} = V_{ref}$. Let $\delta = \phi Vref$. The parameter estimation algorithm of equation 5, 6 gives a desired solution for the parameter set (α, β) of function F given by:

$$\alpha = \frac{2}{K(1+R)}, \frac{\beta}{V_{ref}} = \pm(\frac{1-R}{1+R} - \phi) \quad (7)$$

The $\pm$ sign is to account for sign changes for $V_{in} < V_{th}$ and $V_{in} > V_{th}$. In this case, we need two parameters per pipeline stage for error correction. Three special cases for equation 7 are outlined below.

1. *Capacitor ratio mismatch* R, $R \neq 1$: In this case, $K = 1$ and $\delta = 0$. The parameter set (α, β) of function F obtained via parameter estimation will be:

$$\alpha = \frac{2}{1+R}, \frac{\beta}{V_{ref}} = \pm\frac{1-R}{1+R} \quad (8)$$

   The above equation implies that we need just one parameter per stage for error correction.

2. *Finite op-amp gain error* $K \neq 1$, $K \leq 1$: In this case, $R = 1$ and $\delta = 0$. The parameters for the function F obtained will then be:

$$\alpha = \frac{1}{K}, \frac{\beta}{V_{ref}} = 0 \quad (9)$$

   In this case we just one parameter per pipeline stage for error correction.

3. *Finite op-amp gain error and capacitor ratio mismatch*: In this case, we have $\delta = 0$. The parameter set (α, β) of function F obtained via parameter estimation will be:

$$\alpha = \frac{2}{K(1+R)}, \frac{\beta}{V_{ref}} = \pm\frac{1-R}{1+R} \quad (10)$$

   In this case, we need two parameters per pipeline stage to estimate the correct residue.

In the above discussion, we have neglected the input dependency of the non-idealities like finite op-amp gain. Using more parameters, we can account for the variation of the op-amp gain over the input range. Some of the other not-so-serious non-idealities like comparator offsets and op-amp offsets can be minimized using established circuit design techniques.

5. DIGITAL COMPUTATION OF THE OUTPUT

Once the function F or equivalently the parameters (α, β) for the MSB stages needing error correction have been estimated, it can be stored in an on-chip memory. The computation of a digital output for an input voltage involves recursive processing of the raw digital output through the functions F for the MSB stages. One such implementation is given in [6]. Lets assume that the estimated function F in equation 4 for any stage l is given by F_l. Assume that there are M stages in a pipeline and let B be the required resolution (M > B). Also lets assume that the parameter estimation has been performed only for the first Q stages in the pipeline. The computation of the digital output is summarized below:

1. Start with the last calibrated stage (l = Q).
2. Set the digital estimate (D_{est})= digital code from stage l+1 onwards.
3. Get the refined digital estimate D_{est}^{new} by processing the previous digital estimate (D_{est}) by function F_l and add the bit D_l to the estimate as its MSB. Thus, we have $D_{est}^{new} = D_l F_l(D_{est}) = 2^{M-l} + F_l(D_{est})$.
4. Move to the next most significant stage (l := l -1). Assign $D_{est} := D_{est}^{new}$.
5. If l = 1 (MSB stage), go to the next step, else, go to step 3.
6. Discard the least significant M-B bits in D_{est}. This will give a B-bit corrected output code.

Parameter estimation can be run in the background during normal conversion. Since the parameters change only slowly with time, the algorithm can be run only once in few thousand cycles. This greatly relaxes the speed requirement of the SHADC, giving an opportunity to trade-off speed for high linearity in its design. The SHADC can be a self-calibrating algorithmic ADC, with a slow, high-gain op-amp [1]. The whole algorithm for calibration and computation of the output is done in the digital domain with the use of few parameters (small memory), few multiplications and additions (few multipliers and adders). These multiplications at full speed can be easily implemented using shift registers since the parameters can be expressed in binary with a sufficiently high resolution. However, multipliers will be needed to implement the LMS algorithm for parameter estimation using equation 5. However, if we use the modified LMS algorithm of equation 6, we get rid of mulitpliers as well.

6. SIMULATION RESULTS

A 10-bit resolution ADC has been simulated in MATLAB for illustration purposes. However the scheme is intended to be implemented for resolutions greater than 12bits. There are 15 stages in the pipeline. Only the first four stages are calibrated. The quantization error in the computation of the parameters for each stage has been neglected. Simulation results are presented for the pipelined ADC having capacitor ratio mismatch of $2 - 6\%$ and the op-amp gain of $300 - 500$. The parameter estimation for the ADC was stopped when all the stages, needing calibration were calibrated within 0.5LSB of the expected resolution of the rest of

the pipeline. A ramp input was given to the ADC. Figure 4 shows the uncorrected and the corrected INL profile for the ADC and similarly, figure 5 shows the DNL profile for the ADC before and after digital error correction(calibration). The results indicate that the worst case INL has been improved from ± 7.5 LSB to ± 0.5 LSB. Similarly the DNL profile indicate an improvement from 14 LSB to ± 1 LSB. Simulations for the case1 and case2 of section 4 were also carried out and the results are summarized in the table below:

Cap. Mismatch	2-6%	Nil	2-6%
Op-amp gain	80000	200-500	300-500
Uncorr. INL (LSBs)	± 5	± 4	± 7.5
Uncorr. DNL (LSBs)	10	8	14
Corr. INL (LSBs)	± 0.5	± 0.5	± 0.5
Corr. DNL (LSBs)	± 1	0	± 1

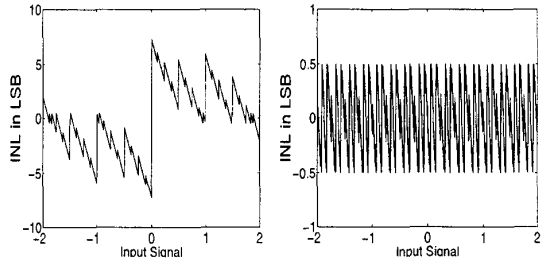

Figure 4: INL error profile: capacitor ratio mismatch 2-6%, op-amp gain 300-500 a) Before Correction b) After Error Correction

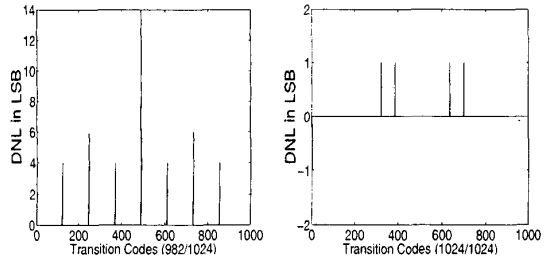

Figure 5: DNL error profile: capacitor ratio mismatch 2-6%, op-amp gain 300-500 a) Before Correction b) After Error Correction

7. CONCLUSIONS

A background error correction technique for pipelined ADC has been proposed. It has been shown to correct for systematic non-idealities like op-amp finite gain error, capacitor ratio mismatch and charge injection. Different cases for non-idealities in the pipelined converter have been formulated. The idea has been illustrated using a 10-bit converter.

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