POWER CONSTRAINED TEST SCHEDULING USING POWER PROFILE MANIPULATION

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ABSTRACT

This paper presents a novel power profile manipulation technique which reduces the testing time of the recently proposed power constrained test scheduling algorithms. The power profile manipulation technique consists of reordering and rotating test sequences and a new power approximation model. It is shown when the proposed power profile manipulation is integrated in power conscious test scheduling, savings up to 25% in testing time are achieved using benchmark circuits synthesized in AMS 0.35μm technology.

1. INTRODUCTION

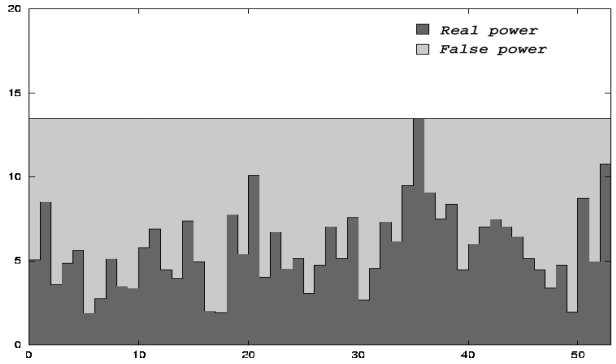
Power dissipation during testing caused by high switching activity in complementary metal-oxide semiconductor (CMOS) technology is an emerging problem due to reliability and manufacturing yield loss [3–5, 7–10]. It was reported in [10] that there is significantly higher switching activity during testing than during functional operation and hence higher power dissipation. This can decrease circuit reliability due excessive temperature and current density which cannot be tolerated by circuits designed for low power. Further, high switching activity during testing leads to manufacturing yield loss which can be explained as follows. High switching activity during testing causes high rate of current flowing in power and ground lines leading to excessive power and ground noise. This noise can erroneously change the logic state of circuit lines causing some good dies to fail the test [9]. Besides power dissipation, another important test parameter which needs to be reduced is testing time. Therefore, in order to minimize testing time under a given power constraint, test scheduling algorithms were reported recently in [3, 7, 8]. A common feature of the previous approaches is the global peak power approximation model used in guiding the test scheduling process. This is a pessimistic assumption which leads to reduced test concurrency and hence high testing time, due to the error in the power approximation model.

The aim of this paper is to introduce a novel power profile manipulation technique which when integrated in power constrained test scheduling reduces testing time.

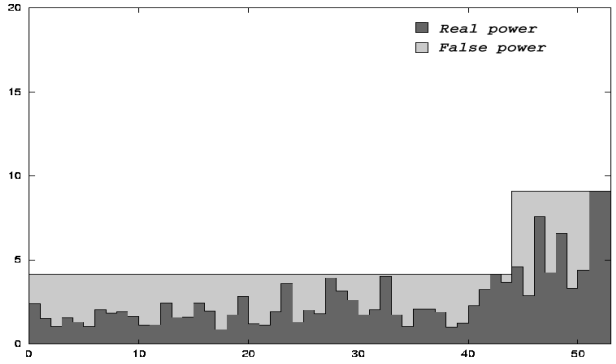
2. MOTIVATION FOR THE NOVEL POWER PROFILE MANIPULATION TECHNIQUE

Power constrained test scheduling (PCTS) algorithms aim to achieve maximum test concurrency in order to reduce the total testing time, without exceeding the power constraint given by the maximum power ratings of the device. Hence, each embedded block (EB) considered during the test scheduling process has to be characterized from the power dissipation point of view.

In order to avoid an increased computational complexity, previous PCTS approaches [3, 7, 8] approximate the power dissipation by the maximum value of instantaneous power dissipation over the entire test. This is achieved by flattening the power profiles (PP) of the EBs to their global peak value. Therefore, traditional power approximation model based on maximum instantaneous power is referred to as global peak power approximation model (GP-PAM) in this paper. Despite its low accuracy the GP-PAM guarantees that the power dissipation of the EBs is not underestimated for any time instance during the test scheduling algorithm. From the power approximation model point of the view, power definition may be classified in the following two components: *real power* caused by the variation in the instantaneous current and *false power* introduced by the error of the approximation model. Since the power definition of the EBs determines the maximum test concurrency, in order to minimize testing time under the given power constraint both real power and false power need to be reduced when employing a power approximation model during test scheduling. For an initially uncorrelated test sequence shown in Figure 1(a) the GP-PAM offers a good trade-off between accuracy and complexity. However, for regular profiles obtained through power profile manipulation technique described later in Section 3 and illustrated in Figure 1(b) the approximation error introduced by GP-PAM is not justified. This motivates the need for *novel power profile manipulation techniques using more accurate power approximation models* that will lower the testing time under the given power constraint.



(a) Initial uncorrelated test sequence using traditional GP-PAM



(b) Reordered correlated test sequence using the proposed 2LP-PAM

Figure 1: Power profiles (PP) for benchmark circuit c432

3. PROPOSED POWER PROFILE MANIPULATION TECHNIQUE

The novel power profile manipulation technique consists of reordering and rotating test sequences and a new power approximation model. The reordered test sequence generated using the algorithm summarized in Section 3.1 is combined with test sequence rotation presented in Section 3.2. The new power approximation model based on two local peak values for power dissipation is introduced in Section 3.3.

3.1. Test sequence reordering

The proposed test sequence reordering algorithm aims to generate regular power profiles for which accurate descriptions of power dissipation can be provided using low complexity power approximation models. In addition to minimizing real power, test sequence reordering also provides a suitable power profile for the new power approximation model that will reduce false power introduced in Section 2.

The algorithm takes as input the transition graph (TG) [4], where a node is associated to a vector in the test sequence and an edge is labeled with the power dissipated during transition between the vectors corresponding to the terminal nodes. A Hamiltonian path in TG is identified trying to place the low weight edges at the beginning part of the path and leaving the high weighted edges for the ending part of the path. The power dissipation is computed by summing the products between the transition count and the average power dissipation per transition of the library cell [1] associated with every node in the netlist. Figure 1 shows the PPs for the c432 circuit from ISCAS85 benchmark set [2]. It can be clearly seen that when using the proposed test sequence reordering algorithm (Figure 1(b)) a regular PP is obtained having a low activity part at the beginning and a high activity part at the end. This regular PP is used by the new power approximation model introduced in Section 3.3.

3.2. Test sequence rotation

Having obtained a reordered test sequence, now test sequence rotation is presented. Rotating the test sequence is an important feature which will be exploited by Algorithm 2 to avoid overlapping of the high activity parts of PPs of different tests that are run concurrently in the same test session. In order to facilitate test sequence rotation, a cyclic PP is obtained by adding the first vector V_0 of the ordered sequence after the last one V_{N-1}, where N is the number of test vectors. The cyclic ordered sequence in conjunction with the new power approximation model is used by the PCTS algorithm from Section 4.

3.3. New power approximation model

The aim of the proposed power approximation model is to exploit the features of PP corresponding to the reordered test sequence shown in 1(b). This is achieved by identifying the low activity part at the beginning and the high activity part at the end of the PP and approximating each part with their local peak value for power dissipation. Thus, the power dissipation of EBs can be modeled using a 4-tuple (P_{lo},L_{lo},P_{hi},L_{hi}) containing two local peak values for power dissipation of the two parts of the power profile (P_{lo},P_{hi}) and the length for each of the parts (L_{lo},L_{hi}). This new power approximation model is referred to as two local peak power approximation model (2LP-PAM) and it is shown in Figure 1(b). The 4-tuple description is determined such that the false power is reduced, and this is achieved by minimizing $P_{lo}L_{lo}+P_{hi}L_{hi}$. For example in the case of power profile shown in Figure 1(b) $P_{lo}\approx$4mW and $P_{hi}\approx$8mW, and the lengths are L_{lo}=44 and L_{hi}=8. It should be noted that $L_{lo}>L_{hi}$ which is exploited when building power compatible lists during PCTS without considerable impact in computational time.

4. POWER CONSTRAINED TEST SCHEDULING USING POWER PROFILE MANIPULATION

The previous section has shown how the power profile is manipulated using test sequence reordering and rotation which facilitates the use of the power approximation models 2LP-PAM. The aim of this section is to show how the proposed power manipulation technique is efficiently integrated into recently proposed PCTS algorithms. The non-partitioning test scheduling algorithm for unequal test lengths proposed in [3] is extended for use in conjunction with the proposed power profile manipulation technique. In the following, the integration the recently proposed PCTS algorithms are emphasized.

Algorithm 1 PCTS Using the Proposed Power Profile Manipulation

Input: test compatibility graph(TCG) and set of tests for the EBs along with their TGs
Output: power constrained test schedule and the set of reordered test sequences
1. **for each** test **do**
   reorder test sequence (Section 3.1);
   compute the 4-tuple $(P_{lo},L_{lo},P_{hi},L_{hi})$ (Section 3.3);
   endfor;
2. compute all cliques of the TCG;
3. **for each** clique C_i **in** TCG **do**
   compute the maximum power compatible lists (PCL) of C_i ;
   using Algorithm 2;
   endfor;
4 .**for each** PCL **do** generate all derived PCLs (DPCL); **endfor**;
5. generate test schedule by determining the minimum cost weighted cover for the DPCL set.

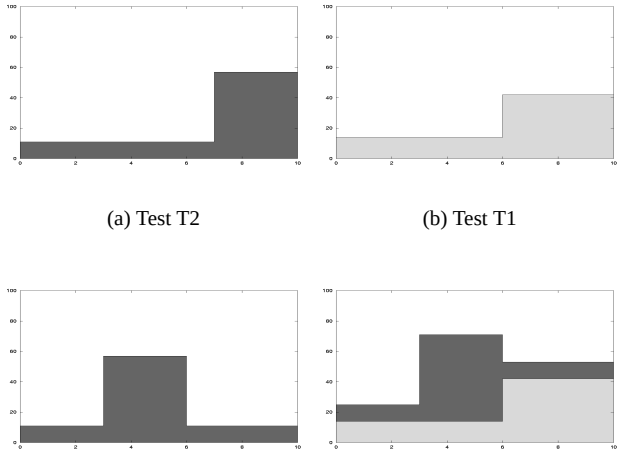
During Step 1 of the Algorithm 1 the test sequences of EBs are reordered as described in Section 3.1. Further the reordered test sequences are made cyclic according to Section 3.2, and the 4-tuple descriptions (Section 3.3) are derived from the resulting cyclic PPs. Step 2 computes all the cliques in the TCG and Step 3 generates the power compatible lists (PCL) using Algorithm 2 summarized as follows. Algorithm 2 checks the following for every subset of each test compatible clique: a) if it complies with the power constraint; and b) if the subset is a maximal, i.e. no other test with lower length than the longest test in the subset can be added to the subset without exceeding the power constraint. Having obtained the PCLs using Algorithm 2, Steps 4 and 5 of Algorithm 1 generate all the derived PCLs and a test schedule respectively.

The example shown in Figure 2 illustrates how the cyclic feature of the PP is exploited during the building of the PCLs. First test T1 (Figure 2(b)) is added to the empty test session. The value of the variable Offset from Algorithm 2 which is initially set to 0, is increased by L_{hi} of test T1, that in this particular case is 4. Next, test T2 (Figure 2(a)) is rotated left by Offset vectors obtaining the power profile shown in Figure 2(c). Finally, Figure 2(d) shows the resulting power profile of the test session composed of

Algorithm 2 Power Compatible Lists

Input: a test compatible clique C and the power constraint P_{constr}
Output: the power compatible lists W
1. W=ϕ;
2. **for each** subset S_i of tests from C **do**
   create PCL_j by arranging tests in S_i in the descending order of their length; Offset=0;Session=ϕ;
   for each test T_j **in** PCL_i **do**
   if $L_{lo_j} \geq$Offset **then** rotate left T_j by Offset vectors;
   else Offset=0; **endif**;
   Session=Session $\bigcup$ T_j; Offset=Offset+L_{hi};
   endfor;
   compute maximum power dissipation P_{max} for Session;
   if $P_{max} \leq P_{constr}$ **then**
   MaximalSet=TRUE;
   for each T_j **not in** PCL_i with length < longest length in PCL_i **do**
   if $L_{lo_j} \geq$Offset **then** rotate left T_j by Offset vectors; **endif**;
   Session'=Session $\bigcup$ T_j;
   compute maximum power dissipation P'$_{max}$ for Session';
   if P'$_{max} \leq P_{constr}$ **then** MaximalSet=FALSE; **endif**;
   endfor;
   if MaximalSet=TRUE **then** W=W $\bigcup$ PCL_j; **endif**;
   endif;
   endfor;
3. **return** W.

tests T1 and T2. It can be concluded from Figure 2(d) that the integration of the test sequence rotation (Section 3.2) in building PCLs (Algorithm 2) guarantees increased test concurrency under the given power constraint, which will lead to lower testing time. This is achieved by avoiding the overlapping of the high switching activity parts of the test sequences that belong to the same PCL, which leads to greater number of test sequences to be merged in each PCL.



(a) Test T2 (b) Test T1

(c) Test T2 rotated (d) T1 and rotated T2

Figure 2: Building power compatible lists (PCLs)

5. EXPERIMENTAL RESULTS

To show the efficiency of the proposed power profile manipulation technique, experiments were performed on a set of hypothetical systems generated using the ISCAS85 benchmark circuits [2] as EBs, and with randomly generated resource allocation graphs [3]. The designs were synthesized and technology mapped into AMS 0.35μm technology [1] in order to determine the average power dissipation per transition for each node in the netlist. The first column of Table 1 shows the number of EBs which ranges from 6 to 24. The power constraint (PC) shown in the second column ranges from 40mW to 85mW. The third and fourth column show the testing time in terms of clock cycles when power constrained test scheduling employs the traditional global peak power approximation model (GP-PAM [3]) and the proposed power profile manipulation technique using the new power approximation model (2LP-PAM from Section 3.3). The testing time for each EB is computed using ATALANTA test tool [6]. Finally, the last column of Table 1 shows the savings when employing the proposed power profile manipulation technique. It can be seen that savings in testing time up to 25% are achieved, as in the case of 24 EBs and PC equal to 55mW. On one hand for designs with a small number of EBs, improvements in testing time are achieved only for low PC values. This is due to the fact that maximum test concurrency is achieved both by the GP-PAM and the proposed 2LP-PAM approaches. On the other hand, for designs with a large number of EBs, the testing time decreases for both approaches as PC value increases. However, the proposed 2LP-PAM approach is more sensitive to small changes in the power constraint than the GP-PAM approach which leads to savings in testing time as shown in the last column in Table 1.

EBs	PC(mW)	T_{GP-PAM}(cycles)	$T_{2LP-PAM}$(cycles)	ΔT(%)
6	40	292	239	18.15
	45-80	239	239	0.00
13	40	819	819	0.00
	45	766	656	14.36
	50	713	588	17.53
	55-60	656	570	13.10
	65	570	568	0.35
	70	570	563	1.22
	75	568	548	3.52
	80-85	563	548	2.66
17	40	1112	1044	6.11
	45	1059	888	16.14
	50	914	871	7.43
	55	881	813	7.71
	60	873	798	8.59
	65	813	738	9.22
	70	813	723	11.07
	75-80	773	670	13.32
	85	738	584	2.66
24	40	832	779	6.37
	45	832	627	24.63
	50	726	612	15.70
	55	627	469	25.19
	60	612	469	23.36
	65-85	469	469	0.00

Table 1: Savings in testing time achieved by the proposed technique when compared to traditional PCTS

6. CONCLUDING REMARKS

This paper introduced a new power profile manipulation technique which can be used in conjunction with recently proposed PCTS algorithms in order to obtain lower testing time under a given power constraint. This is achieved by reordering and rotating test sequences leading to power profiles used by a more accurate power approximation model.

7. REFERENCES

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