

# A Micropower Log Domain *FGMOS* Filter

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## Abstract

In this paper, a *CMOS* implementation of a low voltage micropower logarithmic biquad based on Floating Gate *MOS* transistors (*FGMOS*) is presented. The translinear principle applied to the floating gate *MOS* transistor leads to an easy implementation of the state-space equations without using the source terminal in the loop. The voltage supply can be reduced and also there is no need of separate wells. The technique is proven in this low/band pass filter working at  $1V$  with a maximum power consumption of  $2\mu W$ . The filter parameters can be adjusted in more than two decades, being the upper frequency around  $150kHz$ .

## 1. Introduction

The actual trend towards low voltage and low power (*LV/LP*) *VLSI* design motivated by the increasing market demand on applications where the battery life is a limiting factor, has directed the analog designers' efforts to look for new design strategies that allow the analog cells to coexist on the same substrate along with massive digital system sharing the same voltage supply [1].

Filters are important building blocks appearing on the demanded products. Specifically, continuous-time filters processing large signals are very challenging, as they increase the dynamic range in a context where this can be seriously degraded. Log-domain filters arose in this framework as an alternative for implementing continuous-time filters in the current domain [2],[3]. Log-domain filters are circuits whose internal state is a logarithmic function of the input and output [4]. The transfer function is Externally Linear but Internally Nonlinear (*ELIN*) [5]. Using this approach, the capacitor voltage swings will be smaller than the input signal swings, and the supply voltage will be less restrictive. This subclass of circuits exploits the exponential characteristic of devices, which could be either *BJT* in the active region or *MOS* working in the weak inversion region. The first ones are more suitable for high frequency

applications, whereas the *CMOS* log filters are valid in systems which do not require large time constants and therefore can handle low current levels [6]. Most circuit implementations of log-domain filters published so far do not preserve the advantages of the principle in terms of low-voltage and low-power operation, as they require separated wells for some of the transistors to preserve the linearity. Also, these wells can cause instability problems, as the leakage current is the key to the circuit's multiple operating points [7].

This paper presents a log-domain second order band/low pass filter. The filter does not require separated wells for the *FGMOS* transistors working in the weak inversion region. It has been designed using the modified TransLinear (*TL*) principle for these devices which does not make use of the source terminal in the Kirchoff's law for the translinear loop [8]. The feasibility of the technique is confirmed with the design working at  $1V$ , and less than  $2\mu W$ , presenting it as a promising alternative in the context of *LV/LP* analog design.

## 2. The Filter

### A: The Floating Gate *MOS* transistor.

The key of the circuit described along this paper is the use of the Floating Gate *MOS* (*FGMOS*) transistor. A *FGMOS* transistor is a *MOS* transistor with isolated gate capacitively coupled to the inputs in a way that it is possible to achieve a weighted sum of these inputs at the floating gate node (Fig.1). The current law for this device working in the weak inversion saturation region is given by,

$$I_{DS} = I_s e^{\frac{\sum w_i V_i - V_s}{nU_T}} \quad (1)$$

where  $V_s$  is the source voltage,  $V_i$  is the voltage of the input  $i$  and all the parameters have their standard meanings. The weights are defined as:  $w_i = C_i / C_T$ , being  $C_T$  the total capacitance seen from the floating gate and  $C_i$  the

capacitance from the floating gate to the input transistor terminals.

The general advantages of using Floating Gate MOS can be found along [9]. In the context of this work, the most important ones are the following. First, this transistor makes easy the programmability, thanks to be a multiple inputs device. Second, the TL principle becomes in simple TL loop avoiding the source terminal. As a consequence, a reduction of the minimum voltage drop is obtained, enabling both lower voltage supply operation and lower power consumption. The risk of instabilities generated by leakage currents are minimized, as no independent wells are necessary. Third, voltage addition can be performed in a single device. This implies strategies for sensing common mode signals can be simplified.

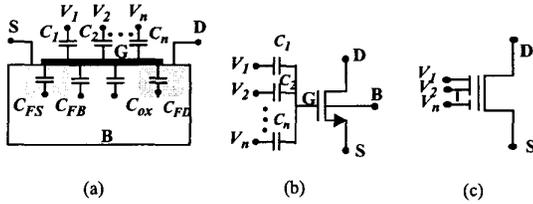


Fig.1: Floating Gate MOS: (a) Capacitors model. (b) Equivalent circuit. (c) Schematic.

### B: Log-domain integration with FGMOS

Any linear filter can be described for a set of first-order differential equations of the type,

$$\dot{x} = \alpha x + \eta x_i \quad (2)$$

where  $x$  represents the differential state variable, and  $x_i$  the input. The parameters  $\alpha$  and  $\eta$  are related with the filter specifications. Looking to the general formulations of logarithmic filters [4], both, the state variable,  $x$ , and the input  $x_i$ , are mapped into two new ones,  $y$  and  $u$ . The updating relationship is exponential,

$$x = ke^y, \quad x_i = k_i e^u \quad (3)$$

handling the linear expression into a nonlinear equation for  $y$  and  $u$ ,

$$\dot{y} = \alpha + Ke^{(u-y)} \quad (4)$$

with  $K = \eta k_i / k$ . Mapping Eq.(4) to physical magnitudes, the left hand side,  $\dot{y}$ , has been chosen as a *current* flowing through a linear capacitor, so  $y$  is proportional to the *voltage* difference between the terminals of the same capacitor. On the other hand, the new variables  $y$  and  $u$  can be considered as input voltages in devices whose behaviour is determined

by an exponential or logarithmic law. A FGMOS transistor working in the weak inversion saturation region maps this performance. Both situations are represented in Fig. 2.

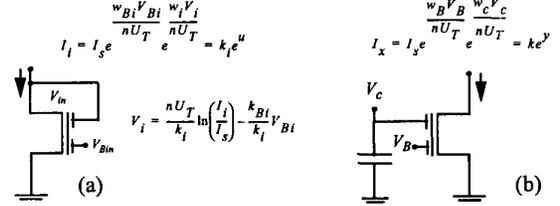


Fig.2: Circuits for log-mapping of space variables: (a)  $x_i$ . (b)  $x$ .

Returning to Eq.(4), the right hand side is the sum of two terms. The first one is a constant current whereas the second could be expressed as a function of the currents previously defined in Fig. 2. This is,

$$e^{(u-y)} = \frac{I_i}{I_x} \cdot e^{\frac{(w_B V_B - w_B V_B)}{n U_T}} \quad (5)$$

whenever the input and output transistors are equally sized. To implement Eq.(5), a circuit which output is a current proportional to the ratio between  $I_i$  and  $I_x$  is required. This is done by applying the TL principle with FGMOS described in [8]. The referenced circuit is drawn in Fig. 3. It is working as a sink current for the integrating capacitor. Adding the current,  $I_B$ , the integrator is comprised. Notice that  $M_x$  transistor works as the expander, delivering the linear output signal when required.

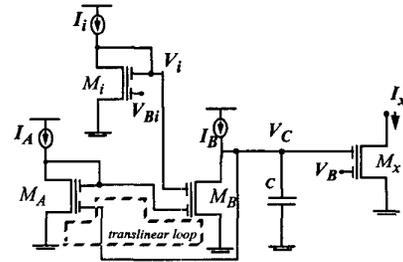


Fig.3: FGMOS log-domain integrator.

The integrator's equation (2) can be rewritten identifying the terms with the real magnitudes.

$$\dot{V}_c = \frac{I_B}{C} - \frac{I_A}{C} e^{\frac{w_c V_c - w_i V_i}{n U_T}} = \frac{I_B}{C} - \frac{I_A}{C} e^{\frac{w_B (V_B - V_{Bi})}{n U_T}} \cdot \frac{I_i}{I_x} \quad (6)$$

Eq. (6) is equivalent to a linear equation from the external

variables point of view,

$$i_x = \frac{nU_T}{w} \cdot \frac{I_B}{C} \cdot I_x - \frac{nU_T}{w} \cdot \frac{I_A}{C} e^{\frac{w_B V_B - V_{B1}}{nU_T}} \cdot I_i \quad (7)$$

where weight  $w$  is related with input  $V_c$  at  $M_x$  transistor. The equations have been formulated under the assumption all the weights  $w_i$  have the same value. A differential version for this equation, that will be used later on, is represented in the circuit of Fig.4 (a).

#### C: The second order filter

The implemented second order prototype is ruled by the following state-space equations:

$$C(I_{1p} - I_{1n}) = -\omega_{o1}(I_{1p} - I_{1n}) - \omega_{o2}(I_{2p} - I_{2n}) + \omega_{o3}(I_{ip} - I_{in}) \quad (8)$$

$$C(I_{2p} - I_{2n}) = \omega_{o4}(I_{1p} - I_{1n}) \quad (9)$$

where  $\omega_{oi}$  ( $i=1,2,3,4$ ) are the filter parameters associated to the external linear equations. These differential expressions can be easily got by substrating two single ones with the form given in eq.(2). Applying the same transformations explained in section B to both of them, gives,

$$\frac{wC}{nU_T} (\dot{V}_{1p} - \dot{V}_{1n}) = -\omega_{o1} - \omega_{o2}(I_{2p}I_{1p}^{-1} - I_{2n}I_{1n}^{-1}) + \omega_{o3}(I_{ip}I_{1p}^{-1} - I_{in}I_{1n}^{-1}) \quad (10)$$

$$\frac{wC}{nU_T} (\dot{V}_{2p} - \dot{V}_{2n}) = \omega_{o4}(I_{1p}I_{2p}^{-1} - I_{1n}I_{2n}^{-1}) \quad (11)$$

In the practical realization, the *FGMOS* transistors have four inputs: two for signal processing, as it is shown in Fig. 3, one for common-mode control, and one for weak inversion saturation region transistor biasing and/or filter tuning. The coefficients in our filter will be given by:

$$\omega_{oi} = \frac{w}{nU_T} I_A e^{\frac{wV_{tun1}}{nU_T}} e^{\frac{-2wV_{cm}}{nU_T}} e^{\frac{wV_{cmj}}{nU_T}} \quad \begin{matrix} j = [1, 2] \\ i = [1, 4] \end{matrix} \quad (12)$$

where the terms  $V_{cmj(b)}$  come from a third input to the floating gate MOS transistor connected to the output of the common mode feedback circuit,  $V_{cm}$  is a constant and  $V_{tun1}$  are the tuning voltages, which go to a fourth input, not shown in Fig. 4.

#### D: The Common Mode Control

In view of the fully differential structure, a feedback (or

feedforward) mechanism to control the common mode levels is needed. Also, the voltage common mode circuit will benefit the correct biasing for transistors working in the weak inversion region, and move the losses of the integrators derived from the output resistances in parallel with the integrating capacitances to very low frequencies. The block is proposed in Fig.4 (b). It is a differential amplifier with a *FGMOS* input pair, one of the transistors senses the common mode signal, and the other one fixes the reference voltage. Each output,  $V_{cmj}/V_{cmjb}$  ( $j$  makes reference to the couple of nodes being sensed) is connected to one input of every transistor supplying current to the integrating capacitor.

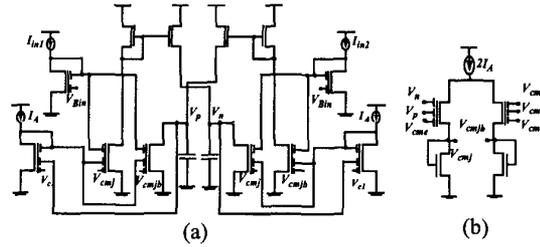


Fig.4: (a) Fully differential realization of eq.(6). (b) Common Mode Feedback Circuit.

#### E: The expander and the input stage

Once the integration is performed, the original state variables have to be restored. The block accomplishing this task appears in Fig.5 (a). It can be noted that the extra inputs are connected to a constant voltage which can also be used to adjust the signal levels. Also, although the block is operating in the current mode, it would be interesting to have a linear current/voltage conversion for testing purposes. The *FGMOS* input stage in Fig. 5 (b) will be used with this aim. Despite the transistors are working in the weak inversion region, the compression executed at the input transistors scales the input signals by the capacitances relationship enabling to manage larger input signals.

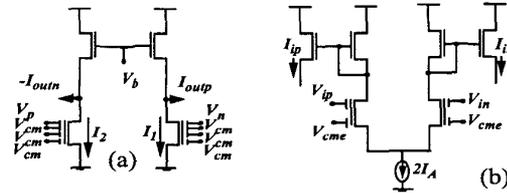


Fig.5: (a) The expander. (b) The input stage.

### 3. Results

According to what has been displayed in this paper, a second order filter has been designed. The filters parameters are given by,

$$\begin{aligned} \omega_o &= \sqrt{\omega_{o2}\omega_{o4}}, Q = \sqrt{\omega_{o2}\omega_{o4}}/\omega_{o1} \\ H_{LP}(0) &= \omega_{o3}/\omega_{o2}, H_{BP}(\omega_o) = \omega_{o3}/\omega_{o1} \end{aligned} \quad (13)$$

The prototype which has been fabricated in a  $0.35\mu\text{m}$  CMOS technology works at less than  $1V$  of voltage supply with a power consumption of  $2\mu\text{W}$ . Figure 6 shows the layout, while Fig. 7 illustrates the programming range for the quality factor, cutoff frequency and gain in the bandpass transfer function. The THD is shorter than 1% for  $200\text{mV}$  peak-to-peak input signal. The filter performance is summarized in Table 1. The power per pole and cut-off frequency for this example is below  $7\text{pJ}$ . The completed test results will be shown at the conference.

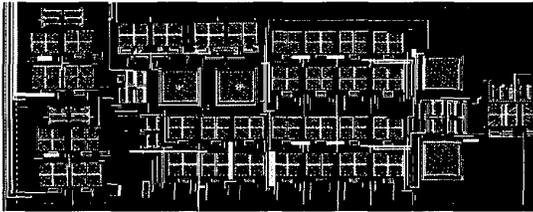


Fig.6: Layout of the second order prototype.

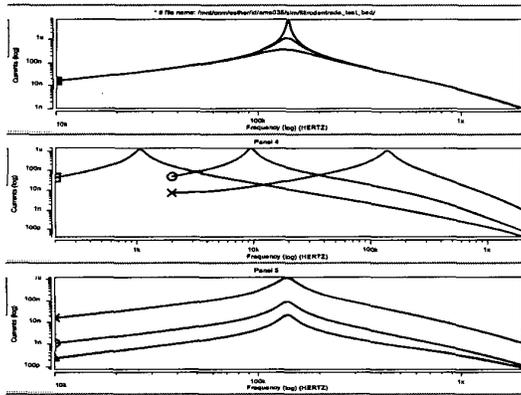


Fig.7: Programming the bandpass filter.

Table 1: Summary of the 2<sup>o</sup>-order filter parameters.

Technology param.	$V_{THn}=0.5V, V_{THp}=-0.6V$
Voltage Supply	1V
Power	$2\mu\text{W}$
Input Capacitances	58fF
THD@ ( $f_{in} = 200\text{mV}_{pp} f_o = 140\text{kHz}$ )	0.9%
DR (THD<1%)	>55dB
Programming Range ( $I_A=30\text{nA}$ )	>40dB, [1kHz,150kHz]
Area	$0.046\text{mm}^2$

### 4. Conclusions

A new low voltage / low power logarithmic integrator circuit based on *FGMOS* techniques has been presented. The circuit proposed exploits the translinear principle applied to floating gate *MOS* transistors, enabling both power supply voltage and power consumption reduction. The results obtained for a second order filter evidence that the filter works with less than  $1V$  power supply voltage, spending less than a  $1\mu\text{W}$  per pole. Again the use of *FGMOS* transistors appears as a promising technique for low power and low voltage applications.

### 5. References

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