A Low-Voltage Compatible Two-Stage Amplifier with ≥120dB Gain in Standard Digital CMOS

Chengming He, Degang Chen and Randall Geiger

Iowa State University
Ames, Iowa 50011, USA

ABSTRACT

A low-voltage compatible 120dB gain two-stage amplifier in standard digital CMOS with≤ 3 transistors between V_{DD} and V_{SS} is presented and circuit details are discussed. With the use of precision voltage attenuator, output level monitoring circuits (OLMC) and a digital tuning network, the first stage was tested, achieving ≥76dB DC gains over 2Vpp output swing. With a modest-gain 2nd stage, ≥120dB (by simulation, or 110 dB based on test) gain can be achieved over 2Vpp swing with PM ≥ 56° at GBW≥120 MHz when VDD=3.5V without OLMC.

1. INTRODUCTION

For the past three decades, semiconductor industry has advanced as Moore's Law predicted. The advances in CMOS process technologies have pushed the feature sizes below 90nm [1]. Meanwhile, the supply voltages have also been decreased significantly with the feature sizes to ensure safe operation. However the threshold voltages for digital transistors have not decreased as quickly as supply voltages in order to avoid large leakage. Such changes impose significant challenges to analog circuit design, especially to high gain large output swing amplifier design [1] [2]. Cascoding or cascading several stages of low gain amplifiers is two traditional solutions for high gain amplifier design. Due to more than 4 transistors stacking from VDD to VSS, cascading is not suitable for low-voltage applications. Though cascading is low-voltage compatible, its frequency response is often degraded too much by complex compensation. Positive-feedback technique has been shown to be an alternative effective way to achieve high DC gain with good frequency response as well as the potential of low-voltage supply applications [3]. However, few chips reach high DC gain due to the difficulty of matching as well as the temperature and process variations. Furthermore, such positive-feedback amplifiers show strong non-linearity and gain decreases sharply as the output swing becomes large. Efforts have been made to decrease the gain dependence on output swing [3] but few achieved a practical solution.

In this paper, we describe a two-stage high DC gain (≥110dB based on measurement or ≥120dB based on simulation) fully differential amplifier with simple Resistor-Capacitor compensation structure in standard digital CMOS process. The amplifier has a new architecture that is well suited for low-supply-voltage applications since it stacks a maximum of only 3 transistors between VDD and VSS. It cascades a high gain first stage with a modest gain second stage and the first stage utilizes a new positive feedback technique to boost the DC gain. A geometric-ratio dependent precision voltage attenuator is used to decrease the gain sensitivity to output swing. Furthermore, a high DC gain over the full output swing range is achieved with the help of a digital tuning network with an output-level monitoring circuit (OLMC). Simulation results show that excellent phase margin, high gain-bandwidth product GBW are both achieved for the first stage while high DC gain and PM ≥ 56° are maintained for the two-stage amplifier. Test results confirmed our design and simulation results.

In Section 2, we will discuss the new positive-feedback amplifier architecture and circuit details. In Section 3, simulation results are discussed and test results are presented. Finally we conclude our work in Section 4.

2. Amplifier Structure and Circuit Detail

2.1 Positive feedback amplifier

Fig. 1 shows the basic architecture of the proposed PFB amplifier (PFA) cascaded by a second stage. Since the gain of two-stage amplifier is the product of the first and the second stage, the following discussion will focus on the first stage of positive feedback amplifier. Using small-signal equivalent model for the first stage, we can get

$$\frac{v_o}{v_i} = -\frac{g_{m1}}{sC_L + g_{o1} + g_{o2} - k * g_{m2}} \quad (1)$$

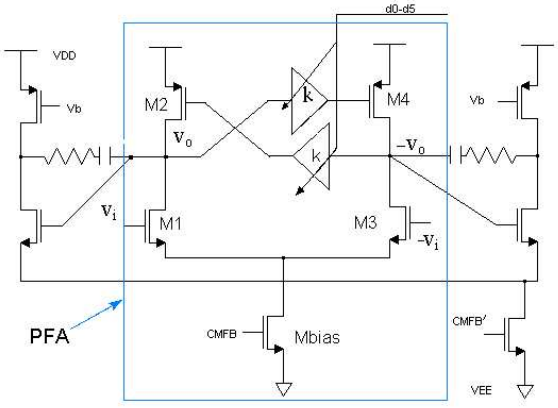

Fig. 1 A High Gain Two-Stage Amplifier Using Positive Feedback Technique

It is clear that when $g_{o1} + g_{o2} - k * g_{m2} \to 0$, a very high DC gain at the operating point can be achieved. Hence the design

goal is to use $k * g_{m2}$ to cancel $g_{o1} + g_{o2}$. Since g_{m2} is typically much larger than $g_{o1} + g_{o2}$, the proposed amplifier uses a precise voltage attenuator (k-network) between -Vo and M2, with the attenuator gain k much less than one. With the attenuator, the sensitivity of $k * g_{m2}$ with respect to the output swing is significantly reduced.

2.2 Precise Voltage attenuator

The attenuator consists of three cascading voltage dividers as shown in Fig. 2. The detail of a voltage divider is shown in the block labeled a) in Fig. 2. Since geometric ratio θ is used to determine the voltage division ratio, the attenuator gain k can be made very precise.

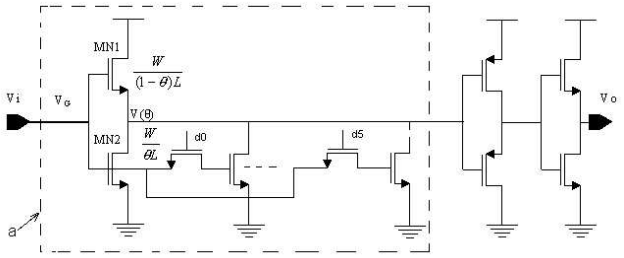

Fig. 2 A Geometric-ratio Dependent Precise Voltage Attenuator

Let $V_{EB} = V_G - V_S - V_{TH}$. When the transistor operating in saturation region, it can be shown that

$$V(\theta) = V_{EB}(1 - \sqrt{1-\theta}) \qquad (2)$$

Thus a precise voltage divider whose attenuation factor is dependent only on geometric ratio is obtained. Since we cannot change the minimal channel length in a specific process, it is much easier to adjust the width ratio between two MOS transistors.

One can arbitrarily achieve any attenuation factor value by adjusting θ. However, in practice, it is unrealistic to make a huge transistor as well as a tiny transistor. Cascading such dividers can obtain the desired attenuation value. The cascaded divider works well with alternating N-P type cascading, which provides the required level shifting for appropriate DC biasing.

Due to process and temperature variations, a fixed attenuation factor cannot effectively cancel the output conductance. A tunable k-network is proposed to compensate the process and temperature variations (shown in Fig. 2a). By switching on/off d0-d5, the equivalent W/L of MN2 is tuned finely. Thus the attenuation factor value of the first N-type divider can be adjusted with small steps. Studies show k decreases when more MOS are in parallel with MN2. In order to accommodate for the worst case temperature and process variation, the initial value of k (<<1) with control-code (d0-d5) to be all 0 should be sufficiently large while the final k with d0-d5 = all 1 should be small enough to guarantee the pole moving from RHP to LHP. In our design, the attenuation factor k decreases with increasing d0-d5 and a suitable k value can be achieved to guarantee very small output conductance.

2.3 Output Level Monitoring Circuitry

The amplifier DC gain decreases dramatically when the output swing becomes large with a fixed control code. However, our studies showed that the gain peaks at different output swing levels with different tuning codes. Thus a high DC gain amplifier over the full output swing is possible if we can select the appropriate tuning code corresponding to the output level. Fig. 3 shows a modified single-stage positive feedback amplifier structure. In order to adjust attenuation factor correctly, an OLMC is inserted between output nodes and control logic block. Theoretically we can maintain very high gain over full output swing range with enough monitoring resolution. Furthermore, given a desired gain requirement (e.g., >76dB over 2Vpp), the OLMC can be implemented with a low resolution ADC (3-bit). Thus with little hardware cost, sufficient large DC gain can be maintained over full output swing. This feature is very good for switch capacitor amplifier applications. The reason is as following: Output level will be determined by the input at sample phase and the OLMC can be moved to monitor input signals so that the k-network is settled when the amplification phase begins. Furthermore, our tuning scheme does not affect the GBW of the amplifier too much since the parasitic capacitance due the k-network is negligible comparing to the load.

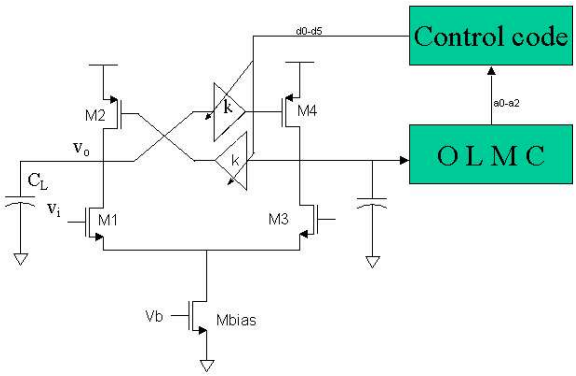

Fig. 3 A Single Stage High gain Positive Feedback Amplifier

2.4 Testing and Tuning Setup

Fig. 4 shows the testing and tuning setup for the first stage positive feedback amplifier. In order to eliminate loading effects of the resistive feedback network on the first stage PFA, a second stage with RC compensation was included. To enable laboratory testing, the second stage was configured as a buffer with gain<1. However, it can also be reconfigured by a gain stage as shown in Fig. 1 to achieve a high DC gain with large output swing as well as better linearity. As mentioned in section 2.3, gain peaks at different output level with different control codes. We can record appropriate control codes with respect to those output swing levels. These codes will be stored in the memory while the

address is the ADC output (Fig. 3). After High DC gain for the first stage PFA is achieved by adjusting the control code d0-d5, the buffer stage will be either switched off if the PFA is used as a single stage high gain amplifier with OLMC and digital control logic or be replaced by the modest gain amplifier with the aid of MOS switches while on-chip RC compensation network being reused by this high gain two-stage amplifier.

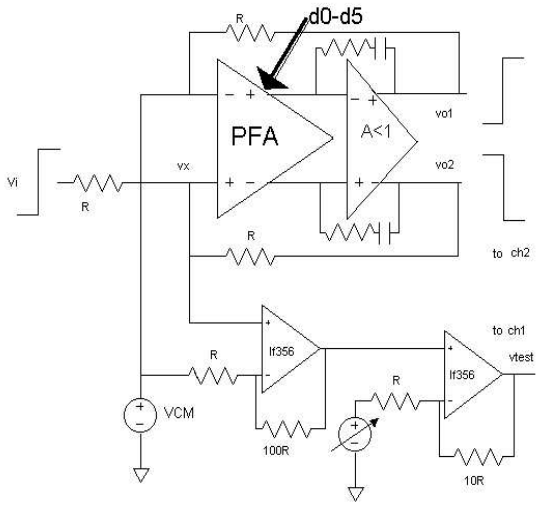

Fig. 4 Testing and Tuning Setup for PFA

3. Simulation and Test Results

The proposed PFA was designed and fabricated in an AMI 0.5 um process with exclusively standard digital CMOS transistors. Fig. 5 shows the die photo of this amplifier. The layout of the amplifier was carefully planned. All transistors were divided to either to 4, 8 or 16 small transistors and they were placed in a common centroid and 90° rotation symmetric way to achieve good matching. Compensation resistors and capacitors were integrated on chip to ease the amplifier's driving capability. The first stage positive feedback amplifier has core area of 0.1mm×0.09mm without compensation. The total area for the testing system was about 0.3mm×0.25mm, which included a buffer stage, compensation components, resistive feedback-network, common-mode feedback circuits and a 6-bit latch.

Simulation studies for all 5 process-corners (NN, FF, SS, FS, SF) and 3 different temperatures (0º, 27º, 80ºC) under 3.5V supply were conducted. In most situations, DC gains of ≥ 80 dB were achieved with appropriately selected control codes for the k-network. For the typical corner, in particular, DC gain of 110 dB was achieved with an optimal 6-bit control code at room temperature (see Fig. 6). With this fixed control code, the DC gain dropped quickly as the output swing level is increased (Fig. 6). However, when the OLMC was turned on to monitor the output swing level and adjust the control code accordingly, more than 85dB DC gain was maintained over a wide output swing range of 2Vpp (Fig. 6). This clearly demonstrated the efficacy of the tuning network.

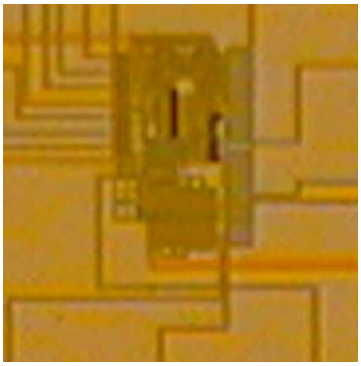

Fig. 5 Die Photo

Measurements verified simulation quite well except the specific large DC gain value since it was difficult to measure >90dB gain. Both gain non-linearity and gain variation with control-code were observed and ≥76dB gain was maintained over 2Vpp with tunable control-code (Fig. 6).

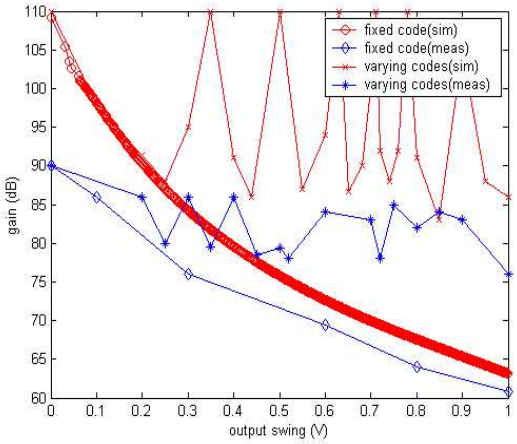

Fig. 6 Gain versus output swing (simulation and measurement)

Tab. 1 Simulated DC gain over wide temperature range

Gain (dB)	SS	SF	FS	FF	NN
0°C	84	85	72	92	103
27°C	82.2	89	84	85	110
80°C	70.4	84.5	83.7	89	88

Note: SS, SF, FS, FF, NN are CMOS process corners

Tab. 2 Measured DC gain of fabricated chips

Chip	#1	#2	#3	#4	#5
Gain (dB)	90	87.6	89.3	84.5	86.5

Tab. 1 showed simulated DC gains for different process corners over a wide temperature range. Tab. 2 summarized the DC gain of all fabricated 5 chips 100% chips worked functionally and ≥80dB DC gain were achieved. This clearly demonstrates our design. Furthermore, simulation results from an AC analysis showed GBW over 140MHz and nearly 90º phase-margin with 1pF load for the first stage (Fig. 7). The total power consumption of the amplifier was about 3.5mW with common-mode feedback.

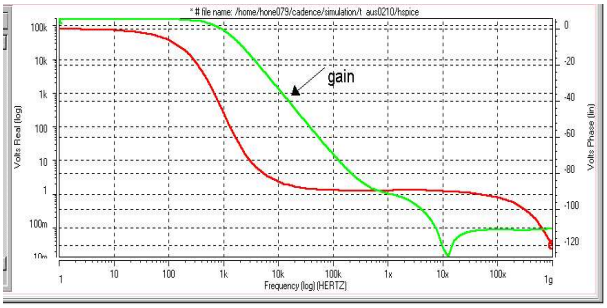

Fig. 7 Frequency Response of First Stage PFA

By reconfiguring the second stage with modest gain, ≥120dB DC gain was achieved in simulation without OLMC while maintain PM≥56° and GBW≥120 MHz over 2Vpp output swing (Fig. 8). Based on the first stage testing results, it can be predicted that the reconfigure two-stage amplifier can achieve 105dB gain over 2Vpp with 3.5V power supply.

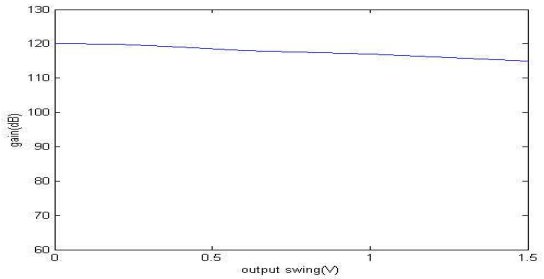

Fig. 8 Gain Versus Output Swing in Two-Stage Amplifier

Although the above simulation and measurement results were obtained with 3.5 V power supply, the same high gain PFA has also been designed, simulated, and verified in a TSMC 0.18um process with 1.8V supply. The AMI 0.5 um process results were reported here because that process is available to us free of charge through MOSIS. In fact, it is important to point out that from the circuit schematic one will find a maximum of only 3 transistors stacked from VDD to VSS in the entire design. Therefore, the proposed amplifier architecture is inherently low-voltage compatible. Furthermore, All transistors used in this PFA are exclusively digital CMOS transistors, a mixed-signal integration in digital CMOS process is demonstrated to enhance the yield and decrease the cost.

4. Conclusion

A high gain fully differential two-stage amplifier using positive-feedback technique in standard digital CMOS processes has been demonstrated to offer comparable or better performance as conventional high gain amplifiers while maintaining low voltage supply compatibility. It can be used in high speed high resolution data converters, high speed comparators, as well as functioning as a basic analog building block in large systems. It will save fabrication cost greatly for mixed-signal systems in low-voltage applications.

5. REFERENCES

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