A 0.35μm CMOS 17-bit@40kS/s SENSOR A/D INTERFACE BASED ON A PROGRAMMABLE-GAIN CASCADE 2-1 ΣΔ MODULATOR

José Manuel García-González, Sara Escalera, José M. de la Rosa, Oscar Guerra, Fernando Medeiro,
Rocío del Río, Belén Pérez-Verdú and Angel Rodríguez-Vázquez

Instituto de Microelectrónica de Sevilla, IMSE (CNM-CSIC)
Edif. CNM-CICA, Avda. Reina Mercedes s/n, 41012 Sevilla, SPAIN
Phone: +34 95056666, FAX: +34 95056686, E-mail: jrosa@imse.cnm.es

ABSTRACT

This paper describes the design and electrical implementation of an A/D interface for sensor applications realized in a 0.35μm standard CMOS technology. The circuit is composed of a low-noise instrumentation preamplifier and a SC cascade (2-1) ΣΔ modulator. The preamplifier, based on hybrid Nested-Miller compensated four-stage opamps, has a fixed gain of 10 and it is capable of handling signals with 20kHz-bandwidth and amplitudes ranging from μVs to hundreds of mVs with a signal-to-(noise+distortion) ratio over 100dB. The modulator architecture has a programmable gain for a better fitting to the characteristics of different sensor outputs. The design of both circuits is based upon a top-down CAD methodology which combines simulation and statistical optimization at different levels of the interface hierarchy. Simulation results show 17-bit@40kS/s for all cases of the modulator gain.(*)

1. INTRODUCTION

Sensors play a critical role in modern electronic systems, covering a wide range of data capturing functions in multiple applications [1]. In recent years, the number of applications is increasingly growing with the combined use of sensors and integrated circuits using the so-called MicroElectroMechanical (MEM) technologies [2]. These technologies have made it possible a new generation of "smart" sensors that combine digital signal processing and communication with the environment on a single chip or within the same package. In most practical applications MEM sensors must operate under very adverse environmental conditions with extreme temperatures, mechanical shocks, electromagnetic interferences, etc [1][2]. Therefore, the measuring circuit driving the sensor, normally formed by a low-noise preamplifier and an Analog-to-Digital Converter (ADC) must be very accurate and robust in order to handle the typically weak sensor output signals (ranging from μVs to hundreds of mVs) in very hostile environmental conditions [3]-[6]. This is aggravated in most applications as a consequence of the offset due to the excitation voltage supplying most transducers. In practice, that offset voltage is subject to temperature and manufacturing process variations, thus causing a shift in the signal range provided by the sensor. Hence, the measuring circuit must accommodate the complete range of possible offsets and real signals.

In this scenario, the use of ADCs based on ΣΔ Modulators (ΣΔMs) is suitable for several reasons. On the one hand, the noise-shaping performed by ΣΔMs allows to achieve high resolution (typically 16-17bit) in the band of interest (10-20kHz), with less power consumption than full Nyquist ADCs [7][8]. On the other hand, the action of feedback renders ΣΔMs very linear. Besides, in some of these applications the principle of sensing devices fits in with the topology of the ΣΔM, thus allowing partial or total integration of the sensor in the converter structure [9][10]. Last but not least, the robustness of ΣΔMs with respect to circuit imperfections make them suitable to include programmable gain without significant performance degradation [6]. This feature allows to accommodate the complete range of possible offsets and information signals in a sensor interface.

This paper describes the design and implementation of an A/D interface formed by a low-noise fixed-gain preamplifier and a third-order cascade (2-1) ΣΔM with programmable gain in a 3.3-V 0.35μm CMOS technology. According to precise simulations which take into account transistor-level performance and technological parasitics, the complete system is capable of handling signals up to 20-kHz BandWidth (B_w) with 17-bit resolution for all cases of modulator gain (0.5, 1, 2 and 4), considering a temperature range of $[-40°C, 175°C]$. To achieve these features with the less power consumption, an optimization-based methodology has been used at different hierarchical levels of the circuit [8].

2. ARCHITECTURE OF THE A/D INTERFACE

Fig.1 shows the conceptual block diagram of a smart sensor chip. The transducer is supplied via an excitation voltage, v_{exc}, and gives a differential voltage, v_{in}, which is function of the parameter to be measured, e.g. pressure, temperature, etc. As v_{in} has a weak amplitude, a very low-noise preamplifier is normally the first block in a sensor front-end [4][5]. In some multi-purpose applications, this preamplifier has a switchable gain to accommodate different signal levels [4]. Once the sensor signal has been boosted to workable levels, an A/D converter (normally based on ΣΔMs) digitizes it and the rest of processing is carried out in the digital domain. In this work, the front-end gain is distributed between a fixed-gain (x10) in the preamplifier and a selectable set of gains (x0.5, x1, x2, x4) in the ΣΔM, which simplifies the architecture and design of the preamplifier.

2.1 Low-noise instrumentation preamplifier

Fig.2 shows the schematic of the preamplifier. It consists of a resistor-feedback instrumentation configuration, which has been demonstrated as a suitable topology in low-noise sensor interfaces
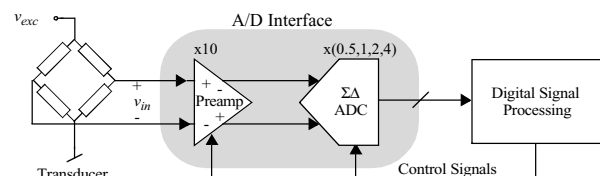

Figure 1. Conceptual block diagram of a "smart" sensor chip.

[11], together with a chopper stabilization technique for removing the flicker noise (switches in Fig.2) [12]. In addition to the close-loop gain (given by $1 + 2R_2/R_1$) and bandwidth ($1/(R_2C)$), the most critical figures of the preamplifier are the thermal noise, and the <u>T</u>otal <u>H</u>armonic-<u>D</u>istortion (THD). These features are specially limiting factors in our application since the <u>S</u>ignal-to-(<u>N</u>oise+<u>D</u>istortion) <u>R</u>atio ($SNDR$) must be over 100dB at the signal amplitude peak, $V_{in\text{-peak}}$, in all cases of the sensor interface gain: x5, x10, x20, x40 (see Fig.1). There are two worst cases which correspond to the gain limits:
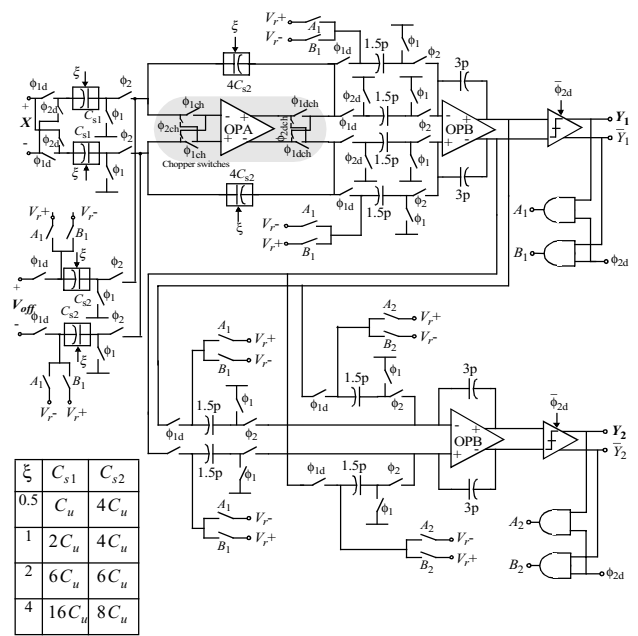
- The maximum gain, x40, which corresponds to the minimum value of $V_{in\text{-peak}} = 35\text{mV}$. For this amplitude, the limiting factor is thermal noise power spectral density which must be $\sqrt{S_{th}} < 1.8\text{nV}/\sqrt{\text{Hz}}$ in order to fulfill $SNR > 100\text{dB}$.
- The minimum gain, x5, which corresponds to the maximum value of $V_{in\text{-peak}} = 280\text{mV}$ in our application. In this case, the critical issue is the linearity which must be $THD < -100\text{dB}$ for a preamplifier output signal amplitude of 2.8V.

To cope with the above requirements, a high DC-gain (~ 100dB) opamp with very low input noise (~ $1\text{nV}/\sqrt{\text{Hz}}$) will be required. These figures can be achieved by using multistage opamp topologies as described in Section 3.

2.2 Modulator topology and high-level sizing

In order to find the best ΣΔM architecture that fulfills the required specifications (17-bit@40kS/s) with the less power consumption, a large number of modulator topologies has been compared in terms of the estimated power consumption and silicon area, considering the impact of main circuit error mechanisms and technology parasitics. The selection procedure – described in [13] – led us to the third-order 2-1 cascade SC ΣΔM shown in Fig.3, with an oversampling ratio of $M = 128$. Note that the first integrator contains two differential input branches: one of them is for the input signal, in which double sampling is used to achieve an extra signal gain of 2, without increasing circuit noise [12]. The second branch receives the DAC outputs. Making use of the spare connection of the second branch, an external DC signal (V_{off}) can be applied during ϕ_1 to center the sensor signal in the modulator full-scale range. This solution renders unnecessary a third branch for offset compensation with the subsequent thermal noise saving. The programmable gain ($\xi = 0.5, 1, 2$ and 4) has been mapped onto switchable capacitor arrays, each of them formed by a variable number of unitary capacitors. Such numbers (shown in Fig.3) are selected for minimum power dissipation, bearing in mind the circuit noise limitation and the high temperature required for this sensor interface ($175°\text{C}$). In order to keep the amplifier dynamic
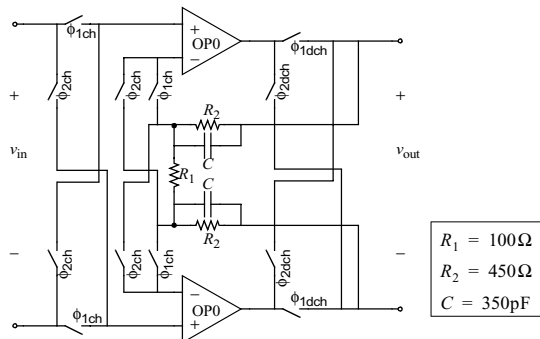
Figure 2. Preamplifier schematic with chopper switches.

Figure 3. SC schematic of the 2-1 cascade ΣΔM.

requirements as relaxed as possible for all cases of the modulator gain, we propose to switch the number of unitary capacitors forming all the capacitances involved – not only the ones forming the sampling capacitors [13].

The modulator in Fig.3 has been high-level sized, i.e, the modulator-level specifications have been mapped onto building-block specifications using statistical optimization for design parameter selection, and compiled equations (capturing non-ideal building block behaviour) for evaluation. This process is fine-tuned by behavioural simulation using ASIDES, an advanced behavioural simulator of SC ΣΔMs [8]. In this process, worst cases for speed (the largest capacitor values) and for thermal noise (the highest temperature and the lowest capacitor values) are contemplated. The results of this sizing process are summarized in Table 1, in which OPA denotes the opamp used at the first integrator in the chain and OPB refers to the opamps used at the second- and third-

Table 1: High-level sizing of the 2-1 ΣΔM with programmable gain

SPECS: 17bit@40kS/s@2V$_p$			Value	Unit
INTEGRATORS	Integration capacitor	Gain 0.5	24	pF
		Gain 1	24	pF
		Gain 2	36	pF
		Gain 4	48	pF
	Unitary capacitor		1.5	pF
	Sigma		0.1	%
	Capacitor non-linearity		25	ppm/V^2
	Bottom parasitic capacitor		5	%
	Switch ON-resistance		<650	Ω
OPAMPS	DC-gain	OPA	68	dB
		OPB	63	dB
	DC-gain non-linearity		15%	V^{-2}
	GBW	OPA (44.2pF load)	17	MHz
		OPB (8.9pF load)	15	MHz
	Slew-rate	OPA (44.2pF load)	17	V/µs
		OPB (8.9pF load)	28	V/µs
	Output swing		±2.5	V
COMPS.	(Hysteresis + Offset) (max.)		30	mV

integrators in the modulator chain (see Fig.3). The data in Table 1 define the specifications of the building blocks, which are the starting point for electrical sizing.

## 3. DESIGN OF THE BUILDING BLOCKS

The sensor-interface building blocks, namely, amplifiers, comparators and switches have been conveniently selected and sized according to the requirements given in Section 2. Design considerations on each of these blocks as well as their electrical performance using HSPICE are detailed in this section.

3.1 Amplifiers

Three different amplifiers are used in the sensor interface: the opamp in the preamplifier (OP0 in Fig.2) and the two opamps used in the $\Sigma\Delta M$ (OPA and OPB in Fig.3). Since the requirements for each of them are different, it is recommendable to obtain three different designs in order to avoid oversizing and optimize the power consumption. For this purpose, the transistor-level sizing tool FRIDGE was used to explore the potential of several opamps topologies [8]. The outcome of this exploration is the following:

- For both amplifiers in the $\Sigma\Delta M$, a fully-differential single-stage folded-cascode topology, shown in Fig.4(a), was selected but using different sizing and biasing for OPA and OPB. Note that an N-type input pair has been considered because a twin-well technology is used, and hence, the body effect can be removed in NMOS transistors. The Common-Mode Feed-Back (CMFB) net has been implemented using a SC circuit, which provides fast and linear operation with small power dissipation.

- For the opamps in the preamplifier (OP0), a four-stage topology with hybrid Nested-Miller compensation technique [14], shown in Fig.4(b), was chosen to fulfill the required high-linearity and low-noise figures. In order to optimize the power consumption, a switchable transistor-unit array is used at the output stage, which allows us to adjust the output current (i_{out}) to fulfill the required specifications with the minimum power consumption for each case of the interface gain.

The electrical performance of all the amplifiers is summarized in
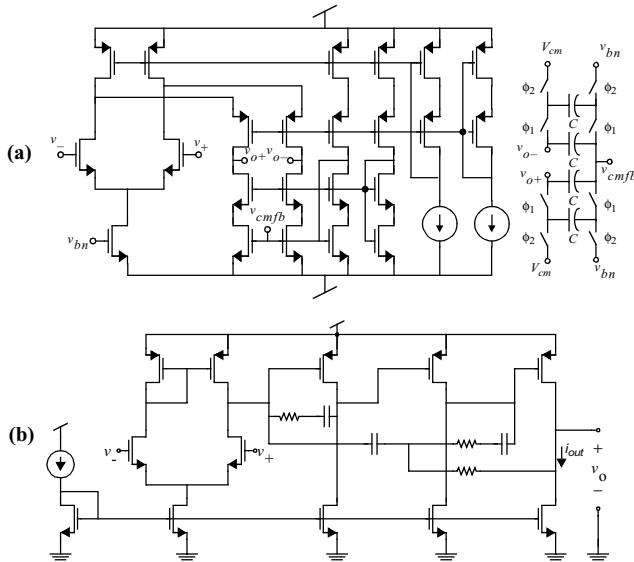
Figure 4. Amplifiers. (a) Folded-cascode amplifier with SC CMFB net. (b) Four-stage amplifier with hybrid Nested-Miller compensation.

Table 2 in terms of target values imposed during the optimization procedure in FRIDGE to the main parameters affecting the specifications of the whole interface.

3.2 Comparators

In order to fulfill the requirements for the comparator given in Table 1, a regenerative latch including a preamplifying stage was selected – shown in Fig.5. The role played by the differential pair is to improve the resolution of the comparator, which can be severely degraded in practice due to dissymmetries between the latch parameters. MonteCarlo simulations and corner analysis have been done for characterizing the comparator performance during its full sizing. Table 3 summarizes the comparator features, showing the worst-case parameters and the power dissipation.

3.3 Switches

In the SC integrators used in the $\Sigma\Delta M$, the value of the finite switch-on resistance, R_{on}, is mainly constricted by dynamic considerations. Incomplete settling originated by transmission gates is traditionally reduced by making $R_{on} C f_S \ll 1$, with C and f_S being the sampling capacitor and the sampling frequency, respectively. In our design, it has been evaluated that $R_{on} < 650\Omega$ can be tolerated with no degradation of the modulator performance. However, in low-voltage technologies, given that the threshold voltage of the MOS transistors is not scaled down in the same amount as the supply voltage, the voltage range in which R_{on} keeps a nearly constant value decreases. The sampling process with such an on-resistance causes dynamic distortion – the more evident the larger the sampling capacitor. In sensor interfaces,
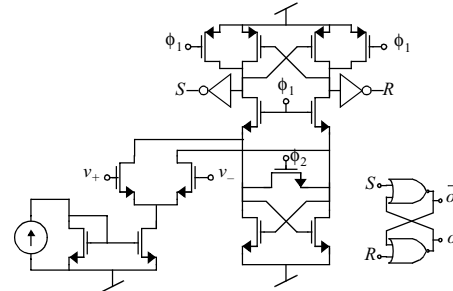
Figure 5. Comparator schematic.

Table 2: Electrical performance of the opamps (HSPICE)

Parameter	OP0 (24pF load)	OPA (45pF load)	OPB(9pF load)
DC-gain (dB)	98.6	73.7	67.6
$\sqrt{S_{th}}$ (nV/$\sqrt{\text{Hz}}$)	0.99	3.8	6.6
GB (MHz)	176.6	22.0	33.3
PM (º)	74.2	86.4	84.8
Slew-Rate (V/µs)	38.7	22.1	31.3
Output Swing (V)	2.74	±2.75	±2.75
Power Cons. (mW)	25	7.1	2.4

Table 3: Electrical performance of the comparators (HSPICE)

Parameter	Worst-case
Offset (mV)	9.92
Hysteresis (mV)	0.12
Resol. time, T_{RLH} (ns)	8.6
Resol. time, T_{RHL} (ns)	6.15
Power Cons. (mW)	0.43

high-linearity is a must. Therefore, the non-linear sampling effect in the first integrator has to be carefully taken into account, especially in the case of $\xi = 4$, in which $C = 24pF$. Thus, the switches used in the first integrator have been sized in order to obtain an $SNDR$ over $17bits$. This is achieved by increasing the aspect ratio of the CMOS switches in the front-end integrator to $29.1/0.35$ and $105.9/0.35$ for the NMOS and the PMOS transistors, respectively.

4. LAYOUT AND SIMULATION RESULTS

The sensor interface has been implemented in a single-poly, five-metal 0.35µm CMOS technology. Fig.6 shows the complete layout showing the main parts of the circuit. Capacitors were implemented using Metal-insulator-Metal (M-i-M) structures and common centroid topologies were used to reduce mismatch error. Table 4 summarizes the circuit performance showing the main results for the preamplifier and the ΣΔM. The preamplifier has been simulated using HSPICE, and the ΣΔM, because of the excessive CPU times required, was analyzed using ASIDES, considering the worst-case for thermal noise ($175°C$) and taking into account the electrical performance of building blocks described in Section 3. As an illustration of the modulator performance, Fig.7 shows the output spectra for all cases of the modulator gain, ξ, corresponding to an input tone of frequency $5kHz$ and an amplitude at the SNR-peak. In all cases, the dynamic range is over 105dB, corresponding to 17-bit resolution. If these results are confirmed by experimental measurements, the presented circuit will be within the state-of-the-art ΣΔMs. Moreover, to the best of the authors knowledge, among previously reported ΣΔMs achieving resolutions over 16-bit within signal bandwidths higher than 20-kHz, only the works in [15] and [16], would present a better performance in terms of power dissipation and resolution, respectively. However, the combined use of programmable-gain and preamplification in this paper allow us to increase the signal range as compared to [15][16], making it possible to handle 20-kHz signals with amplitudes up to 140dB below full-scale (2V in our case).
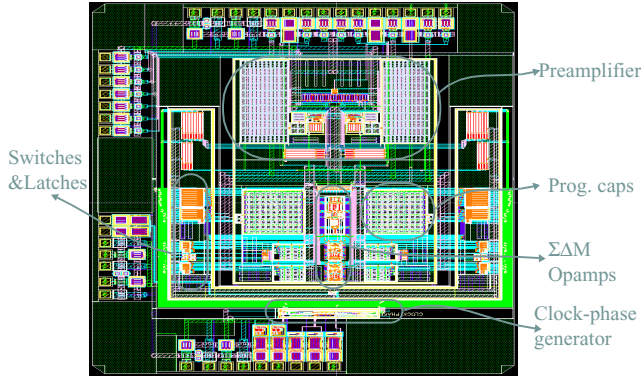

Figure 6. Complete layout of the sensor interface.

Table 4: Performance summary (Simulation)

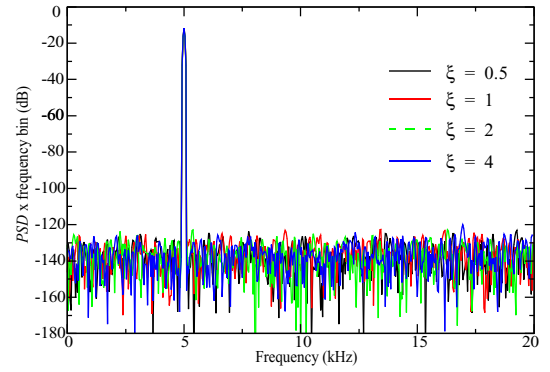| PREAMPLIFIER		ΣΔ MODULATOR	
Gain	19.99 dB	Resolution	17bits
f3dB	995 kHz	Signal Bandwidth	20kHz
SNR ($V_{\text{in-peak}}$=35mV)	99.3dB	Programmable Signal Gain	0.5, 1,2,4
THD ($V_{\text{in-peak}}$=200mV)	-100dB	Sampling Rate	5.12MHz
Power Cons. (switchable)	36-48mW	Power Cons.	14mW

Figure 7. Output spectra for all cases of the modulator gain.

CONCLUSIONS

The design of a 0.35µm CMOS programmable-gain sensor interface has been described. The architecture selection process and the design of their building blocks have been based upon a top-down CAD methodology that combines simulation and statistical optimization at different levels of the interface hierarchy. Simulations considering main circuit errors showed an effective resolution equal to 17 bits in a 20-kHz signal bandwidth for all gain cases.

REFERENCES

[1] G. Van der Horn and J.L. Huijsing, *Integrated Smart Sensors*, Kluwer Academic Publishers, 1998.
[2] D. S. Eddy and D.R. Sparks., "Application of MEMs Technology in Automotive Sensors and Actuators", *Proc. of the IEEE*, pp. 1747-1755, Aug. 1998.
[3] J.E. Johnston, "A 24-bit Delta-Sigma ADC with an Ultra-Low Noise Chopper-Stabilized Programmable Gain Instrumentation Amplifier", *Proc. of Advances A/D and D/A Conversion Techniques and their Applications*, pp. 27-28, 1999.
[4] P. Malcovati and F. Maloberti, "An Integrated Microsystem for 3-D Magnetic Field Measurements", *IEEE Trans. on Instrumentation and Measurement*, pp. 341-345, April 2000.
[5] C.B. Wang, "A 20-bit 25-kHz Delta-Sigma A/D Converter Utilizing a Frequency-Shaped Chopper Stabilization Scheme", *IEEE J. of Solid-State Circuits*, pp. 566-569, March 2001.
[6] F. Murabayashi et al., "A Programmable Sensor Signal Conditioning LSI", *Proc. of the Second IEEE Asia Pacific Conference on ASICs*, pp. 107-110, 2000.
[7] S.R. Norsworthy, R. Schreier and G. Temes, *Delta-Sigma Data Converters − Theory, Design and Simulation*, IEEE Press, 1997.
[8] F. Medeiro, B. Pérez-Verdú and A. Rodríguez-Vázquez, *Top-down Design of High-Performance Sigma-Delta Modulators,* Kluwer Academic Publishers, 1999.
[9] K.A.A. Makinwa and J.H. Huijsing, "A Smart CMOS Wind Sensor", *Proc. IEEE ISSCC, digest of Technical Papers*, pp. 432-479, 2002.
[10] H. Kulah, N. Yazdi, and K. Najafi, "A CMOS Switched-Capacitor Interface Circuit for an Integrated Accelerometer", *Proc. IEEE Midwest Symp. on Circuits and Systems*, pp. 244-247, August 2002.
[11] D.A. Kerth, D. S. Piasecki, "An Oversampling Converter for Strain Gauge Transducers", *IEEE J. of Solid-State Circuits*, pp. 1689-1696, December 1992.
[12] C. C. Enz and G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", *Proc. of the IEEE*, Vol. 84, pp. 1584-1614, Nov. 1996.
[13] F. Medeiro et al., "Design Considerations for an Automotive Sensor Interface ΣΔ Modulator", *Proc. of the 2003 International Symposium on Circuits and Systems*, pp. III.538-541.
[14] R. Mita, G. Palumbo and S. Pennisi, "Hybrid Nested Miller Compensation with Nulling Resistors", *Proc. of the 2002 Int. Conference on Electronics, Circuits and Systems*, pp.177-180.
[15] S. Rabii and B. A. Wooley: "A 1.8-V Digital-Audio Sigma-Delta Modulator in 0.8-µm CMOS", *IEEE J. of Solid-State Circuits*, pp. 783-796, June 1997.
[16] Y. Yang, A. Chokhawala, M. Alexander, J. Melanon and D. Hester: "A 114-dB 68-mW Chopper-Stabilized Stereo Multibit Audio ADC in 5.62mm^2", *IEEE J. of Solid-State Circuits*, pp. 2061-2068, Dec. 2003.