

# A 1V 4.2mW Fully Integrated 2.5Gb/s CMOS Limiting Amplifier using Folded Active Inductors

Chia-Hsin Wu, Jieh-Wei Liao, and Shen-Iuan Liu

Department of Electrical Engineering & Graduate Institute of Electronics Engineering  
National Taiwan University, Taipei, Taiwan 10617, R. O. C.  
Email: lsi@cc.ee.ntu.edu.tw

## Abstract

A 1V 4.2mW fully integrated 2.5Gb/s CMOS limiting amplifier is presented in this paper. Without any voltage boosting technique, this amplifier can work well as low as 1V supply voltage and is attributed to utilize folded active inductors. The folded active inductor not only consumes lower voltage headroom but also is area-efficient, compared to the conventional active and on-chip inductors, respectively. This work with the offset-canceling network has been implemented in a 0.25 $\mu$ m CMOS process and occupies only 0.12mm<sup>2</sup>. Measured performance shows 1.75GHz bandwidth with 39.9dB differential gain, and the power consumption is only about 4.2mW excluding the power consumption of the output buffer.

## 1. Introduction

Optical communication is rapidly bloomed from long-haul optic-fiber network into short-distance local area network (LAN). For LAN applications, low cost and adequate performance are the two of most considered indexes. Fig. 1 shows the optical receiver front-end block diagram. The function of the optical receiver is to detect the NRZ optical signal then to regenerate the transmitted data and clock. Transimpedance amplifier (TIA) converts small level signal current to moderate voltage level, then limiting amplifier (LA) is responsible to amplify the input signal to a sufficient voltage level for the reliable operation of the clock and data recovery (CDR) circuit. Currently, commercial 2.5Gb/s SONET/STM systems are composed of several discrete chips, which are implemented in different processes such as GaAs, Si Bipolar and CMOS processes. However, with significant advancement in CMOS technology, various CMOS Gigabit receiver circuits have been demonstrated in many papers [1-5].

For a CMOS limiting amplifier, the primary factor which constraints bandwidth is the inherent parasitic capacitance in CMOS process. Many bandwidth enhancement techniques have been developed to overcome the significant parasitic capacitance. Among these techniques, inductive shunt peaking technique is widely adopted due to its simplicity and effectiveness. Inductive shunt peaking can be implemented by on-chip spiral inductors or conventional active inductors. The on-chip inductor is not only difficult to keep its self-resonance frequency higher than operating frequency in larger inductance, but also occupies huge area. For a conventional active inductor, it requires larger voltage

drop. Therefore, higher supply voltage or voltage boosting technique is required while using conventional active inductors. In this paper, a 1V 2.5Gb/s CMOS limiting amplifier using folded active inductors is presented without any voltage boosting technique. Measured eye diagrams meet OC48/STM16 mask specifications in only 4.2mW power consumption excluding the power consumption of the buffer.

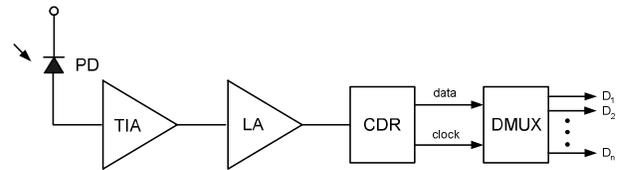


Fig. 1 Optical receiver front-end.

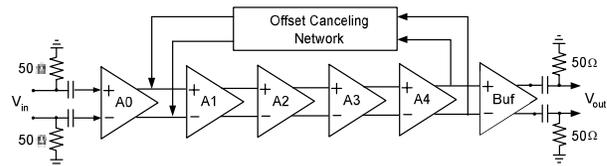


Fig. 2 Limiting amplifier architecture.

## 2. Limiting Amplifier Architecture

Fig. 2 shows the schematic of a typical LA. It consists of several gain stages to provide sufficient gain, and the offset cancelling network to minimize dc offset due to process variations. A typical gain stage is composed of an NMOS differential pair and PMOS loads. The LA which consists of the typical gain stages can operate up to 1.25Gb/s without any bandwidth enhancement technique [2]. However, to design a 2.5Gb/s LA, the performance of the typical gain stage is insufficient and the bandwidth enhancement, such as inductive shunt peaking, is required. In inductive shunt peaking techniques, on-chip inductors and active ones are widely adopted. Nevertheless, no matter to on-chip inductors or active ones, they introduce different drawbacks to deteriorate circuit performances. For an on-chip inductor, it introduces large parasitic capacitance to limit bandwidth improvement and occupies large chip area. For a conventional active inductor, it consumes larger power and acquires larger dc voltage drop.

In this work, the gain stages employing folded active inductors can perform inductive shunt peaking without large dc voltage drop. Using folded active inductors, this amplifier

can operate well at 2.5Gb/s  $2^{11}$ -1 PRBS data under 1V supply voltage, and the core circuit consumes only 4.2mW.

### 3. Circuit Design

#### A. Gain Stage with Folded Active Inductors

The bandwidth of each gain stage can be increased by using inductive loads. In order to acquire the optimum peaking, the inductance can be designed as [4]:

$$L_{opt} = 0.4 \cdot R^2 \cdot C \quad (1)$$

, and the bandwidth can be increased by 70% without introducing undesirable peaking in the bandwidth. The inductance is chosen around 20nH for 2.5Gb/s applications. The inductive peaking load can be implemented by on-chip inductors, conventional active inductors [3], and conventional active inductors with a voltage boosting technique [4], as shown in Fig. 3, respectively. Although the peaking with on-chip inductors consumes smallest voltage drop, it will occupy largest chip area and introduce significant parasitic capacitance. For peaking with conventional active inductors, it will require largest dc voltage drop and more power, but it consumes less chip area and has large inductance up to  $f_T/2$ . Further, the active inductor with voltage boosting is proposed in [4] as shown in Fig. 3(c). Nevertheless, a high voltage generation circuit is required and makes the chip design more complex.

In this design, each gain stage employs the folded active inductors rather than the implementations as shown in Fig. 3. The schematic of a folded active inductor is shown as Fig. 4(a). From its small signal model in Fig. 4(b), the impedance  $Z_{in}$  can be approximated by

$$Z_{in} = \frac{1}{g_m} \frac{1 + sC_{gs}R_f}{1 + s\frac{C_{gs}}{g_m}} \quad (2)$$

The impedance vs. frequency can be plotted in Fig. 5(a), and it can be modeled in Fig. 5(b) between pole and zero frequencies.

The schematic of each gain cell is depicted as Fig. 6. M1 and M2 perform as a differential pair, and M3 to M6 perform two folded active inductors to cancel the parasitic capacitances at nodes P and Q. M5 and M6 are biased in linear region to perform as resistors. In this design, large voltage drop can be across the gate and source of M3 and M4, and it does not deteriorate voltage headroom, compared to conventional active inductors. The bodies of the PMOS loads are connected to  $V_{pb}$  rather than GND to relieve body effect, thus the voltage drop of the PMOS loads can be decreased. Consequently, the gain cell can work well even at 1V supply voltage without any high voltage generation circuit.

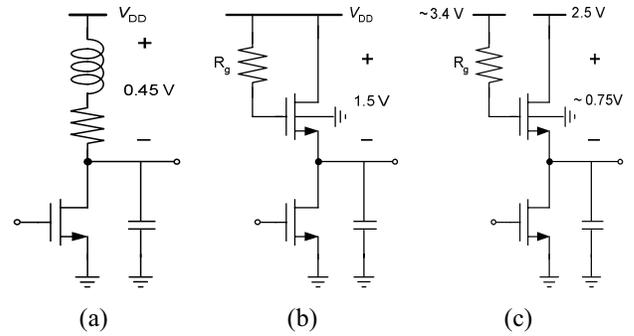


Fig. 3 The inductive loads: (a) on-chip inductor, (b) active inductor, (c) active inductor with voltage boosting [4].

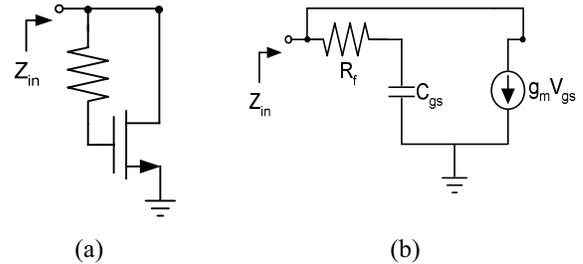


Fig. 4 Folded active inductor (a) schematic, (b) small signal model.

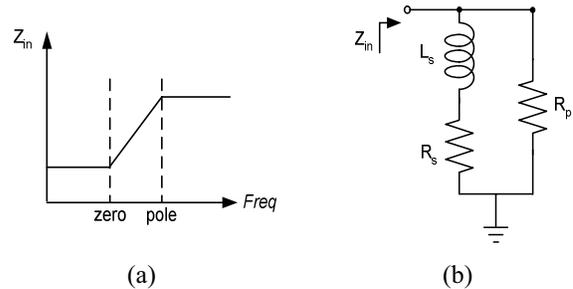


Fig. 5 Folded active inductor (a)  $Z_{in}$  vs. frequency, (b) small signal equivalent model.

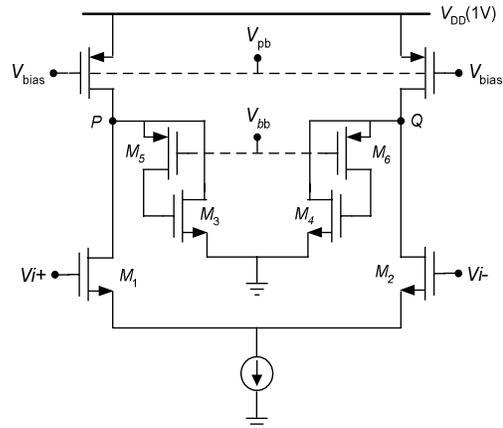


Fig. 6 The schematic of the gain cell.

### B. Offset Canceling Network

The offset canceling network is generally implemented as a low-pass RC filter to extract the dc offset. In order to meet low 3dB corner frequency, the resistance and capacitance are usually very large to occupy large chip area, thus the network is implemented with external components. In order to minimize external components and reduce chip area, the top-detection feedback circuit is adopted as the offset canceling network. The schematic of the top-detection feedback circuit is shown in Fig. 7. The area of the top-detection feedback is smaller than that of conventional RC circuit, and it is insensitive to process variation at the same time. The low 3dB corner frequency is designed around 20kHz.

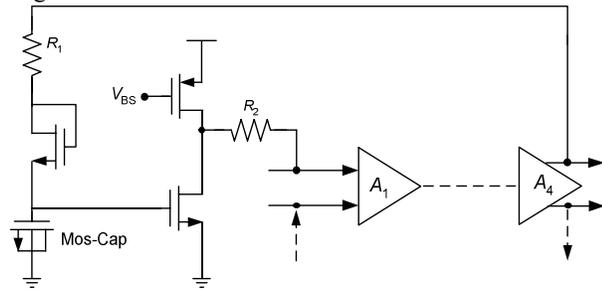


Fig. 7 Top-detection feedback circuit.

## 4. Experimental results

The fully integrated limiting amplifier with folded active inductors has been implemented in CMOS 0.25 $\mu$ m 1P5M CMOS process. The die photo is shown in Fig. 8. The area of the core circuit is 350 $\mu$ m x 330 $\mu$ m, which is almost equal to an on-chip spiral inductor. The measured S21 and return loss, such as S11 and S22, are shown in Fig. 9. The measured -3dB corner frequency is 1.75GHz, and measured S21 is 22dB. The lower S21 is attributed to the bad input matching while in testing. In order to evaluate the voltage gain correctly, the transient response is tested. Fig. 10 shows the measured transient response to calculate the differential gain. The input and output signals are 4mV<sub>pp</sub> and 200mV<sub>pp</sub> at 1.25GHz, respectively, and the equivalent differential voltage gain is 39.9dB (33.9dB + 6dB = 39.9dB).

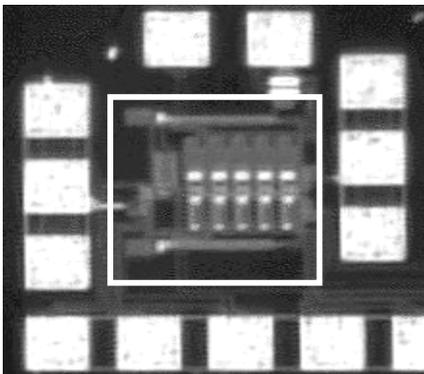


Fig. 8 Chip photo. Core circuit: 0.35mm x 0.33mm.

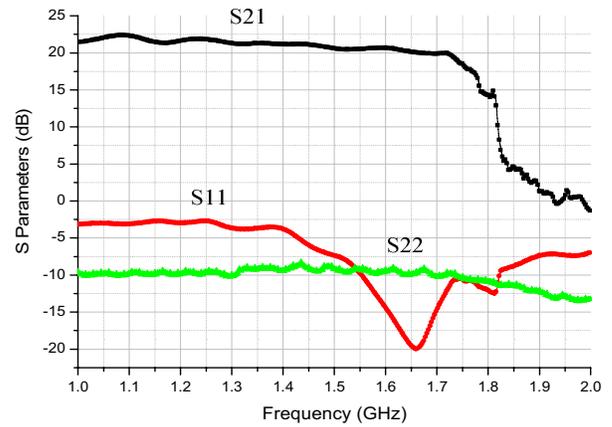


Fig. 9 Measured S parameters.

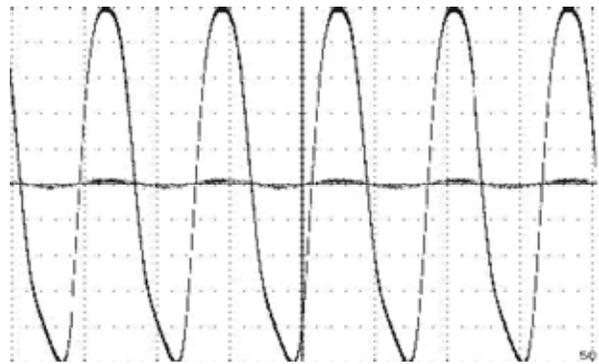


Fig. 10 Measured transient response. (input: signal: 4mV<sub>pp</sub>, output: 200mV<sub>pp</sub> @1.25GHz, Horizontal scale:500ps/div, Vertical scale: 20mV/div).

The measured transient response demonstrates the LA has sufficient gain and bandwidth to amplify 2.5Gb/s small signal input random data. Fig. 11 shows the measured eye diagram at 2.5Gb/s 2<sup>11</sup>-1 PRBS input with different input amplitudes. The measured eye diagrams can meet OC48/STM16 mask specifications.

In order to compare with the state-of-the-art published papers, the in-house figure-of-merit (FOM) can be defined as

$$\begin{aligned}
 FOM &= 20 \log \left( \frac{Gain \cdot Bandwidth (GHz)}{Power (mW)} \right) \\
 &= Gain (dB) + 20 \log \left( \frac{Bandwidth (GHz)}{Power (mW)} \right)
 \end{aligned} \quad (3)$$

, which considers the circuit performance and power consumption simultaneously. The FOM indicates the gain-bandwidth product per unit power consumption, and the higher FOM means the LA has higher circuit performance under unit power consumption. Table I summaries the circuit

performance and the comparison with the state-of-the-art published papers. It demonstrates this work employing folded active inductors has comparable performance.

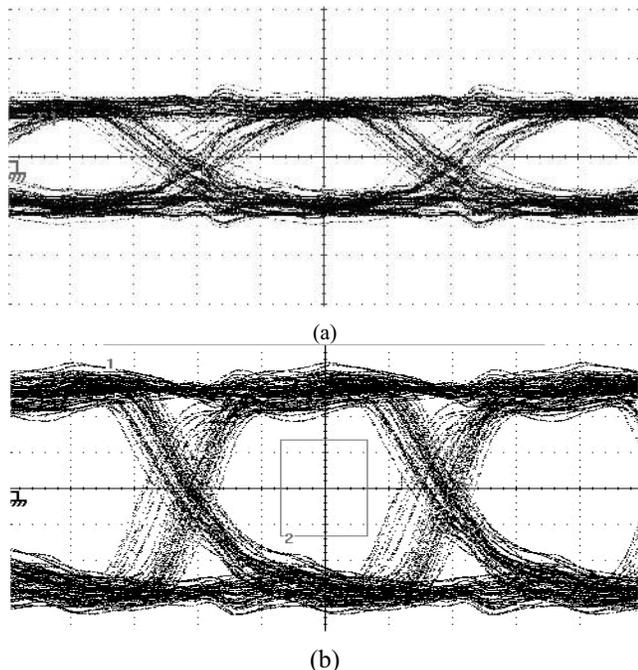


Fig. 11 The measured output eye diagram at (a)4mV<sub>pp</sub>, (b)30mV<sub>pp</sub>, 2.5Gb/s 2<sup>11</sup>-1 PRBS input data (Horizontal scale:500ps/div, Vertical scale:100mV/div).

## 5. Conclusion

In this paper, a 1V 4.2mW 2.5Gb/s fully integrated CMOS limiting amplifier is presented. Using the proposed folded active inductors, the CMOS LA can work well at only 1V supply voltage without any voltage boosting technique. By adopting the folded active inductor and top-detection feedback circuit, the power consumption and area can be reduced. In order to compare the state-of-the-art published

papers fairly, the in-house figure of merit is adopted. The FOM of this work is comparable to other published papers, and the power consumption and supply voltage are the lowest in these published papers. The folded active inductor makes the proposed LA using active inductors at low supply voltage without any voltage boosting technique. The measured output eye diagram meets 2.5Gb/s OC48/STM16 mask specifications at 1V supply voltage.

## Acknowledgement

The authors would like to thank Chip Implementation Center, Taiwan, for chip implementation.

## References

- [1] M. Ingels, and M. Steyaert, "A 1-Gb/s 0.7 $\mu$ m CMOS optical receiver with full rail-to-rail output swing", *IEEE J. Solid-State Circuits*, vol. 34, pp. 971-977, July 1999.
- [2] A. Tanabe, M. Soda, Y. Nakahara, A. Furukawa, T. Tamura, and K. Yoshida, "A single-chip 2.4-Gb/s CMOS optical receiver IC with low substrate crosstalk preamplifier", *International Symposium on Solid-State Circuits Conference*, pp. 304-305, Feb. 1998.
- [3] W. Z. Chen, and C. H. Lu, "A 2.5 Gbps CMOS Optical Receiver Analog Front-End." *IEEE Custom Integrated Circuit Conference*, pp. 359-362, May 2002.
- [4] E. Säckinger, and W. C. Fischer, "A 3-GHz 32-dB CMOS Limiting Amplifier for SONET OC-48 Receivers," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1884-1888, Dec. 2000
- [5] S. Galal, and B. Razavi, "10Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18 $\mu$ m CMOS Technology", *International Symposium on Solid-State Circuits Conference*, pp. 188-189, Feb. 2003.

Table I. Performance and Comparison with the state-of-the-art papers.

	This work	[5]	[3]	[4]
Process	0.25 $\mu$ m CMOS	0.18 $\mu$ m CMOS	0.35 $\mu$ m CMOS	0.25 $\mu$ m CMOS
Supply voltage	1V	1.8V	3V	2.5V
Power consumption @ without buffers	4.2mW	100mW	77.5mW	53mW
Operating data rate	2.5Gb/s	10Gb/s	2.5Gb/s	2.5Gb/s
DC gain (differential)	39.9dB	50dB	42dB	32.3dB
Bandwidth (-3dB)	1.75GHz	9.4GHz	2.2GHz	3GHz
Chip area (mm <sup>2</sup> )	0.12	0.75	0.12	0.03
Input sensitivity	4mV <sub>pp</sub>	5mV <sub>pp</sub>	N/A	2mV <sub>pp</sub>
FOM	32.3	29.4	11.1	7.4