A 15mW 69dB 2Gsamples/s CMOS Analog Front-End for Low-Band UWB Applications

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***Abstract*—This paper presents a CMOS analog front-end (AFE) for short range impulse radio system in low-band ultra-wideband (UWB) based on 2ns width PAM modulation. The wideband amplifier provides 69dB gain from 30MHz to 1.2GHz, realized by a limiting amplifier with an active-inductor load and a cross-coupled g_m gain-boosting cell in each gain stage. The received signal is digitized at 2GHz sampling rate by the 8 parallel 1-bit ADCs, each of which is composed of transmission-gate type sample-and-hold circuits and a dynamic differential comparator. A timing generator based on a 4-stage ring oscillator in a PLL is employed to provide 8-phase 250MHz clocks. Realized in 0.18μm CMOS technology, the AFE occupies a 1.0 x 1.2 mm^2 active area with the 3rd order loop filter integrated in the same die. This chip also includes an integrated pulse generator for loop-back self-testing purpose. The receiver AFE achieves 200μV sensitivity and consumes 15mW from a 1.8V supply.**

I. INTRODUCTION

In recent years, the short-range impulse radio UWB below 960MHz has raised interests in the applications of radio frequency identification (RFID), localizer and sensor networks [1]. By using repetitive pulses, it transmits signals over a much wider frequency band than conventional carrier-based radio systems. The UWB system features in immunity to multi-path fading, potentially unlicensed operation due to the low spectral power density, security against eavesdropping, and penetrating through obstacles. Based on its application, the development of the impulse radio transceiver should target on low power consumption, low hardware complexity and low cost.

Due to the carrier-less property, power-consuming circuits, such as up/down conversion and IF filters, can be eliminated. The receiver is required to distinguish the digital data by correlating the pulses after adequate amplification. The correlation can be performed in the analog domain or the digital domain. The former requires timing signals with fine resolution and high performance mixer with integration and dump circuits. The latter digitizes the received signals and uses the digital circuits to conduct the correlation. This design is based on the digital correlation approach for its robustness in the pulse search procedure. The analog front-end complying with the digital backend is designed to achieve simple hardware complexity and low power consumption.

This paper presents an analog front-end (AFE) architecture and the circuit designs for the low band impulse radio UWB. Section II introduces the designed signals and circuit specification. The circuit architecture is described in section III. In section IV, the simulation results are presented. Finally, section V draws the conclusion.

II. SIGNALING AND SYSTEM SPECIFICATIONS

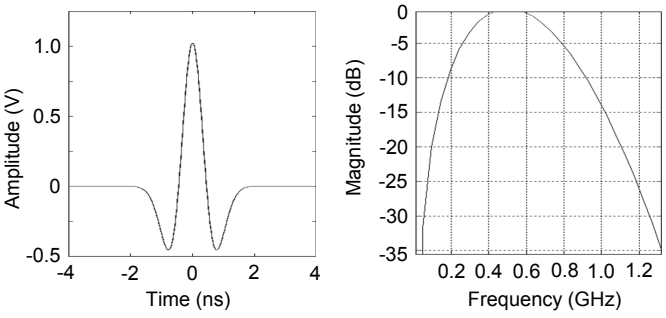

Fig. 1 The received pulse and its spectrum

This impulse radio system adopts binary pulse amplitude modulation (PAM) with 2ns width pulses for the signal band from 30MHz to 960MHz. After the differentiation effects caused by the antenna, the received pulse is modeled by a 2nd derivative Gaussian pulse shape [2] derived in (1). The time domain shape and spectrum are shown in Fig. 1. The received signals are then sampled at 2Gsamples/s for pulse correlation and data detection. The pulse repetition time is another issue to design the signaling. Short pulse repetition time increases the data rate, but has severe interference problems. On the contrary, long pulse repetition time provides better immunity while lowering the data rate. Based on the channel property, the RMS delay is 10~20ns [3]. In this work, the pulse repetition time is designed to be 16ns.

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$$p(t) = A[1 - 4(\frac{t}{T_d})^2]e^{-2\pi(t/T_d)^2} \quad (1)$$

The pulse train is further spread by a Golay spreading code [4]. It provides identification for different users, and smoothes the spikes of the spectrum. The longer the spreading code is, the better immunity to interferences and noises the system has. However, it reduces the data rate since it uses multiples of pulses to send one bit of data. Based on different channel conditions, the length of spreading code is designed from 0 to 1024, and the corresponding data rate is 62.4Mbps to 61kbps, respectively.

For the required transmitted power should be less than -41.3dBm/MHz regulated by FCC, the emitted pulses have the power of -17dBm over the effective bandwidth of 500MHz. According to the indoor channel analyzed by USC [3], the maximum path loss in 10 meters is 64dB. Considering the implementation loss of 10dB, the desired total gain of the receiver is 74dB. With the gain of the LNA is 10dB, the gain of the succeeding font-end circuits in the receiver should be above 64dB. .

III. ANALOG FRONT-END ARCHITECTURE

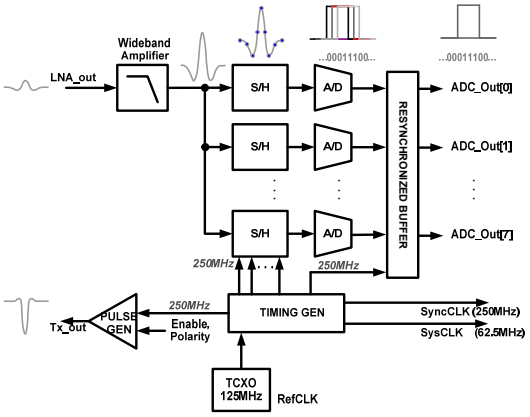


Fig. 2 Analog front-end architecture

The reception of the impulse radio signals requires high speed sampling with precise timing for the correlation procedure. Fig. 2 shows the proposed analog front-end circuit architecture that contains a wideband amplifier, 8-channel parallel 1-bit ADCs and resynchronization buffer clocked by a built-in timing generator. The amplifier provides 64dB gain so that the output voltage fits in the detectable range for the ADCs in the 10-meter transmission range. The minimum input of the wideband amplifier is 200uV, and the minimum input of the ADCs is 100mV considering the output offset of the amplifier. The resynchronization buffer resynchronizes the 8-phase consecutive outputs from the ADCs to facilitate the digital baseband to detect the impulse and decode the data. The timing generator provides precise timing signals for ADCs at the 2Gsamples/s sampling rate and with 100ps jitter tolerance [1]. It utilizes the 4-stage ring oscillator in a PLL loop to generate 8 phases of 250MHz clocks with an external 125MHz TCXO reference. In addition to the receiving path, a simple pulse generator is implemented for self-test purpose to generate 2ns wide pulses based on the on-chip timing signals. The circuit design of each block is detailed as follows.

A. *Wideband Amplifier*

The wideband amplifier is configured as a limiting amplifier as shown in Fig. 3. It consists of four gain stages providing a total gain of 69 dB and a buffer stage driving the parallel ADCs that appear as about 4pF load. Due to the high voltage gain, the circuit is sensitive to offsets and thus DC offset cancellation network is added in the negative feedback path. The extraction network is a low-pass filter using on-chip MOS resistors and MOS capacitors with the cut-off frequency at 30MHz. The resulting amplifier loop has the 30MHz to 1.2GHz bandpass characteristics.

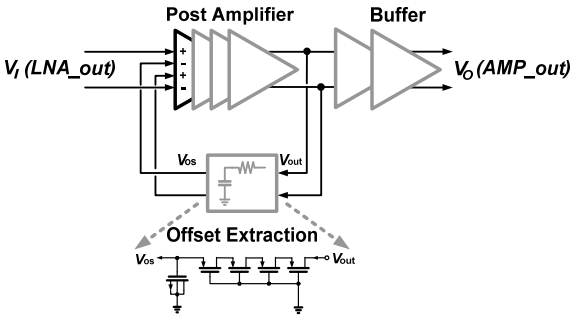


Fig.3 Wideband amplifier with offset cancellation

Each gain cell, shown in Fig. 4(a), employs a differential pair to provide high gain and broad bandwidth. The active inductor is used as the load to cancel the output pole and enhance its frequency response [5]. Cross-coupled NMOS transistors are put at the output nodes to provide high output impedances and increase the voltage gain. The first gain stage has another input from the offset extraction feedback and demands a subtraction function to remove the effect. Shown in Fig. 4(b), it resembles the gain stages except the cross-coupled devices are replaced by the negative offset feeding ones.

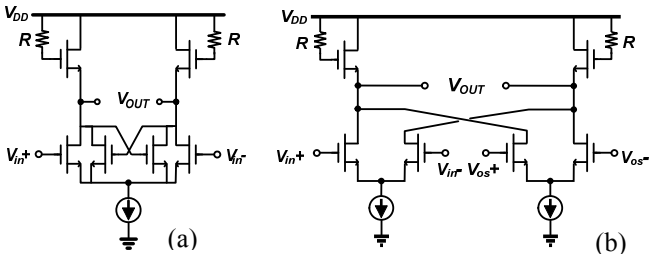
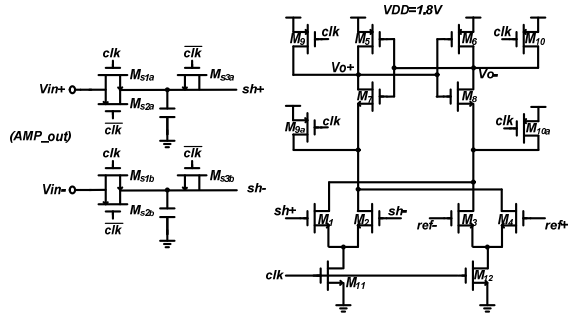


Fig. 4 (a) Gain stage circuit (b) Offset subtractor

B. *ADC*

The 1-bit ADC contains a sample-and-hold circuit and a differential comparator, shown in Fig. 5(a) and 5(b) respectively. The sample-and-hold circuit employs the transmission gate to reduce the input impedance variation

during the on/off states. The dummy switch is added after the transmission gate and the hold capacitor to eliminate the clock-feed-through effect.



(a) (b)

Fig. 5 (a) Sample-and-Hold Circuit (b) Differential comparator

Fully differential circuitry is used to have better power noise rejection and immunity to common mode noises. Differential comparator is employed as in Fig. 5(b) with auxiliary transistors M_{9a} and M_{10a} that help to pre-charge and pre-discharge the output latches and speed up the response. It results in 0.2ns rise time and 0.3ns fall time in state transition. However, device mismatches in the differential circuits brings about the comparator offset. From Fig. 5(b), by setting transistors channel width W_2=W_4=W_A and W_1=W_3=W_B, the input voltage that changes the comparator state is [6][7]

$$sh^+ - sh^- = \frac{W_B}{W_A}(ref^+ - ref^-) \qquad (2)$$

By varying W_A and W_B, the threshold of the comparator can be adjusted to the desired level. Equation (2) implies that the offset of the comparator depends on the mismatches among M_1-M_4 when M_5-M_{12} are assumed to match perfectly.

Furthermore, the total offset voltage consists of the sum of the offsets in both source coupled pairs. The offset voltage of one differential pair can be derived as [6]

$$V_{OS} = \Delta V_T + \frac{V_{gs} - V_T}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta\beta}{\beta}\right) \qquad (3)$$

where ΔV_T, ΔR_L and $\Delta\beta$ are the mismatches of threshold voltage, load resistance and transistor dimension respectively. V_T, R_L and β are their average values. The offset voltage in this comparator architecture is dominated by $\Delta\beta$, which suggests that the lower the V_{gs}, the smaller the offset [6].

C. *Timing Generator*

Fig. 6 shows the architecture of the timing generator. The ring oscillator VCO is composed of 4 delay stages to provide 8 phases clocks at 250MHz for the ADCs. A third order loop filter is integrated in the chip with MIM capacitors and Poly resistors to set the loop bandwidth to 5MHz. The delay stage is a differential pair with the symmetric load [8] controlled by the self-biased circuitry, as depicted in Fig. 7. The bias voltage of the NMOS current source is continuously adjusted in order to provide a bias current independent of supply and substrate voltages. The self-bias network takes advantage of the replica of the delay cells and generates the proper biasing voltages for the PMOS loads and the NMOS tail current devices from the control voltage generated by the loop filter.

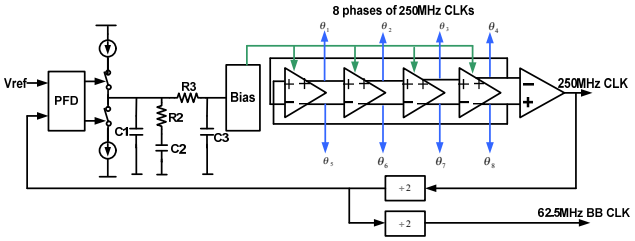


Fig. 6 Timing generator circuit

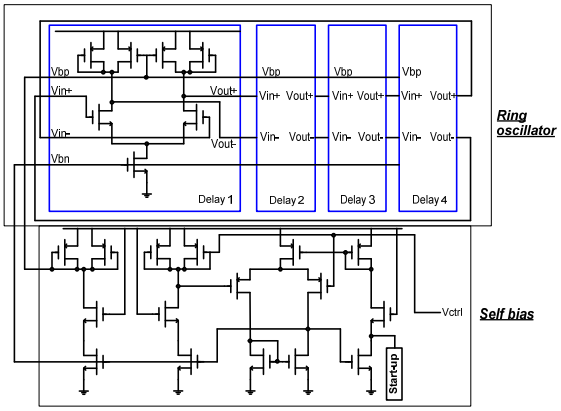


Fig.7 VCO and self-bias circuits

IV. Simulation Results

The front-end circuits for UWB are designed using 0.18μm CMOS technology. The receiving blocks have been integrated and simulated using SpectreRF. Fig. 8 shows the post-layout simulation results of the wideband amplifier frequency response. The gain achieves 69dB for the bandwidth from 30MHz to 1.2GHz. Besides, it has linear phase response in the band of interest. Fig. 9 shows the post-layout simulation results of the 1-bit ADC with the input threshold of 100mV. When the input pulse is amplified to above 100mV, the ADC acquires the correct data and outputs the digital signals in 1 bit. Under different process corners and temperature conditions, the 1-bit ADCs can operate correctly to digitize the input pulses. Fig. 10 shows the 8 phases of 250MHz clocks from the designed timing generator. For different process corners from the foundry models, the timing signals provide stable and precise timing information. The total power consumption for the whole chip is 15mW with 1.8V power supply. Shown in Fig. 11, the chip occupies 1.0 x 1.2 mm^2 active area. The performance of this chip is summarized in Table 1.

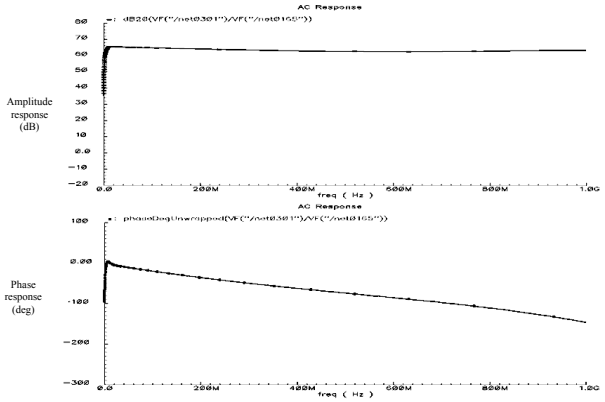


Fig. 8 The amplitude and phase responses of the amplifier

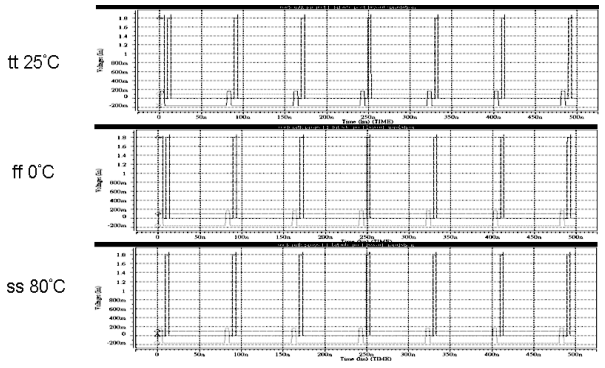


Fig. 9 Post-layout simulation of 1-bit ADC

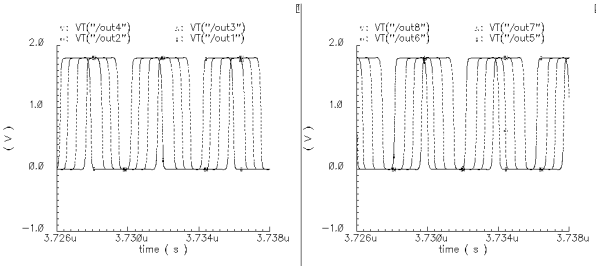


Fig. 10 Post-layout simulation results of timing generator

Table 1 Performance summary of UWB AFE

Design Technology	**0.18um CMOS 1P6M**
Chip core area	**1.0 x 1.2 mm^2**
Power consumption	**15mW**
Receiver sensitivity	**200uV (minimum)**
Gain of receiver chain	**69dB**
AFE bandwidth	**30MHz-1.2GHz**
AFE sampling rate	**2Gsamples/s**
ADC resolution	**8-phase parallel 1 bit**
Internal clock rate	**8-phase 250MHz**
Clock jitter	**100ps**

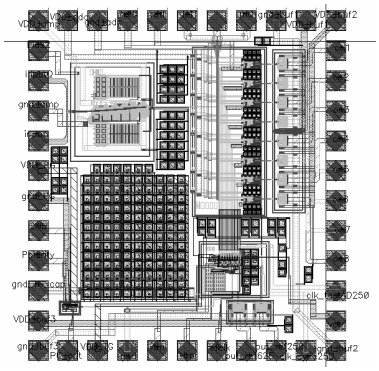


Fig. 11 Layout of low-band UWB AFE

V. CONCLUSION

A single chip receiver analog front-end is designed for the impulse radio UWB system. For the low-band UWB operation, the pulse generator generates 2ns width PAM pulses in 16ns pulse repetition time. The AFE provides 69dB gain with a limiting amplifier that achieves high gain and wide bandwidth by using an active-inductor load and a cross-coupled g_m gain-boosting stage. It produces 1-bit digital signals at 2GHz sampling rate for digital correlation by 8 parallel ADCs clocked by a timing generator with 8 phases of 250MHz clocks. Implemented in 0.18μm CMOS technology, the chip integrates all the front-end circuits and consumes 15mW from a 1.8V supply.

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