A 0.9-V 67-µW Analog Front-End using Adaptive-SNR Technique for Digital Hearing Aid

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***Abstract*—An analog front-end composed of a preamplifier and a Σ-Δ modulator is proposed and implemented for digital hearing aid chip. Combined gain control (CGC), the technique, which incorporates an automatic gain control (AGC) with an exponential gain control (EGC), is employed to enlarge dynamic range and reduce power consumption. The proposed Σ-Δ modulator exploits adaptive-SNR technique, which generates four different SNRs, thereby achieving low power consumption and optimizing performance. The measured power dissipation of the preamplifier is 35-µW. In case of Σ-Δ modulator, the peak signal-to-noise ratio (SNR) is 86-dB, the average power consumption is 31.4-µW and the variation of SNR is 14-dB. The proposed analog front-end dissipates less than 67-µW from a single 0.9-V supply. The core area of the preamplifier and the Σ-Δ modulator is 0.1-mm^2 and 0.4-mm^2, respectively, in a 0.25-µm standard CMOS technology.**

I. INTRODUCTION

Explosive growth for a biomedical electronic system market needs more low-power and low-voltage techniques than before [1]. Accordingly, an improvement in both of power dissipation and a performance of a digital hearing aid is necessary. Figure 1 shows a block diagram of a typical digital hearing aid system, consisting of five blocks: a preamplifier, a Σ-Δ analog-to-digital converter (ADC), a digital signal processing unit (DSP), a Σ-Δ digital-to-analog converter (DAC), and a receiver driver. Among these individual blocks, an analog front-end that comprises a preamplifier and a Σ-Δ modulator is reported to consume a major part of the total power [2], [3]. Therefore, reducing the power consumption of the analog front-end is attractive to decrease the total system power consumption.

In this paper, a new analog front-end architecture is proposed and implemented to achieve low power consumption with a 0.9-V supply voltage. Although lower supply voltage can be another effective solution, it may cause significant degradation of the system performance and make the analog circuit design difficult. In the proposed analog front-end, the preamplifier with combined gain control (CGC) and the Σ-Δ modulator which exploits adaptive-SNR technique are included.

The detail architecture of the proposed front-end will be explained in Section II. Section III will describe the circuits

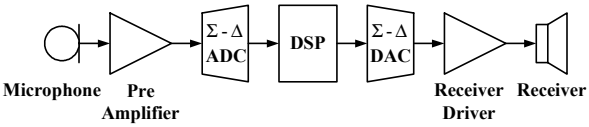

Figure 1. Block diagram of a digital hearing aid system

of the preamplifier with measurement results. In Section IV details of the Σ-Δ modulator will be covered. Finally, conclusions will be made in Section V.

II. SYSTEM DESIGN CONSIDERATIONS

Figure 2 shows the relation between the input of the microphone and the input of the preamplifier.

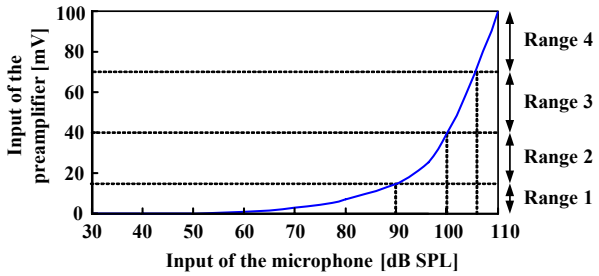

Figure 2. Characteristics of a microphone for a digital hearing aid

A previous study revealed that a normal sound level common in human daily life ranges from 30 to 90-dB SPL, which corresponds to Range 1 in Figure 2 [4]. In this range, the amplitude of the sound is so small that a high performance analog front-end must be used. On the other hand, above 90-dB SPL, Ranges 2 ~ 4 of Figure 2, the sound level is sufficiently large that analog front-end needs not to provide high gain. Obviously, for a small sound the high performance analog front-end is indispensable. But for the large sound, the conventional analog front-end may over-perform and cause unnecessary power consumption.

In this paper, a new analog front-end architecture is proposed to satisfy not only a high performance for a small sound but also a power optimization for a medium to large sound amplitude.

In the conventional design of a preamplifier, an automatic gain control (AGC) and an exponential gain

control (EGC) are designed separately because of design difficulties. In this study, however, CGC integrates AGC and EGC into a single block to reduce power consumption. In the design of the Σ-Δ modulator, the input sound level is divided into four parts as shown in Figure 2 to control the SNR separately at each range achieving power-optimized performance.

III. PREAMPLIFIER

A. Circuit Design

Figure 3 illustrates the suggested preamplifier. The gain of the proposed preamplifier is given as follows.

$$\frac{OUT}{IN} = gain = \frac{W_1 L_2 \left(1 + \frac{V_x}{V_{dd} - V_{VC}}\right)}{W_2 L_1 \left(1 - \frac{V_x}{V_{dd} - V_{VC}}\right)}, \quad \begin{aligned} V_1 &= V_{VC} - V_x \\ V_2 &= V_{VC} + V_x \end{aligned} \qquad (1)$$

where V_{VC} is a volume control voltage, and V_1 and V_2 are resistance control voltages generated by the gain control unit (GCU). GCU changes V_x according to the input signal V_{VC}. The EGC and AGC functions can be realized by controlling V_{VC} and V_x.

MOS resistive circuit (MRC) is implemented using four N-type transistors. It helps CGC to get the exponential gain characteristics with V_{VC} as a control signal. Moreover, a threshold knee point of the preamplifier can be changed by modifying V_{TH}. When the input sound level is high, low V_{TH} is used to reduce power dissipation and enlarge dynamic range of the preamplifier. The peak detector (PD) senses the envelope of the preamplifier output voltage and controls the GCU.

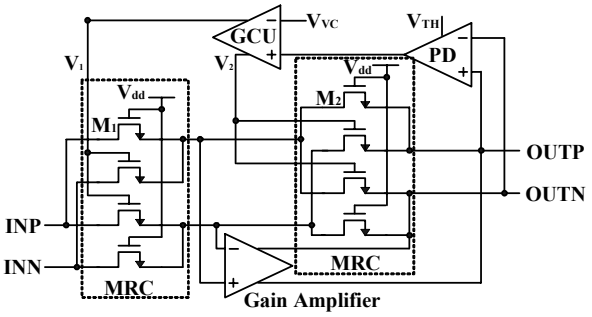

Figure 3. Proposed preamplifier with CGC technique

B. Measurement Results

Figure 4 shows the preamplifier microphotograph in a 0.25-μm CMOS process. In Figure 5, the measured gain and threshold knee point variations are presented as a function of V_{VC} with V_{TH} as a parameter. Because the human sense of hearing of the loudness of sound operates on a logarithmic scale and the preamplifier outputs go up linearly with the input on the same scale, it is found to operate as a volume control successfully. By reducing V_{TH}, the threshold knee point is decreased simultaneously. By preventing unnecessary high gain, it reduces power dissipation according to external conditions. Power consumption of the preamplifier is 35-μW and its core area is 0.1-mm^2

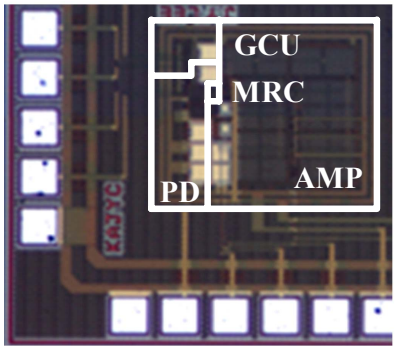

Figure 4. Chip microphotograph of the proposed preamplifier

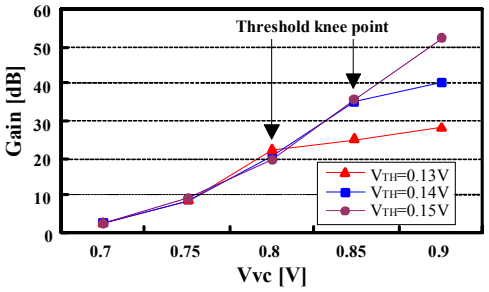

Figure 5. Measured performance of the proposed preamplifier

IV. Σ-Δ MODULATOR

A. Circuit Design

To realize the proposed adaptive-SNR technique, the Σ-Δ modulator should provide four kinds of SNR for each range of Figure 2. By changing the clock frequency, the Σ-Δ modulator achieves different SNR characteristics, thereby obtaining power-optimized performance to specific sound range. But high clock frequency incurs a number of difficulties in design of analog circuit such as operational transconductance amplifier (OTA), because the unity-gain frequency of the OTA should be at least four times higher than the clock frequency of the Σ-Δ modulator [5]. The clock frequency is selected as 1.024-MHz and 2.048-MHz with the oversampling ratio (OSR) of 64 and 128, respectively. Higher order Σ-Δ modulator is another approach to change values of SNR. However the performance of more than 3rd order Σ-Δ modulator seriously suffers from nonidealities such as finite gain and bandwidth of the OTA and instabilities caused by saturation of the integrator [6]. In order to minimize side-effects of the higher order Σ-Δ modulators and change the SNR characteristics, the order of the Σ-Δ modulator must be limited under three.

The MATLAB simulation results in Figure 6 show that the proposed Σ-Δ modulator accomplishes different SNR and SNDR values according to the input amplitude.

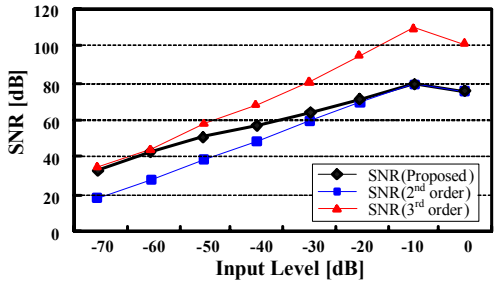

Figure.6. Simulated results of conventional vs. proposed Σ-Δ modulator

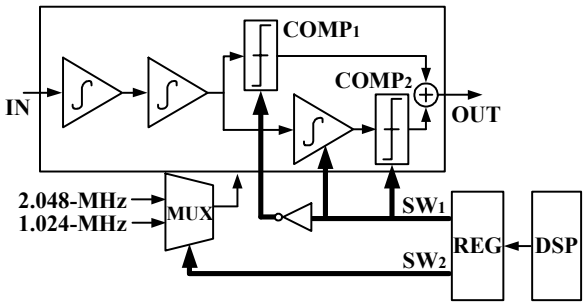

Figure 7. Proposed Σ-Δ modulator architecture

The architecture of the proposed Σ-Δ modulator is described in Figure 7. SW_1 determines the order of the Σ-Δ modulator between the second and third while SW_2 decides the clock frequency of the Σ-Δ modulator. A combination of these two switches allows the Σ-Δ modulator to obtain four kinds of SNRs. For easy and convenient control, these parameters of the switches are stored and applied by the control register in a DSP. By choosing the proper values according to the external sound amplitudes, the proposed Σ-Δ modulator obtains power-optimized SNR.

Figure 8 shows the schematic of the proposed Σ-Δ modulator. When the $/SW_1$ is closed, this Σ-Δ modulator operates in 2nd order by bypassing the output from the 2nd integrator to the OUTN or OUTP. Because the resistance value of the conventional N-type switch varies according to the drain voltage, the 2nd integrator output degrades seriously when it passes through $/SW_1$. Hence, in order to prevent this distortion, high performance switch of which resistance is stable under all drain voltages is demanded. However, implementation of such a switch is difficult to design and consumes extra power. Therefore, this paper exploits a new method by using $COMP_1$. It converts 2nd integrator output into a PWM signal and pass it through the $/SW_1$ without signal distortion. When the $COMP_1$ is activated, the 3rd integrator and $COMP_2$ are completely turned off to eliminate extra power consumption. On the other hand, if the $/SW_1$ is opened, the 3rd integrator accepts the output of the 2nd integrated as an input and performs the 3rd order modulation. In this phase, $COMP_1$ is turned off to avoid extra power dissipation. By turning SW_2 on and off, the clock frequency can be selected between 2.048-MHz and 1.024-MHz, respectively. By controlling SW_1 and SW_2 together, four types of the Σ-Δ modulators having different kinds of SNR are obtained. With SW_1 open, type 1 and type 2 2nd order Σ-Δ modulators are achieved by turning SW_2 off and on, respectively. With SW_1 closed, type 3 and type 4 3rd order Σ-Δ modulators are realized by turning SW_2 off and on, respectively.

In Figure 9 a low power OTA is presented for the Σ-Δ modulator. It is composed of a compensated two-stage, a cross-coupled active load, and a class AB output stage [7]. It demonstrates 77.6-dB DC gain, 7.07-MHz unity gain bandwidth, and a 55° phase margin for a 3-pF load.

A 1-bit quantizer i.e., COMP1 and COMP2 with a clocked circuit minimizes the hysteresis and offset voltage [8].

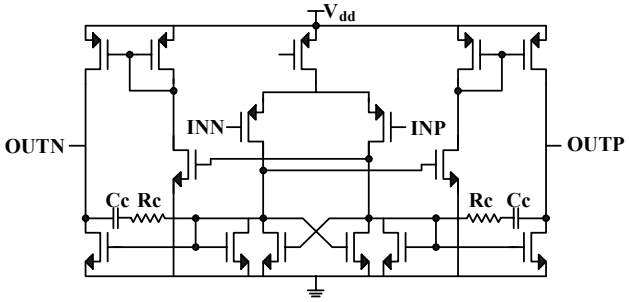

Figure 9. Two-stage/class AB OTA

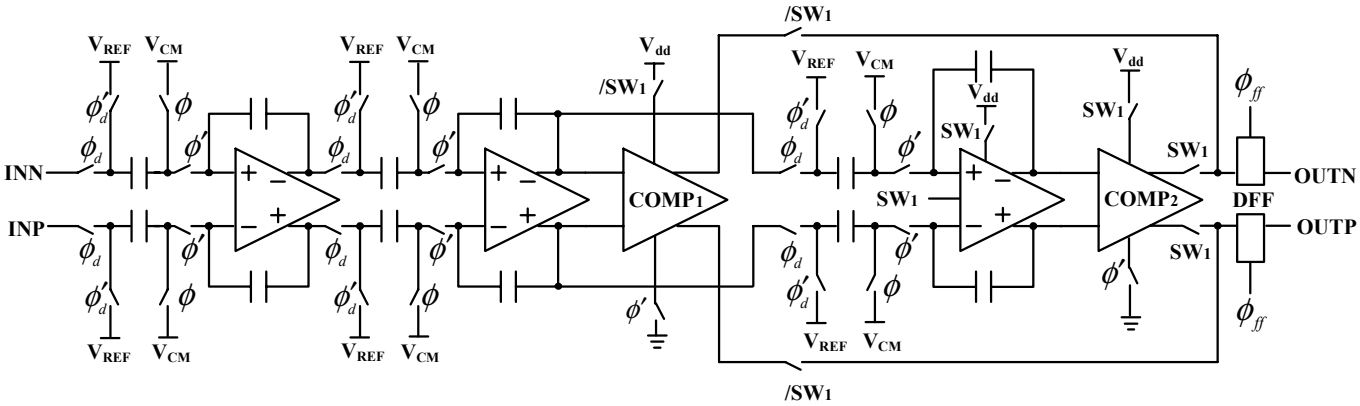

Figure 8. Σ-Δ modulator exploiting adaptive SNR technique

B. *Measurement Results*

The Chip microphotograph of the proposed Σ-Δ modulator is shown in Figure 10. It was also fabricated in a 0.25-μm CMOS process and its core size is 0.4-mm^2

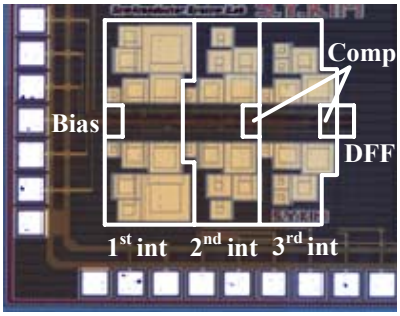

Figure 10. Chip microphotograph of the proposed Σ-Δ modulator

Figure 11 describes the measured output spectrum of a type 1 modulator with 2-kHz sinusoidal input signal and 1.024-MHz clock frequency. Under these conditions, the measured peak SNR is 72-dB. Figure 12 shows the measured SNR and SNDR as a function of input.

Table I summarizes the performances of the Σ-Δ modulator with combination of SW_1 and SW_2. When the input sound is less than 90-dB SPL, this modulator acts as a type 4 modulator to offer high performance. But if the sound is higher than 105-dB SPL, the Σ-Δ modulator operates as the type 1 to reduce its power dissipation.

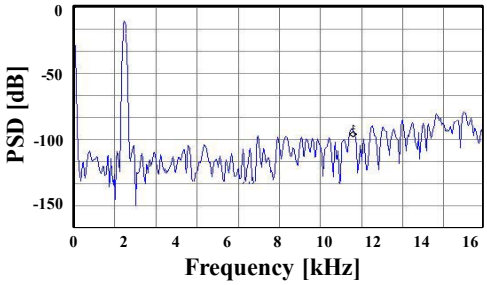

Figure 11. Measured spectrum of the proposed Σ-Δ modulator

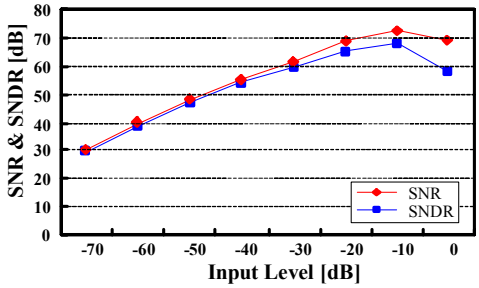

Figure 12. Measured SNR / SNDR vs. input amplitude

The performance comparison of the proposed analog front-end with that of conventional works is described in Table II. Compared with previous works, the proposed analog front-end dissipates the lowest power consumption at 0.9-V power supply voltage.

TABLE I. Σ-Δ MODULATOR PERFORMANCE SUMMARY

Order of Modulator	2		3	
Type	1	2	3	4
Clock Frequency (MHz)	1.024	2.048	1.024	2.048
Oversampling Ratio	64	128	64	128
Peak SNR (dB)	72	81	78	86
Power Consumption (µW)	26.4	26.8	35.7	36.7
Signal Bandwidth (kHz)	8			
Die Size (core area)	570-µm × 690-µm			

TABLE II. PERFORMANCE COMPARISON OF THE ANALOG FRONT-END

	JSSC 1997 [2]	**JSSC 2002 [3]**	**This work**
Supply Voltage (V)	2.15	1.1	0.9
Peak SNR (dB)	77	92	86
Power Consumption (µW)	323	190	67 (avg.)
CMOS Technology	0.8-µm	0.6-µm	0.25-µm

V. CONCLUSION

A new analog front-end is designed and realized in a 0.25-µm standard CMOS process for a digital hearing aid. By exploiting CGC and adaptive-SNR technique, the proposed analog front-end reduces power consumption and obtains large dynamic range. The proposed preamplifier consumes 35-µW and 0.1-mm^2 area. The peak SNR of the Σ-Δ modulator is 86-dB and average power consumption is 31.4-µW with 0.4-mm^2 core area. The SNR varies over 14-dB range and power consumption changes 11.5-µW from type 1 to type 4. The proposed analog front-end dissipates less than 67-µW from a single 0.9-V supply.

ACKNOWLEDGEMENTS

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