A 12-bit Current Steering DAC For Cryogenic Applications

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***Abstract*—This paper present a 100MHz 12-bit digital to analog converter (DAC) capable to work under ultra-wide temperature (UWT) range from -180°C to +120°C and at ultra low temperature (ULT) of -230°C. To obtain high resolution and good speed over the UWT, partial thermometer-decoded and segmented scheme is employed. A bandgap voltage reference is designed for UWT applications. The cryogenic DAC chip is implemented in a 0.5μm SiGe technology with die area of 4.08×2.34 mm^2 and total power consumption of 105mW with a 3.3V supply voltage.**

Index Terms—**digital to analog converter (DAC), bandgap reference (BGR), ultra-wide temperature (UWT), ultra low temperature (ULT).**

I. Introduction

Digital to analog converter (DAC) is a critical component in modern mixed signal systems. It's critical to accomplishing the vision for space exploration of habitats, rovers, mining and manufacturing, distributed sensors, etc. Mixed signal systems capable of operating in the extreme environment will reduce design complexity, increase flexibility and modularity, reduce power consumption and increase system reliability. However, DACs are not available today that will operate exposed to the extreme environment. This is problematic, since the development of modular, expandable, and reconfigurable human and robotics systems for space application clearly requires electronic components and integrated packaged electronics modules which can operate robustly without bulky and power inefficient external thermal control. This paper presents a 12-bit current-steering DAC design that is capable of operating over an UWT range (-180°C to 120°C) and for a worst case at ULT of -230°C for deployed space surface entities.

Unlike other conventional IC technologies, SiGe offers unparalleled cryogenic temperature performance, radiation tolerance, wide temperature range capability, and optimal mixed-signal circuit design flexibility at the monolithic level by offering power efficient, multiple breakdown voltage, high-speed transistors (SiGe HBTs) together on the same piece of silicon wafer with high density Si CMOS and passive components [1][2]. The DAC presented in this paper is based on SiGe technology to obtain better application performance.

In section II, the 12 bit DAC design for cryogenic applications will be presented. The DAC employs a 6MSB+4NSB+2LSB systematic structure that achieves the optimized performance considering the precision, the complexity and the speed of the DAC. The simulation results and layout design of the DAC chip will be given in section III and IV, respectively.

II. Circuit Design

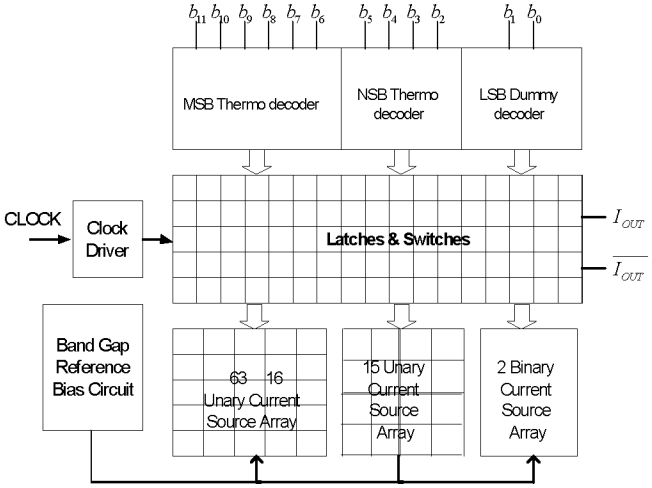

Fig.1 Block diagram of proposed cryogenic DAC.

This on-chip 12-bit DAC is implemented by using the 6MSB+4NSB+2LSB segmented current steering architecture, as shown in Fig. 1, which includes thermometer decoder, current switch logic array, and segmented current source array, clock driver and bandgap voltage reference, etc.

For a 12-bit current-steering DAC, segmentation for significant bits can be applied to reduce the currents through current switches [3]. The thermometer-based DAC has advantages over its binary counterpart, such as low differential nonlinearity (DNL), guaranteed-monotonic and reduced glitch noise. However, it is not feasible to use a full thermometer code representation for all bits in high-resolution converters, since the number of switches and the complexity of the interconnection wires grow exponentionally with increasing number of bits. Therefore, for the 12-bit DAC design, there is a trade-off between the number of bits to segment and the impact on layout complexity, glitches, mononicity, precision, integral non-linearity (INL), DNL and speed etc [4].

Generally, an optimal and practical method is to use the multi-segmented structure [5]. The M MSBs are

thermometer coded in one cluster, the K LSBs are kept binary coded, and the N-M-K intermediate bits are also thermometer coded in another separate cluster. For 12-bit DAC, we thus choose 6MSB+4NSB+2LSB to keep the best balance between minimizing the circuit area of thermometer decoders and optimizing the DAC performance to meet $INL \leq 1LSB$ and $DNL \leq 0.5LSB$.

The 6 MSBs of the digital binary inputs are thermometer-decoded to control 63 current sources, each having 16-NSB current weighting, and 4 thermometer-decoded NSBs to control 15 current sources with unit-NSB current weighting, while the remaining 2LSBs controls 2 binary-weighted current sources. The output currents of all current sources, which are switched ON and OFF according to the digital input codes, are summed and driven into any resistive load in order to generate the required analog output voltage. The DAC comprises current cell matrix, current switch matrix, decode circuit and a bias generator [6].

Fig. 2 shows the current source units for four different segmented bit cells, MSB, NSB, LSB1 and LSB2. The current relationship between them is,

$$I_{MSB} = 16I_{NSB} = 32I_{LSB1} = 64I_{LSB2} \quad (1)$$

which corresponds to the segmentation of DAC. In addition, All bits cells are composed of PMOS FETs with same size to minimize the process mismatch error during fabrication. Precise design and simulation is necessary to make all bits cells working in saturation region.

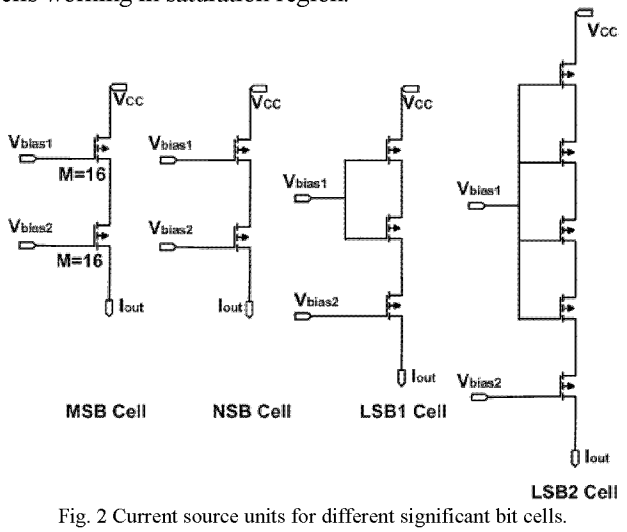

Fig. 2 Current source units for different significant bit cells.

In this DAC, we use PMOS FETs as current source sink to get stable current source for switch circuit with more accuracy and more convenience. Compared with NMOS FETs, PMOS FETs have smaller 1/f noise and don't need additional output pull-up circuit to make output load connected with power supply, which would guarantee much convenience and compatibility when cascaded with following circuits. Meanwhile, P-well of PMOS FETs can effectively eliminate the crosstalk transmitted by substrate and other noises.

For LSB_1 and LSB_2 current switch cells, since the D_0 and D_1 input signals aren't converted into thermometer code, there is an apparent delay difference compared with other significant bits. This delay difference will make MSB and LSB switches switched ON asynchronously, which consequently cause worse DNL and INL as well as output current error. Therefore, one LSB dummy decoder composed of inverters in even number is used to remove such unfavorable effect.

To avoid that current switch transistors are completely switched off simultaneously and consequently minimize current glitches, differential switches are used so that the current source always delivers current. It is also necessary for switching signals to be properly matched to reduce the glitches. Meanwhile, we need to keep the rise and fall behavior of the switch signals as equal as possible to improve the dynamic performance of DAC.

The switching transistors with minimum size should be chosen to achieve the fastest switching speed with minimum power consumption and to reduce the effect of clock feed-through (CFT). However, considering the short channel effect, transistor matching and reliability over UWT, medium size NMOS with W/L=10/1μm and 3-paralleled PMOS with the same W/L=10/1μm are chosen for the cryogenic DAC design. Moreover, paralleled switching transistors with the same aspect ratio that indicate larger size were used for MSB cells in order to lower the voltage across the transistors with some penalty of increased CFT due to the increased gate capacitance.

For current-steering type of converter, the static and dynamic characters of DAC including DNL, INL and Signal Noise Ratio (SNR), spurious free dynamic range (SFDR) are tremendously dependent with the accuracy and stability of internal-generated current reference. As a result, It necessitates stable and temperature-independent bandgap reference working in the UWT scope from -180°C to +120°C.

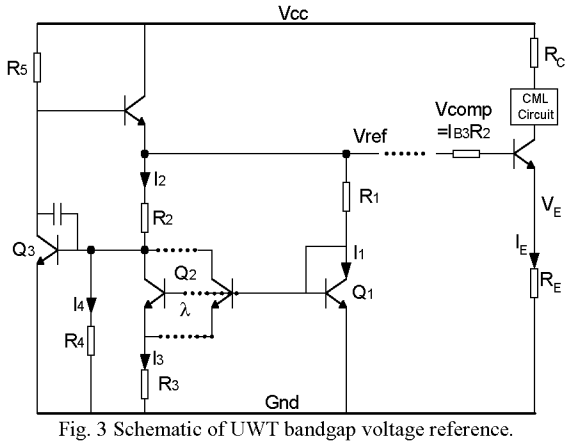

Fig. 3 Schematic of UWT bandgap voltage reference.

The bandgap reference for UWT application is showed in Fig. 3. The bandgap reference voltage can be found as

$$V_{ref} = R_2 I_{B3} + V_{BE3}\left(1+\frac{R_2}{R_4}\right) + V_T \frac{R_2}{R_3}\ln\left(\lambda \frac{I_1}{I_3}\right) \quad (2)$$

where $V_T=kT/q$ and λ is the number of transistors Q_2 in parallel.

Thus, the current flowing through the current source is given by

$$I_E = I_S \exp\left(\frac{V_{ref} - I_{B3}R_2 - R_E I_E}{V_T}\right) \quad (3)$$

Utilizing the positive temperature coefficient of V_T and the negative temperature dependence of V_{BE}, one can thus generate constant current over UWT.

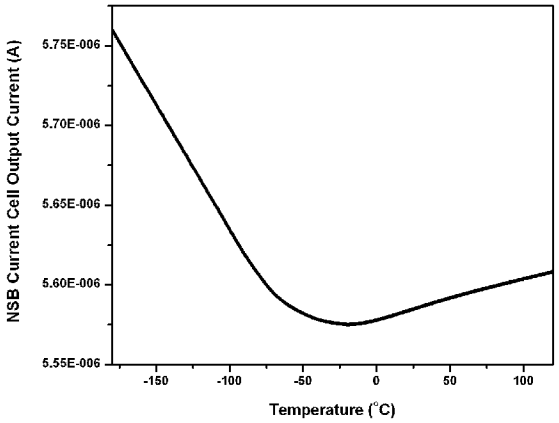

Fig. 4 NSB output current versus temperature from -180°C to 120°C.

Fig.4 shows the simulation output current of NSB current source cell which is generated by the bandgap reference we proposed. The current output at -180°C is 5.76μA, and the smallest current is 5.575μA at -25°C. Thus, the effective temperature coefficient is 110.4ppm/°C, which guarantee that every segmented bit can obtain stable, accurate and temperature-independent current. In addition, when temperature drops down to -230°C, the current output reaches 5.87μA.

In the current steering DAC, the impedance Z_{imp} seen in the drain of the switch transistors of each current cell has to be made large enough so its impact on the INL specification of the DAC can be tolerated [6]. However, the Z_{imp} is frequency dependent. The impedance that is required to obtain a certain resolution can be calculated and approximately equals to

$$Z_{imp} = \frac{NR_L}{4Q} \quad (7)$$

where R_L means the load resistance, N represents the total number of unit current sources and Q is the ratio between the signal and the second harmonics. To obtain 12 bit output resolution, Z_{imp} has to be about 750kΩ.When the frequency goes to above 100MHz, cascode current source is needed to meet the requirement of Z_{imp}.

III. Simulation Results

Figure.5 and Figure.6 give the converted sine waveforms at 5MHZ output frequency with the 100MHz input sampling clock frequency at the temperature of 25°C and -230°C, respectively. Their simulated output spectrums are presented in figure.7 and figure.8, respectively.

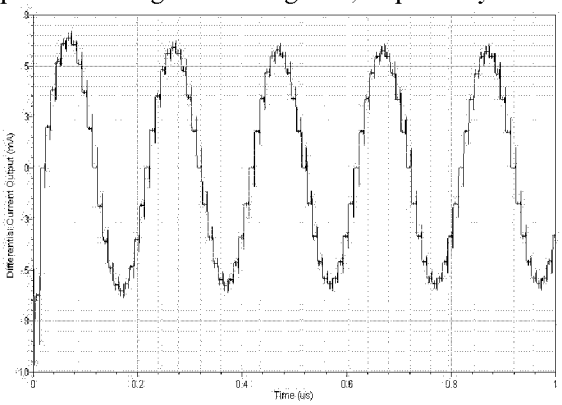

Figure.5 Differential output current waveform with f_{out} =5MHz and clock =100MHz at 27°C.

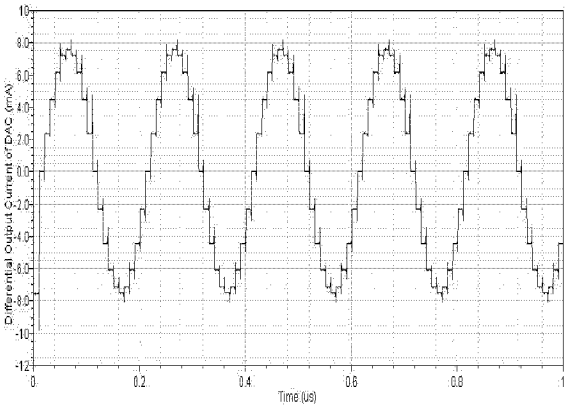

Figure.6 Differential output current waveform with f_{out} =5MHz and clock=100MHz at -230°C.

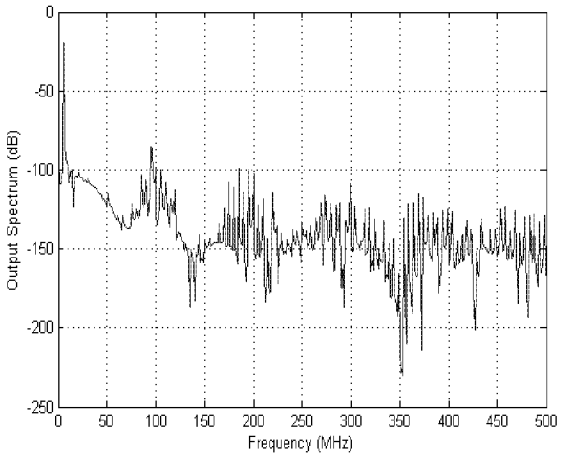

Figure.7 Output spectrum f_{out} =5MHz with clock =100MHz at 27°C.

The amplitude current of the differential outputs is about 6mA. Before deglitching low pass filtering, the SFDR of 5MHZ output frequency with 100MHZ clock at the temperature of -230°C is about 62.2dBc, while the SFDR at 25°C is about 65.8dBc. The total power consumption at 100MHZ with 3.3V power supply voltage is roughly 105mW at -230°C and 103mW at 25°C, respectively.

Simulation results have indicated that proposed DAC is capable to provide comparable performance under the -230°C ultra-low temperature condition as good as room temperature condition. At the same time, the applications for ultra-wide temperature scope from -180°C to +120°C are also guaranteed.

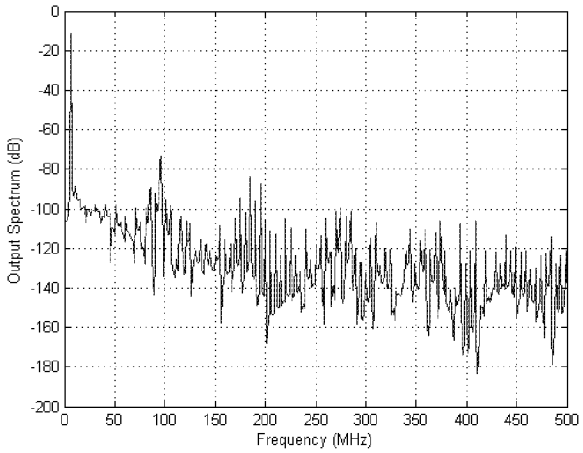

Figure.8 Output spectrum f_{out} =5MHz with clock =100MHz at -230°C.

IV. Layout of the Cyrogenic DAC

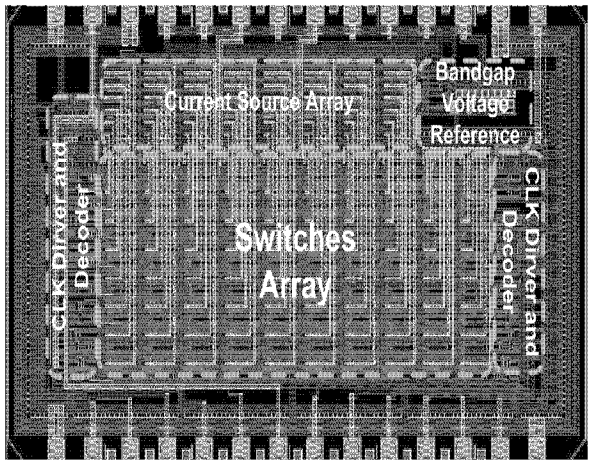

Fig. 9 Layout of cryogenic DAC.

We have implemented the proposed DAC in a 0. 5μm SiGe technology. The layout of the DAC chip is showed in figure.9, which includes bandgap reference, decoder block, current array and switch array. The size of whole layout chip is 4.08mm × 2.34mm. The current sources array and the switches are placed in a separate array to avoid coupling from the digital signals to the current sources, as showed in figure. 9.

To minimize the systematic error introduced by the voltage drop in the ground lines of the current-source transistors and take account of the increased device current in cryogenic temperature, metal lines with sufficient width from careful calculations based on precise simulation have been used. The maximum delay of the metal wire in chip is about 75ps and the clock tree is carefully built to ensure an acceptable clock skew.

V. Conclusion

In this paper, a 100MHz 12-bit DAC capable to operate under ultra-wide temperature (UWT) range from -180°C to +120°C and at ultra low temperature (ULT) of -230°C has been presented. In order to achieve temperature-independency, a bandgap reference with low temperature coefficient of 110.4ppm/°C over the UWT range is designed to provide different segmented current source cells with stable and accurate current. The cryogenic DAC was implemented in a 0.5um SiGe technology. The chip die area is 4.08×2.34 mm^2 and the total power consumption is about 105mW with a 3.3V power supply at ULT of -230°C. Should this paper be accepted, the measured chip performance will be available before final revision.

Acknowledgment

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