A Portable All-Digital Pulsewidth Control Loop for SOC Applications

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Abstract—**A cell-based all-digital PWCL is presented in this paper. To improve design effort as well as facilitate system-level integration, the new design can be developed in hardware description language (HDL) and implemented with standard-cell libraries, therefore, easily portable between technologies. In addition, a high-resolution architecture is designed to enhance pulsewidth precision. For different requirements of applications, the characteristic of scalable modulating range allows hardware decision in early stage. The proposed methodology has been proven at UMC 0.18um CMOS technology. When operated at 350 MHz, the pulse width acquisition ranges from 10% to 85% with 0.9% steps.**

I. INTRODUCTION

In CMOS circuit designs, great attentions must be paid to clock quality, including frequency, distribution, phase and duty cycle. Currently, phase-locked loop (PLL) or delay-locked loop (DLL) is widely utilized for clock circuitry. Precise duty cycles are often required to fit demands in modern high-speed and low-power circuit designs. Even though PLL and DLL can reach frequency multiplication and phase alignment, they cannot offer desired duty cycles of clock signal. Pulsewidth control loops (PWCLs) [1]-[4] can be used to overcome this problem. Figure 1 shows a conventional PWCL circuit.

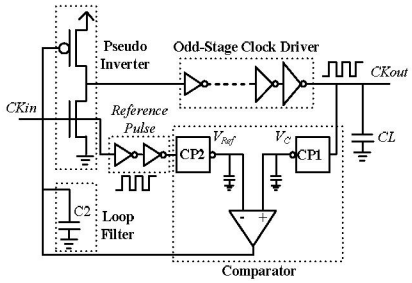

Figure 1. A typical PWCL circuit.

The PWCLs in [1][2] were proposed to precisely adjust the output duty cycle of the multistage driver. Most PWCLs [1]-[3] are realized by analog approaches at present. However, as discussions in [2] extensive circuit simulations are usually performed to determine loop gain and loop filter. Also, an analog PWCL usually takes a long transient time to converge. Recently, a robust all-digital PWCL (ADPWCL) [4] has been introduced, where the architecture is constructed with digital circuits. However, specific circuit blocks and custom layout of the ADPWCL are redesigned for each new technology. Thus, efforts at physical design level remain unsolved.

In order to provide fast turnaround time, a PWCL is desirable to be globally flexible to fit various system specifications, such as acquisition range, technology changes, and integrated simulations, etc. Thus, a cell-based all-digital solution for PWCL with high-resolution and scalable-acquisition-range is presented in this paper. The new ADPWCL can be described by Verilog HDL and implemented through synthesis and layout CAD tools. Based on scalable function blocks, it allows architecture decision in early stage. Also, due to cell-based feature, new ADPWCL can be incorporated into HDL-level simulation and system evaluation. A prototype design is realized at UMC 0.18um technology. When operated at 350 MHz, the ADPWCL gives modulation range from 10% to 85% with 0.9% acquisition steps and simulation RMS jitter of 25ps.

II. CELL-BASED ALL-DIGITAL PWCL ARCHITECTURE

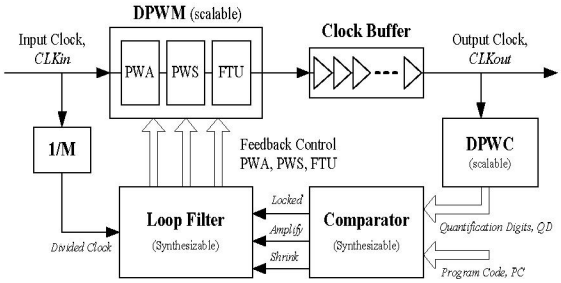

Figure 2. Proposed portable ADPWCL.

A block diagram of portable ADPWCL is shown in Figure 2. Overall system is decomposed into five main function blocks: 1) Clock Buffer providing suitable driving strengths for application circuits, 2) Digital Pulsewidth Converter (DPWC) cyclically converting the pulsewidth of CLKout into binary digits, 3) Comparator performing pulsewidth comparison and lock detection, 4) Loop Filter utilized to reduce the noise coming from the environment, and generate digital control codes of feedback control, and 5) Digital Pulsewidth Modulator (DPWM) responding for modulating pulsewidth.

Due to physical constrains of setup/hold time, the divider M is used to slow down target frequency as well as allocate timing for critical path of loop filter. Based on the control codes from loop filter, the DPWM gives the function of modulating pulsewidth with digital techniques. The feedback loop operates continuously until comparator enters locked state, namely the DPWC quantization digits (QD) match the external program code. The ADPWCL can generate desired pulsewidth for demands of applications.

A. Digital Pulse Width Converter (DPWC)

To measure the continuous clock pulsewidth in digital way, the design concept of time-to-digital converter [5] can be cited for purpose. A transformed architecture [4] has been introduced to convert pulsewidth into binary digits, as shown in figure 3. The incoming clock signal propagates through the buffer chain to become a series of delayed clock signals. The delayed clocks are utilized to trigger the DFFs successively, and measure the pulsewidth. The ratio of consecutive "1" and total word length represents the duty cycle. Thus, a continuous clock pulsewidth can be digitally quantized into n-bit word.

However, the long critical path of conventional DPWC is quite long and therefore limits operating frequency. While the propagated clocks are used for quantization, great deals of power dissipations can be contributed.

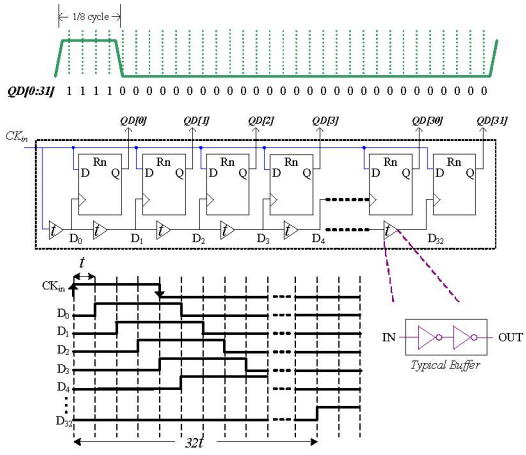

Figure 3. Conventional DPWC architecture.

Therefore, a modified DPWC is designed to solve the issues. The pulsewidth of clock decides duty cycle, and the pulsewidth conversion is processed between clock's rising and falling edges. Thus, the propagated clocks after falling edge could be expectably avoided. As common cell constructions, a buffer usually consists of two inverters. In order to save redundant propagated clocks, the first inverter is replaced by a NAND and the input clock is transplanted from DFF to delay cell as shown in figure 4.

The DPWC operation completes just in time after clock falling edge; therefore, the critical path is significantly reduced. Also, since the setup-time physical constrain of DFF is resolved, the dead zone, non-ideal conversion of narrow pulse, is reduced. Moreover, the new DPWC reduces power consumptions because redundant propagated clocks are now gated and saved within new delay cell.

To evaluate performances, a prototype 32-stage DPWC is realized at UMC 0.18um 1P6M CMOS technology. Compared with conventional design, the new DPWC improves operating frequency from 350 MHz to 1GHz. According to conversions of different duty cycle, power savings are listed in table I.

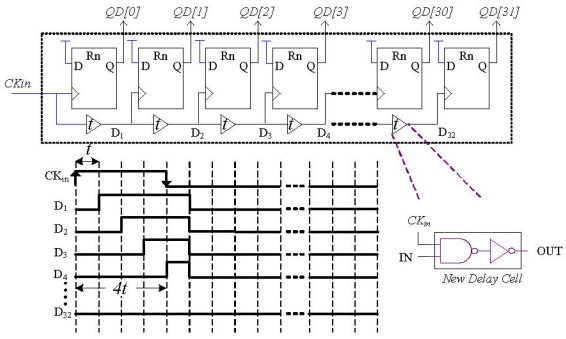

Figure 4. Modified DPWC architecture.

TABLE I. COMPARISIONS OF POWER COMSUMPTION

Duty Cycle (@ 350MHz)	75%	50%	25%
Typical (uW)	1602	1872	2016
Proposed (uW)	1058	774	503
Power Saving	34%	59%	75%

B. Digital Pulse Width Modulator (DPWM)

A pulsewidth modulator gives the function of reshaping clock waveform. Analog modulators [1]-[3] and digital one [4] have been utilized to modulate pulsewidth. However, specific-purpose circuit designs and custom layouts are still required. It still takes design efforts during technology migrations.

Therefore, we have three design goals in developing a portable clock modulator. First, the portable DPWM should be suitable for cell-based flow and capable for various cell-libraries. Second, scalability of acquisition range is desired for specification changes. Third, pulsewidth deviation should be carefully reduced to meet demands of advanced applications. Thus, our proposed DPWM is decomposed into scalable pulsewidth amplifier (PWA), pulsewidth shrinker (PWS) and fine-tune unit (FTU). The PWS reduces the pulsewidth according to digital control codes. On the contrary, the PWA amplifies the pulsewidth. FTU provides fine acquisition step of pulsewidth, as shown in figure 5.

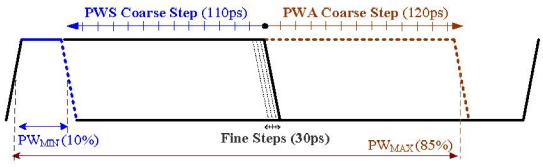

Figure 5. Pulsewidth acquisitions of DPWM.

To illustrate the detail circuit, the PWA consists of PWA stages as figure 6. Each of PWA stage provides 4 paths for signal propagation. Passing through the lowest path of each stage, the pulse width of clock is remained. If clock signal passes through an upper path, the pulsewidth is amplified, namely, the pulsewidth difference of adjacent paths in the same stage is equivalent to one buffer delay τ. Also, aimed at reducing pulsewidth, the PWS composed of PWS stages is depicted in figure 7. The cascaded pulsewidth increase PW_{diff} can be described in Eq. (1), where M, K are the total of PWA / PWS stages; A_{SEL}, and S_{SEL} represent the control codes, respectively.

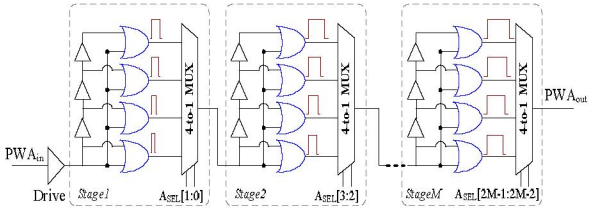

Figure 6. Scalable architecture of PWA.

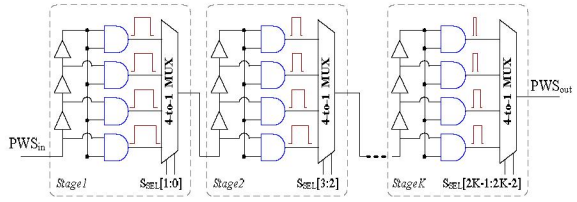

Figure 7. Scalable architecture of PWS.

$$PW_{diff} = \sum_{i=0}^{M-1}\left[\tau A_{SEL[2i]} + 2\tau A_{SEL[2i+1]}\right] - \sum_{j=0}^{K-1}\left[\tau S_{SEL[2j]} + 2\tau S_{SEL[2j+1]}\right]. \quad (1)$$

A new method of improving resolution is proposed for reducing pulsewidth deviations. The main idea is using the delay difference of propagation paths. As depicted in figure 8, a few buffer capacitances are added to slightly increase wire load. Higher capacitance load induces larger signal propagation delay and the output clock pulsewidth becomes wider. Dividing each PWA / PWS coarse step into fine steps, the FTU provides precise acquisition step r. Eq. (2) represents the pulsewidth increase of FTU. The equivalence acquisition range of DPWM is expressed in Eq. (3).

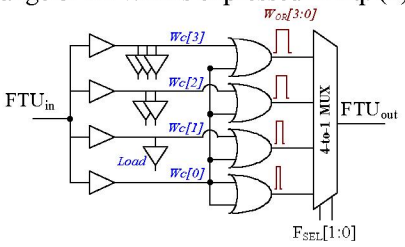

Figure 8. Architecture of Fine-Tune Unit.

$$FTU_{diff} = \left[r F_{SEL[0]} + 2r F_{SEL[1]}\right]. \quad (2)$$

$$DPWM_{out} = PW_{in} + PW_{diff} + FTU_{diff}. \quad (3)$$

In addition, it is essential to fix rising edge of each stage in DPWM during control code switches. The characteristic stabilizes phase-locking in PLL and allows further cooperation of PLL in later section.

A prototype modulator, consisting of five PWA/PWS stages and one FTU stage, provides (5*3+5*3)*3 acquisition steps. SPICE simulations of pulsewidth modulations in two cases (PWA, PWS) are given in figure 9. The robust and linear characteristic of DPWM architecture allows simple formulation of pulsewidth. In addition to coarse steps of hundred picoseconds, FTU provides fine resolution of 30ps as figure 10.

Compared with traditional designs [1]-[4], the proposed DPWM can be constructed with common logic cells, therefore easily transferred between cell-libraries. The consistence allows the architecture very suitable for extending acquisition range and enhancing resolution. The universal architecture gives design flexibility for application specification and hardware decision in early stage.

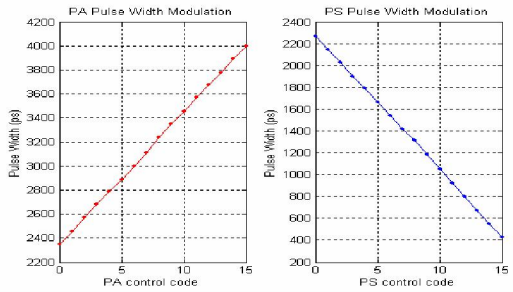

Figure 9. Post-layout Simulations of PWA and PWS.

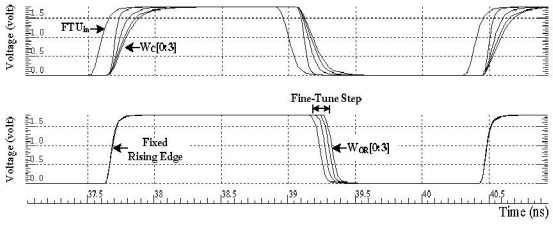

Figure 10. Simulations and characteristics of FTU.

III. System Application And Verification

An integration system is designed to verify the feasibility of the new ADPWCL. Figure 11 illustrates the on-chip communication (OCC) system configuration containing ADPLL, ADPWCL and on-chip serial transmission IPs. OCC have been actively studied to solve the scalability problem caused by popular bus-based SoC communication. As discussions in [6], serial communication is the key technology to overcome the wire complexity to make the implementation of OCC possible and practical. The main feature of the serial transmission circuits is the usage of true-single-phase pulse-triggered-based shift register, which requires a clock signal with narrow duty-cycle, 0.5ns below.

The ADPWCL dynamically controls and modulates pulsewidth while ADPLL performs operations of phase alignment and frequency synthesis. With the cooperation of ADPWCL and ADPLL, the output clock can fulfill the demands for desired clock of applications. The prototype integration design is verified and realized at UMC 0.18um 1P6M CMOS technology as figure 12.

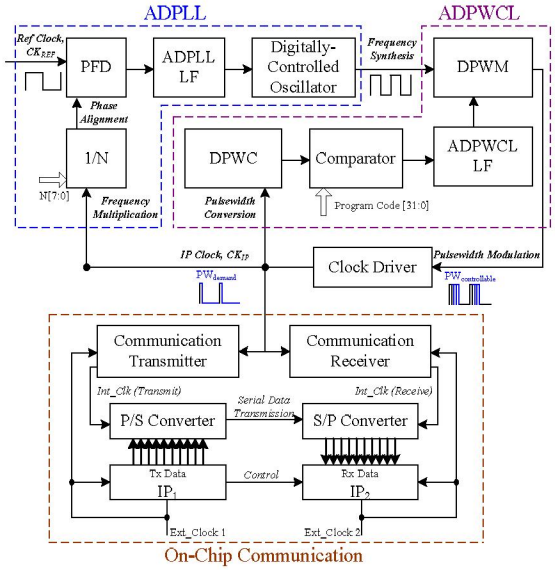

Figure 11. On-chip serial communication system.

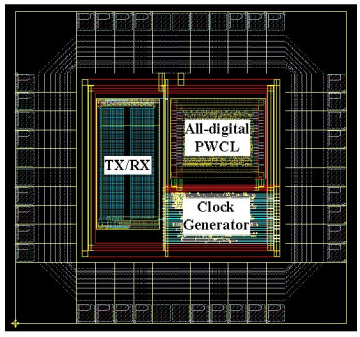

Figure 12. Chip layout of the OCC system.

Figure 13 shows the ADPWCL converges and enters into locked state according to different program codes at 350 MHz with SPICE simulations.

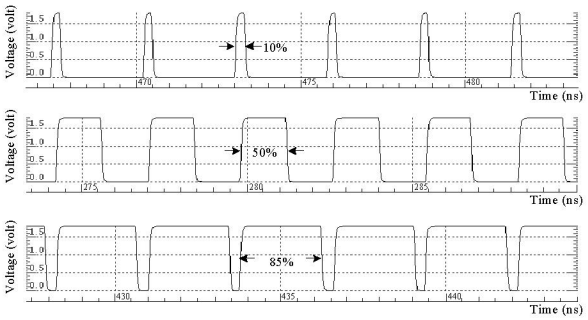

Figure 13. Output waveforms with programmable duty cycles at 350MHz.

IV. COMPARISIONS OF PWCL DESIGNS

Design	JSSC02 [2]	APASIC 02[3]	ISCAS05 [4]	Ours
Process	0.35um	0.18um	0.25um	0.18um
Architecture	Analog	Analog	All digital	All digital
Technique	Custom	Custom	Custom	Cell-Based
Programmable	N	Y	Y	Y
Portable	N	N	N	Y
Acquistion Range	50% (0.8GHz)	20~50% (0.4GHz)	20~80% (0.3GHz)	10~85% (0.35GHz)
Resolution	0.25 ns/V	5%	10%	0.9%

V. CONCLUSION

To meet the demands for fast turnaround time of SoC applications, a portable all-digital PWCL design is developed. The modified DPWC presents low-power and optimized-latency operations. A high-resolution DPWM is first proposed to enhance pulsewidth precision. With scalable circuit blocks and synthesizable loop controller, designers can develop ADPWCL in Verilog and save efforts significantly. When operated at 350MHz, the pulsewidth acquisition range is from 10% to 85% with 0.9 % steps. The ADPWCL design can be efficiently incorporated into modern SoC design flow due to its IP-based feature.

ACKNOWLEDGMENT

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