Design of a 130-nm CMOS Reconfigurable Cascade ΣΔ Modulator for GSM/UMTS/Bluetooth

Alonso Morgado, Rocío del Río and José M. de la Rosa

Instituto de Microelectrónica de Sevilla – IMSE-CNM (CSIC/University of Seville)
Edif. CICA-CNM, Avda. Reina Mercedes s/n, 41012- Sevilla, SPAIN
Phone: +34 95 5056666, Fax: +34 95 5056686, E-mail: {alonso|rocio|jrosa}@imse.cnm.es

Abstract **– This paper reports a 130-nm CMOS programmable cascade ΣΔ modulator for multistandard wireless terminals, covering three standards: GSM, Bluetooth and UMTS. The modulator is reconfigured at both architecture- and circuit-level in order to adapt its performance to the different standard specifications with optimized power consumption. The design of the building blocks is based upon a top-down CAD methodology that combines simulation and statistical optimization at different levels of the system hierarchy. Transistor-level simulations show correct operation for all standards, featuring 13-bit, 11.3-bit and 9-bit effective resolution within 200-kHz, 1-MHz and 4-MHz bandwidth, respectively.**[†1]

I. INTRODUCTION

The fourth generation (4G) of wireless communication systems will make the convergence of services provided by 2G/3G cellular phones, wireless area networks and short-range connectivity possible, giving rise to what has been called *always-best-connected systems* [1][2]. In such systems, one of the key blocks is the Analog-to-Digital Converter (ADC), because of the different sampling rates and resolutions required to handle the wide range of signals coming from each individual operation mode.

Sigma-Delta Modulators (ΣΔMs) are good candidates for the implementation of ADCs in highly integrated multistandard transceivers for the following reasons [3][4]:

- First, this type of ADCs trades analog accuracy by signal processing (oversampling and quantization noise shaping), thus making easier their integration in modern deep-submicron VLSI technologies, more suited to implement fast digital circuits than precise analog functions.
- Second, the robustness of ΣΔMs with respect to circuit imperfections make them suitable to include system- and subcircuit-level reconfiguration strategies, without significant performance degradation.

In this work, the transistor-level design of a 130-nm CMOS reconfigurable ΣΔM is presented. The circuit is intended to cope with GSM/Bluetooth/UMTS requirements in a direct-conversion receiver. An expandible cascade architecture is used to fulfill the required specifications with optimized power consumption. CADENCE-SPECTRE simulations are shown to demonstrate the correct operation of the circuit for the different standards.

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II. MODULATOR ARCHITECTURE

The modulator has been designed to fulfill the requirements of a multistandard direct-conversion receiver for GSM/Bluetooth/UMTS, considering a separate (switchable) RF section and a programmable baseband section [2]. The required modulator effective resolution was extracted from an iterative simulation-based procedure, realized in MATLAB/SIMULINK [5], considering the propagation of the different standard test signals through the receiver front-end. The outcome is shown in Table I, which lists the modulator specifications for the different standards covered in this paper [6].

An expandible cascade ΣΔM has been selected as the best suited architecture for those specifications [7]. This cascade topology comprises a 2nd-order first stage followed by 1st-order stages, and can be easily extended to build a ΣΔM of a generic order L by simply adjusting the number of 1st-order stages. In order to find out the best ΣΔM architecture that fulfills the specifications in Table I with the less power consumption, a large number of modulator topologies (univocally described by L, the oversampling ratio, M, and the number of bits of the last stage, B) has been compared in terms of their estimated power consumption, considering the impact of main circuit error mechanisms and technology parasitics. The selection procedure —described in [6]— led us to the expandible cascade Switched-Capacitor (SC) ΣΔM shown in Fig.1, which can be reconfigured, using the *GSM* and *SB* control signals (see Fig. 1) for each standard as follows:

- GSM: $L = 3$, $B = 1$ and $M = 100$
- Bluetooth: $L = 4$, $B = 1$ and $M = 20$
- UMTS: $L = 4$, $B = 2$ and $M = 10$

The former issues can be handled at circuit level, by reconfiguring the last stage of the expandible cascade to either 1-bit or 2-bit, and by dividing the master clock frequency (80MHz) by a factor 2. In addition, the same sampling capacitor (0.25pF) is used for all cases, thus eliminating the need for switchable capacitor arrays at the modulator front-end [6]. The integration capacitor of the fourth stage is though modified from 0.5pF in Bluetooth to 0.25pF in UMTS, in order to have a loop gain equal to one at this stage and make the implementation of the multi-bit quantizer easier.

The modulator-level specifications have been mapped onto

TABLE I. MODULATOR SPECIFICATIONS.

	GSM	Bluetooth	UMTS
Effective resolution	13bit	11bit	9bit
Bandwidth	200kHz	1MHz	4MHz

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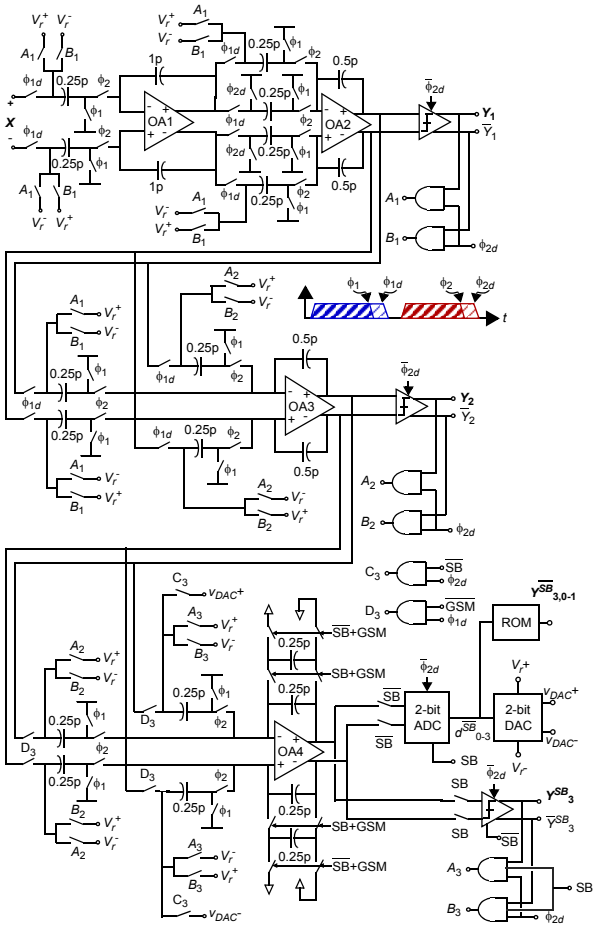


Figure 1. SC schematic of the reconfigurable cascade ΣΔM.

building-block specifications using statistical optimization for design parameter selection, and compiled equations (capturing non-ideal building block behaviour) for evaluation. This process is fine-tuned by behavioral simulation using SIMSIDES [8]. In this process, the worst cases for speed and for thermal noise are considered. The results of this sizing process are summarized in Table II. These specifications define the starting point for the electrical sizing of the building blocks, which is described in the next section.

TABLE II. HIGH-LEVEL SIZING OF THE MODULATOR.

Standard	Integs.	Amplifiers					Comparators	
		Input Noise (nV/√Hz)	DC gain (dB)	Eq. load (pF)	*GB* (MHz)	*SR* (V/μs)	Hyst. (mV)	Offset (mV)
GSM	#1	55.4	57.9	3.51	21.1	90.4	30mV	40mV
	#2	55.4	57.9	5.67	13.1	88.9		
	#3	85.0	58.1	5.67	8.6	36.1		
Bluetooth	#1	28.3	55.7	3.51	93.4	271.2	30mV	40mV
	#2	28.3	55.7	5.67	57.9	266.8		
	#3	30.0	54.0	5.67	49.6	108.5		
	#4	30.0	54.0	5.67	49.6	108.5		
UMTS	#1	15.8	50.0	3.53	193.9	628.6	30mV	40mV
	#2	15.8	50.0	5.70	120.2	621.6		
	#3	25.6	53.3	5.70	316.4	324.9		
	#4	25.6	53.3	16.15	111.7	173.7		

III. DESIGN OF THE BUILDING BLOCKS

A. Amplifiers

All amplifiers in the ΣΔM use a folded-cascode topology, since the required DC gains are not high, whereas the speed specifications are quite demanding for UMTS. The four amplifiers (OA1 to OA4 in Fig.1) share the same transistor sizes, with the only difference being a larger differential input pair in OA2 and OA3 in order to obtain a faster response. This, together with the use of a reconfigurable bias current for each amplifier and standard, allows to fulfill the specifications for the different operation modes. The differential input pair of the folded-cascode amplifiers uses pMOS transistors in all cases, what affects power consumption but enables to cancel their body effect in order to reduce the impact of substrate noise coupling [9]. The use of minimum-length transistors has been avoided in the input pair and in the current mirrors to limit $1/f$ noise and mismatching.

Table III summarizes the electrical parameters for each standard obtained after full sizing of the amplifiers, together with their corresponding bias currents. Results correspond to the worst-case value of each individual parameter obtained from a corner analysis, considering fast and slow device models, ±10% variation in the 3.3-V supply and temperatures in the range [–40°C, +85°C]. Note that the electrical results in Table III cover those obtained in the high-level sizing of the ΣΔM (Table II), with the main difference being the value of the equivalent integrator loads, which are finally considerably smaller than originally estimated.

Besides, special attention has been paid to the non-linearity of the amplifier DC gains. This effect is originated by the variation of the amplifier output impedance when its output voltage swings. This translates into a dependence of the open-loop DC gain on the output voltage, so that the DC gain reaches its maximum at the central point and decreases as the output approaches the rails. In order to accurately account for this non-linearity in behavioral simulations, we have resorted to a table look-up procedure using amplifier DC curves obtained by electrical simulation, whose data are included in behavioral simulations through a fast-convergence iterative procedure [10].

TABLE III. WORST-CASE RESULTS FOR THE AMPLIFIERS.

	GSM		Bluetooth			UMTS			
	OA1	OA2-OA3	OA1	OA4	OA2-OA3	OA1	OA4	OA2	OA3
DC gain (dB)	61.6	64.2	62.7		64.6	58.8		57.3	59.9
GBW (MHz)	244	143	183	105	130	326	102	251	232
Phase margin (°)	72	76	72	79	76	72	84	76	
Slew rate (V/μs)	253	102	144	80	85	474	141	352	289
Eq. cap. load (pF)	0.64	1.33	0.63	1.14	1.32	0.64	2.15	1.34	
Output swing (V)	±1.83	±1.92	±2.1		±2.01	±1.40		±1.02	±1.21
Input cap. (pF)	0.29	0.44	0.29		0.43	0.30		0.45	
Output cap. (fF)	31	38	29		39	31		39	24
Input eq. noise (nV/√Hz)	11.8	10.4	13.6		11.0	10.5		7.8	8.2
Bias current (μA)	28	24	16		20	52		80	66
Power cons. (mW)	2.32	1.99	1.32		1.65	4.31		6.63	5.47

B. Capacitors

All integrators in the SC ΣΔM use 0.25-pF sampling capacitors. This value has been fixed considering the trade-off between the modulator operation for GSM —in which thermal noise and mismatch[†2] can seriously limit the required resolution (13bit)— and that for UMTS —in which the required bandwidth (4MHz) in combination with large capacitive loads at the integrators can seriously impact power consumption.

Capacitors use metal-insulator-metal (MiM) structures available in the intended technology, which allows thin inter-metal oxide between the two top metal layers. They exhibit a good matching (0.097%), very small bottom-plate parasitics (4.6%) and a variation of the nominal capacitance of $\pm 15\%$. The fully-differential implementation of the reconfigurable modulator requires only 2×17 unit capacitors.

C. Switches

The design of the CMOS switches has been tackled with two main considerations in mind. First, the on-resistance heavily affects the integrator dynamic, slowing down its transient response [10]. Second, the switch on-resistance can be highly dependent on voltage. The sampling process with such a non-linear resistance causes dynamic distortion [11] at the ΣΔM front-end, the more evident the larger the signal frequency. Among the solutions to these problems, resorting to larger aspect ratios increases capacitive parasitics, whereas including clock-boosting [12] increases complexity and diminishes the robustness of the design.

According to the above considerations, resistances in the range of 260Ω can be tolerated in combination with the amplifier dynamics. In our process, such a value can be obtained using standard-threshold CMOS transmission gates, with no need for clock boosters. The sizes of the pMOS and nMOS devices — $23.49/0.34$ and $7.56/0.34$, respectively— have been selected to equalize their transconductances, keeping the resistance of the transmission gate as linear as possible.

D. Comparators

The resolution specifications for comparators in single-bit modulator stages are typically not very demanding, with tolerable offset and hysteresis around 40mV and 30mV, respectively. However, the maximum comparison time must be around a quarter of the clock period —3ns for the 80-MHz clock frequency corresponding to UMTS. For this reason, the latched comparator in Fig.2 has been adopted [13]. It includes a pre-amplifying stage —which attenuates the impact of common-mode interferences on the comparator and of kick-back noise on the integrator—, a CMOS regenerative stage and a SR latch. A small voltage imbalance at the comparator input is rail-to-rail regenerated during the positive-feedback comparison phase, using $\bar{\phi}_{2d}$ as the strobe signal in order to make the latch react before the integrator output changes at the beginning of ϕ_1. Monte Carlo and corner analysis have been used to characterize the comparator after full sizing. Table IV summarizes its worst-case performance for a 0.2-pF load, with data shown being the statistical results considering the mean plus 3 sigmas.

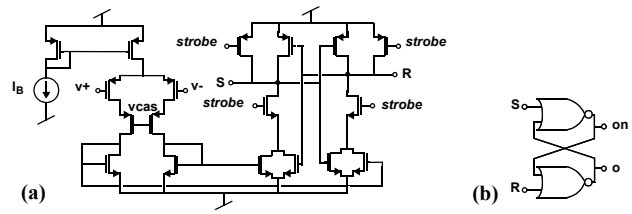


Figure 2. Comparator: (a) Pre-amplifier and latch, (b) SR flip-flop.

†2. Note that only the last-stage coefficients are reconfigurable. Therefore, the influence of reconfiguration on the mismatch performance is negligible in this design.

E. Multi-bit Quantizer

For the modulator operation in UMTS mode, a 2-bit quantizer is employed at the last stage to convert the 4th-integrator output into digital ($Y^{SB}_{3,0\text{-}1}$ in Fig.1) and then back to analog (v_{DAC}+, v_{DAC}-) to close the 3rd-stage loop. The 2-bit A/D/A converter is implemented with a flash ADC and a resistive-ladder DAC, as shown in Fig.3. Comparators in the ADC are similar to those used in the single-bit modulator stages (see Fig.2), but with an extra differential pair at the pre-amplifying stage in order to operate with fully-differential inputs. The thermometer code at the comparators outputs is translated into a 1-of-4 output code ($d_{0\text{-}3}$) that controls the generation of the analog output of the multi-bit quantizer. The resistive-ladder DAC consists of 6 segments of 400-Ω (unsalicided $p+$ poly) unit resistors connected between reference voltages $V_r^+ = 2.25\text{V}$ and $V_r^- = 1.05\text{V}$, thus providing a differential full scale of +1.2V with 500-μA current consumption.

F. Reconfigurable master bias current generator

The bias currents required for the ΣΔM operation are all internally generated from a single master current provided by an external resistor. This current is mirrored and properly scaled to bias the pre-amplifying stages of the comparators and the reference voltage generator. The value of the bias current for the four amplifiers OA1-OA4 is adapted from one standard to another according to the scheme illustrated in Fig.4.

TABLE IV. WORST-CASE RESULTS FOR THE COMPARATOR.

Hysteresis	0.6mV	Offset	35.3mV
Resolution time, LH	2.10ns	Resolution time, HL	2.11ns
Power consumption	0.50mW		

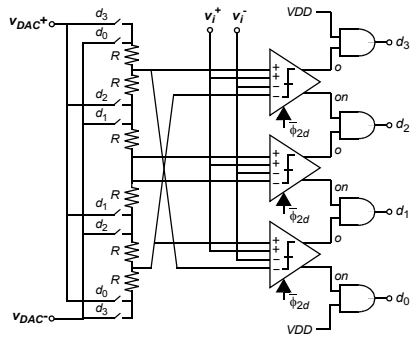
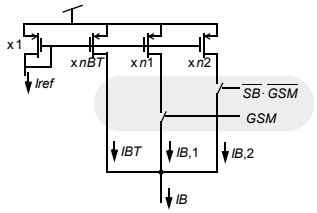


Figure 3. 2-bit quantizer at the modulator last stage (UMTS).



	GSM	BT	UMTS
(*GSM*, *SB*)	(1,X)	(0,1)	(0,0)
I_B	$I_{BT}+I_{B,1}$	I_{BT}	$I_{BT}+I_{B,1}+I_{B,2}$

Figure 4. Reconfiguration of the bias current of an amplifier.

IV. TRANSISTOR-LEVEL SIMULATION RESULTS

The performance of the ΣΔM has been evaluated through several transient electrical simulations at transistor level in CADENCE-SPECTRE. Worst-case thermal noise for each standard has been incorporated to simulations by including an input equivalent noise source, with noise sequences generated in MATLAB. Fig.5 shows the modulator output spectra for the different standards considering a $0.63\,V_{pd}$ input tone. Table V summarizes electrical results, which are in good agreement with those obtained by behavioral simulation. The power consumption for the analog core of the reconfigurable ΣΔM is approximately 7.8mW for GSM, 7.3mW for Bluetooth and 20.6mW for UMTS.

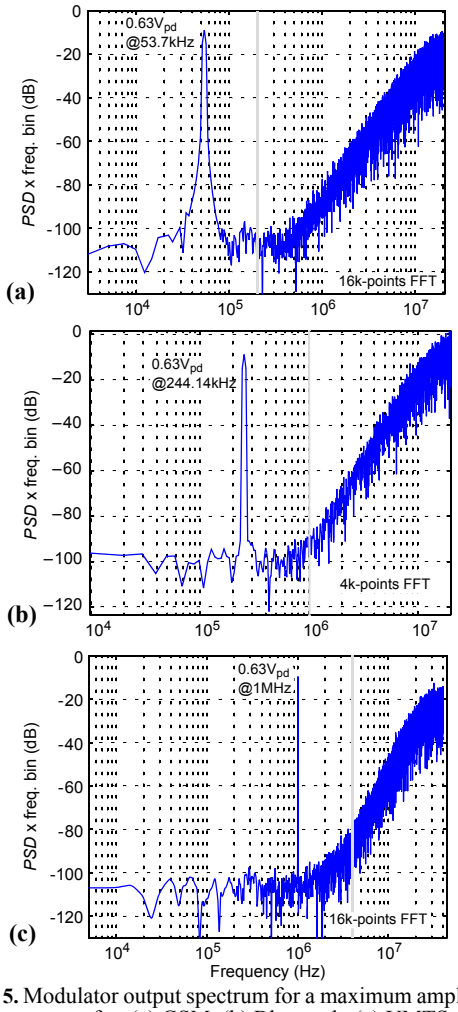


Figure 5. Modulator output spectrum for a maximum amplitude input tone for: (a) GSM, (b) Bluetooth, (c) UMTS.

TABLE V. MODULATOR SIMULATION RESULTS (0.63VPD INPUT TONE).

	GSM		Bluetooth		UMTS	
	Behav. Sim. (worst)[a]	Electr. Sim. (typ)[b]	Behav. Sim. (worst)[a]	Electr. Sim. (slow)[d]	Behav. Sim. (worst)[c]	Electr. Sim. (slow)[d]
SNDR	79.3dB	80.0dB	67.2dB	70dB	56.3dB	56.0dB
Resolution	12.9bit	13.0bit	10.9bit	11.3bit	9.1bit	9.0bit
Bandwidth	200kHz		1MHz		4MHz	

a. Worst-case for amplifier parameters (Table III) and maximum thermal noise.
b. Typ MOS models and worst-case equivalent thermal noise.
c. Worst-case for amplifier parameters (Table III) and max. cap values.
d. Slow MOS models, max. temperature and worst-case equivalent thermal noise.

CONCLUSIONS

The design of a 130-nm CMOS expandible cascade ΣΔM for GSM/Bluetooth/UMTS has been presented. The circuit is reconfigured at both architecture- and circuit-level in order to optimize the power consumption. Transistor-level SPECTRE simulations demonstrate a correct performance for all standards. In the time of writing this paper, the layout of the circuit – shown in Fig.6 – has been finished and sent for fabrication. Experimental results will be presented at the conference.

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REFERENCES

[1] V. Gazis *et al.*: "Toward a Generic Always Best Connected Capability in Integrated WLAN/UMTS Cellular Mobile Networks (and Beyond)". *IEEE Wireless Communications*, pp. 20-29, June 2005.

[2] A. Savla *et al.*: "A reconfigurable low IF-zero IF receiver architecture for multi-standard wide area wireless networks". *Proc. ICECS*, pp. 935-937, 2003.

[3] T. Burger *et al.*: "A 13.5mW 185-Msample/s ΔΣ Modulator for UMTS/GSM Dual-Standard IF Reception". *IEEE J. of Solid-State Circuits*, pp. 1868-1878, Dec. 2001.

[4] T.M.R. Miller *et al.*: "A Multibit Sigma-Delta ADC for Multimode Receivers". *IEEE J. of Solid-State Circuits*, pp. 475-482, March 2003.

[5] The MathWorks Inc.: "MATLAB®. The Language of Technical Computing. V.7.0 R.14", 2004.

[6] A. Morgado *et al.*: "Reconfiguration of Cascade Sigma-Delta Modulators for Multistandard GSM/Bluetooth/UMTS/WLAN Transceivers", *Proc. of the 2006 ISCAS*, pp. 1884-1887, May. 2005.

[7] F. Medeiro *et al.*: "High-Order Cascade Multi-bit ΣΔ Modulators". Chapter 9 at *CMOS Telecom Data Converters* (A. Rodríguez-Vázquez, F. Medeiro, and E. Janssens, Eds.). Kluwer Academic Publishers, 2003.

[8] J.Ruiz-Amaya *et al.*: "High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time ΣΔ Modulators Using SIMULINK-Based Time-Domain Behavioral Models". *IEEE Trans. on Circuits and Systems-I*, pp. 1795-1810, Sept. 2005.

[9] X. Aragonès *et al.*: *Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs*. Kluwer Academic Publishers, 1999.

[10] R. del Río *et al.*: "Highly Linear 2.5-V CMOS ΣΔ Modulator for ADSL+". *IEEE Trans. on Circuits and Systems-I*, pp. 47-62, Jan. 2004.

[11] W. Yu *et al.*: "Distortion Analysis of MOS Track-and-Hold Sampling Mixers Using Time-Varying Volterra Series". *IEEE Trans. on Circuits and Systems - II*, pp. 101-113, Feb. 1999.

[12] J.-T. Wu and K.-L. Chang: "MOS Charge Pumps for Low-Voltage Operation". *IEEE J. of Solid-State Circuits*, pp. 592-597, April 1998.

[13] Y.-T. Wang and B. Razavi: "An 8-Bit 150-MHz CMOS A/D Converter". *IEEE J. of Solid-State Circuits*, pp. 308-317, March 2000.

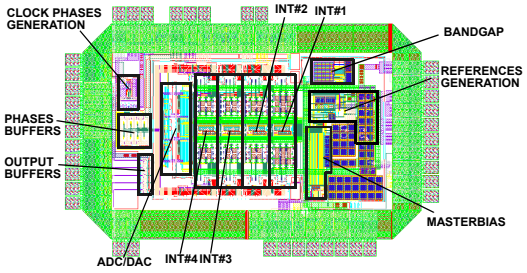

Figure 6. Layout of the modulator.