Limits to a Correct Operation in RTD-based Ternary Inverters

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***Abstract*— Multiple-valued Logic (MVL) circuits are one of the most attractive applications of the Monostable-to-Multistable transition Logic (MML), and they are on the basis of advanced circuits for communications. However, a proper design is not inherent to the usual MML circuit topologies. This paper analyses the case of an MML ternary inverter, and determines the relations that circuit representative parameters must verify to obtain a correct behaviour.**

I. Introduction

Resonant tunnelling devices are today considered the most mature type of quantum-effect devices, already operating at room temperature, and being promising candidates for future nanoscale integration. Resonant tunnelling diodes (RTDs) use to be implemented in III-V materials, and they exhibit a negative differential resistance (NDR) region in their current-voltage characteristics which can be exploited to significantly increase the functionality implemented by a single gate in comparison to MOS and bipolar technologies [1].

Figure 1*a* shows the *I-V* characteristic of an RTD enhancing key parameters for circuit design: peak current and voltage, I_p and V_p, and valley current and voltage, I_v and V_v. Three regions are defined according to Fig. 1*a*: two regions of positive (I and III) and one of negative (II) differential resistance. Circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) [2-4]. The basic MOBILE is a rising edge triggered current controlled gate which consists of two RTDs (the load and driver RTDs) connected in series and driven by a switching bias voltage (V_{bias}). When connected in series, RTDs provide multiple-peak structures in their *I-V* characteristics, which make it attractive for multiple-valued logic (MVL). MVL circuit applications are based on the Monostable-to-Multistable transition Logic (MML) [5], an extension of the binary MOBILE. Logic operation is based on the sequential switching of the RTDs connected in series, which is produced when the bias voltage rises to an appropriate value. Logic functionality is achieved by embedding an input stage (compound-semiconductor transistors, HEMT or HBT) which modifies, according the applied input signal, the peak current of some of the RTDs. MML circuits have been mainly applied in communication systems, where their high-speed performance is expected to be of the most importance for future commercial applications [6], [7].

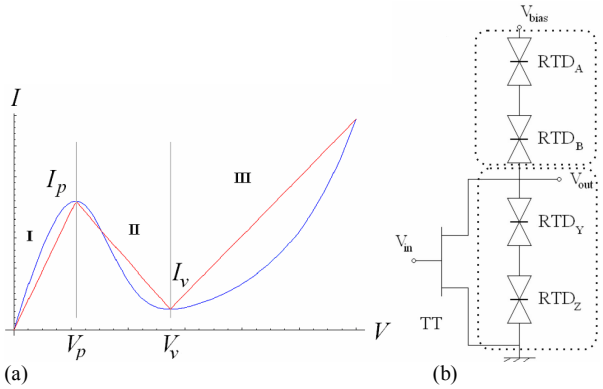


Figure 1. (a) *I-V* characteristic for a LOCOM RTD (blue) and its linear approach (red) and (b) typical structure of a MML ternary inverter.

In this paper DC operation of a key MML circuit, the ternary-valued inverter has been studied. Our analysis shows that a correct DC operation is not an inherent property to the circuit topology, being its careful design a main concern. To analytically study the problem we have resorted to piecewise linear descriptions for the RTD driving point characteristics, which allows obtaining relations between RTD and transistor parameters that ensure a correct behaviour of the structure. The paper is organized as follows: Section II deals with the operation principle of RTD-based ternary inverters. The importance of a correct sizing of the parameters of the structure as well as the relationships between them to ensure a proper behaviour are analyzed in Section III and Section IV respectively. Simulation results are shown in Section V. Finally, some conclusions are given.

II. Operation Principle

The piecewise linear model we have used for the RTDs has been derived from real RTDs fabricated in the LOCOM [8] fabrication process. Fig. 1*a* shows the piecewise linear model we are using. Peak and valley currents as well as peak and valley voltages have been selected from the LOCOM RTDs. For this RTD, V_p is $0.21V$, the peak current density 21 KA/cm^2, and the peak current ratio is about 6.25 at room temperature. The transistor is a depletion HFET with threshold voltage $-0.2V$.

Thus, current through the RTD is given by

$$\begin{cases} f\, m_I V & V \le V_p \\ f(m_{II}(V - V_v) + I_v) & V_p \le V \le V_v \\ f(m_{III}(V - V_v) + I_v) & V \ge V_v \end{cases} \qquad (1)$$

where V is the voltage applied to the RTD and f the area factor[1].

Figure 1*b* depicts a typical structure of a ternary inverter based on MML. Two negative differential resistance (NDR) devices can be identified: the driver and the load NDRs. The driver consists of a HFET (TT) and two series RTDs (RTD_Y and RTD_Z). The HFET provides the logic functionality as its input modulates the drain to source current of the transistor, and consequently the total current through the driver. For this structure, three feasible values of the V_{in} are considered, the high (V_{in}^H), medium (V_{in}^M) and low (V_{in}^L) voltages, associated with the logical *2*, *1* and *0* respectively. The load is made up of the series connection of RTD_A and RTD_B.

A correct evaluation of the input is determined by the relation between the peak currents of the driver and the load. If the input is at a high level, $V_{in} = V_{in}^H$, (ternary logic level "2"), the output must be at logic level "0". When logic level "1" ($V_{in}=V_{in}^M$) the output must also be "1". Finally, for the lowest level of the input (V_{in}^L), the output has to reach its highest value (level "2"). RTDs are supposed to have equal current densities so that peak currents are proportional to RTD areas. A proper operation is achieved if, additionally, the output node maintains its value for V_{bias} high even if the input changes. Thus, the multistability property is guaranteed.

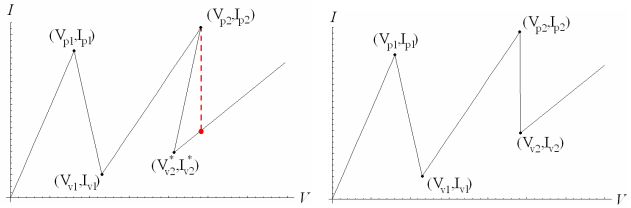
A first approach to the operation of the structure is given by the analysis of the switching sequence of the RTDs: the first to switch is that with the smallest area factor. This approach is not efficient since it is difficult to add the effect of the transistor. This problem can be efficiently approached by considering that both NDRs (the load, NDR_L, and the driver, NDR_D) are composed of two RTDs each one, and thus, they present a driving point characteristic with two peaks and two valleys. Based on simple geometrical considerations it is possible to analytically obtain the joint *I-V* characteristic for two series-connected RTDs. Two generic piecewise linear series-connected RTDs, RTD_1 and RTD_2, with area factors f_1 and f_2 respectively ($f_1>f_2$) are considered. The new joint *I-V* characteristic has two peak and two valley voltages (and currents) dependent on the values of f_1 and f_2. The first peak and the first valley are due to the RTD which area factor is smaller, whereas the second peak and valley are caused by the other RTD [9].

The joint *I-V* characteristic obtained is shown in Fig. 2*a*. It is easy to prove that for this representation, the second valley voltage is always below the second peak voltage. In order to handle well-defined functions, we have made $V_{v2}^{f_1,f_2} = V_{p2}^{f_1,f_2}$ (thus the second valley current has been changed as the red dotted line in Fig. 2*a* indicates), so that the resulting characteristic is depicted in Fig. 2*b*.

III. Correct Sizing of the Structure

DC operation of the ternary inverter is obtained by applying the Kirchoff Laws to the circuit in Fig. 1*b*, i.e., current through NDR_L must be equal to current through NDR_D. Thus,

[1] In this work all RTDs are supposed to have equal current densities, thus, peak and valley currents are proportional to *f*. An area factor of 1 corresponds to a RTD of area 10μm^2.



(a) (b)

Figure 2. (a) Real *I-V* characteristic of two series connected RTDs and (b) joint *I-V* representation after changing the position of the second peak voltage.

$$g_L[V_{bias} - V_{out}] = g_D[V_{out}] + I_{DS}[V_{in}, V_{out}] \qquad (2)$$

where $g[v]$ and $I_{DS}[V_{GS}, V_{DS}]$ represent the mathematical description of the driving point characteristic of two series connected linear RTDs ($g_D[v]$ for the driver and $g_L[v]$ for the load) and the transistor, respectively.

Two problems related to a correct sizing of the structure can be pointed out. The first one is the evaluation problem, which occurs when the modulation of the effective peak current through transistor TT is not enough for the output to invert the input V_{in}, for V_{bias} high. The second problem is the multistability lack, which occurs when a variation of the input forces a change of the output logic level. Next, both problems will be analyzed.

A. The evaluation problem

Due to the existence of two peaks in the *I-V* characteristic of both NDR_D and NDR_L, the operation of the ternary inverter shows two "transitions". The relation between the peak currents of the driver and the load during the evaluation phase will determine the final value of the output voltage. Once we know which RTD has the stronger influence in each peak and valley of the joint *I-V* characteristic, it is possible to make several suppositions about the order in which RTDs commute depending on the value of the input (usually RTD areas fulfil the relation $A_A>A_B>A_Y>A_Z$ [5]).

When $V_{in}=V_{in}^L$ the following relationship between the peak currents $I_{p1}^{f_Z,f_Y} < I_{p2}^{f_Z,f_Y} < I_{p1}^{f_B,f_A} < I_{p2}^{f_B,f_A}$ is verified. According to Section 3, both transitions are due to the RTDs belonging to NDR_D. In a similar way, when $V_{in}=V_{in}^H$, the peak currents verify $I_{p1}^{f_B,f_A} < I_{p2}^{f_B,f_A} < I_{p1}^{f_Z,f_Y} < I_{p2}^{f_Z,f_Y}$, that is, the first and the second transition are due to the RTDs of NDR_L (RTD_B and RTD_A). Finally, for $V_{in}=V_{in}^M$ two possibilities have been found to reach a 'medium' logical level of the output: if $I_{p1}^{f_Z,f_Y} < I_{p1}^{f_B,f_A} < I_{p2}^{f_Z,f_Y} < I_{p2}^{f_B,f_A}$, RTD_Z commutes before RTD_B, whereas if $I_{p1}^{f_B,f_A} < I_{p1}^{f_Z,f_Y} < I_{p2}^{f_B,f_A} < I_{p2}^{f_Z,f_Y}$, RTD_B does it firstly.

A very useful way of understanding how V_{out} evaluates when V_{bias} increases its value from 0 to V_{bias}^H for a fixed input value is a DC plot of the solutions to (2). Figures 3*a* and 3*b* depicts this plot in the V_{bias}-V_{out} plane for $V_{in}=V_{in}^L$ and $V_{in}=V_{in}^H$ respectively, where the red dashed line represents the real operation of the ternary inverter. Marks "1" and "2" point out the transitions due to switching RTD_Z and RTD_Y respectively and "F" the final value of V_{out} when $V_{bias}=V_{bias}^H$.

B. *The multistability dissapearance problem*

This problem comes from the disappearance of one (or more) of the stable states in the DC solution representation when V_{bias}=V_{bias}^{H}. Let us consider the disappearance of the highest output level when the input voltage increases its value to V_{in}=V_{in}^{H}. This malfunction appears when NDR_L is biased about its first peak voltage (RTD_B is in its peak and commutes, forcing a change in the output node), thus, V_{out} is approximately $V_{bias}^{H} - V_{p1}^{f_B,f_A}$. Figure 3*c* depicts the load curve for a properly-sized MML inverter, in which the five solutions found have been marked in red. Let us consider the case in which the input is fixed at its low value. A malfunction is found around $V_{out} \cong V_{p1}^{f_Z,f_Y}$ when V_{in}=V_{in}^{L}, which happens when RTD_Z reaches its peak voltage, increasing the value of the output node. In order to find solutions to Eq. (2) around $V_{out} \cong V_{p1}^{f_Y,f_Z}$ it is mandatory that the first peak current of NDR_D is above the current of NDR_L when it is biased with a voltage equal to $V_{bias}^{H} - V_{p1}^{f_Y,f_Z}$ (see Fig. 3*d*).

IV. Critical Dependencies

Once the mechanisms to analyze both malfunctions have been studied, the relationships between circuit parameters to guarantee a correct DC operation will be obtained.

A. *Evaluation constraints*

Let us begin with the evaluation for V_{in}=V_{in}^{L}. In this situation, the first transition is due to RTD_Z, thus we must ensure that the first peak current of the driver is less than the first peak current of the load. In this way, the RTD with smallest area of the driver (RTD_Z) always commutes before the smallest RTD of the load (RTD_B). The critical situation in which both the first peak current of NDR_D and NDR_L are equal is shown in Figures 4*a*. Thus, the first relation between parameters comes from:

$$f_Z I_p + FF \cdot I_{DS}\left[V_{in}^{L}, V_{p1}(f_Z,f_Y)\right] < f_B I_p \tag{3}$$

According to the previous Section, RTD_Y is the second RTD to commute, so that second peak current of the driver must be less than the first peak current of the load (which is originated by the smallest RTD of the load, that is, RTD_B). The limit case in which the first peak current of NDR_L coincides with the second peak current of NDR_D is depicted in Fig. 4*b*. According to this, a new expression for a minimum value of *FF* is derived,

$$f_Y I_p + FF \cdot I_{DS}\left[V_{in}^{L}, V_{p2}(f_Z,f_Y)\right] < f_B I_p \tag{4}$$

When V_{in}=V_{in}^{M}, the sequence of commutation of RTD_Z and RTD_B is determined by the relationship between the smallest peak currents of the driver and the load. When RTD_Z is the first to commute, two constraints can be derived concerning to the first and the second transition respectively,

$$f_Z I_p + FF \cdot I_{DS}\left[V_{in}^{M}, V_{p1}(f_Z,f_Y)\right] < f_B I_p \tag{5}$$

$$f_Y I_p + FF \cdot I_{DS}\left[V_{in}^{M}, V_{p2}(f_Z,f_Y)\right] > f_B I_p \tag{6}$$

On the other hand, when RTD_B commutes firstly,

$$f_Z I_p + FF \cdot I_{DS}\left[V_{in}^{M}, V_{p1}(f_Z,f_Y)\right] > f_B I_p \tag{7}$$

$$f_Z I_p + FF \cdot I_{DS}\left[V_{in}^{M}, V_{p1}(f_Z,f_Y)\right] < f_A I_p \tag{8}$$

For the highest value of the input voltage, V_{in}=V_{in}^{H}, the first transition happens when RTD_B commutes, thus,

$$f_Z I_p + FF \cdot I_{DS}\left[V_{in}^{H}, V_{p1}(f_Z,f_Y)\right] > f_B I_p \tag{9}$$

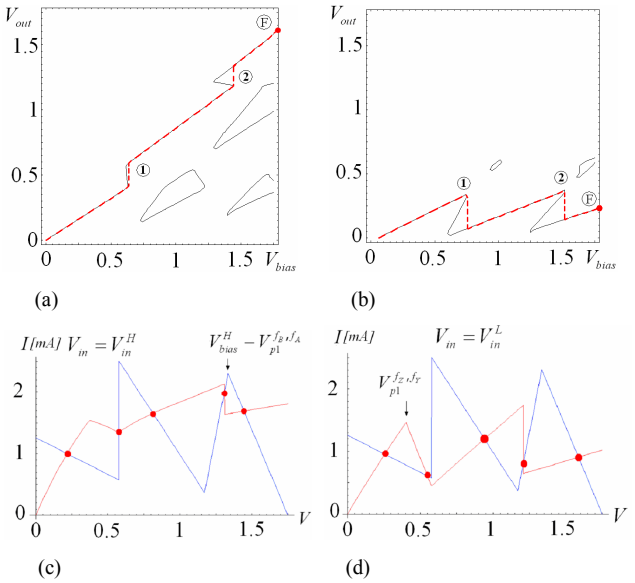


Figure 3. (a)-(b) V_{bias}-V_{out} plots pointing out the first ("1") and the second ("2") transition and the final value of V_{out} ("F") when V_{in}= V_{in}^{L}, V_{in} = V_{in}^{H}, respectively. Load curves marking the solutions to Eq. (2) in red, for (c) V_{in} = V_{in}^{H} and (d), V_{in} = V_{in}^{L}.

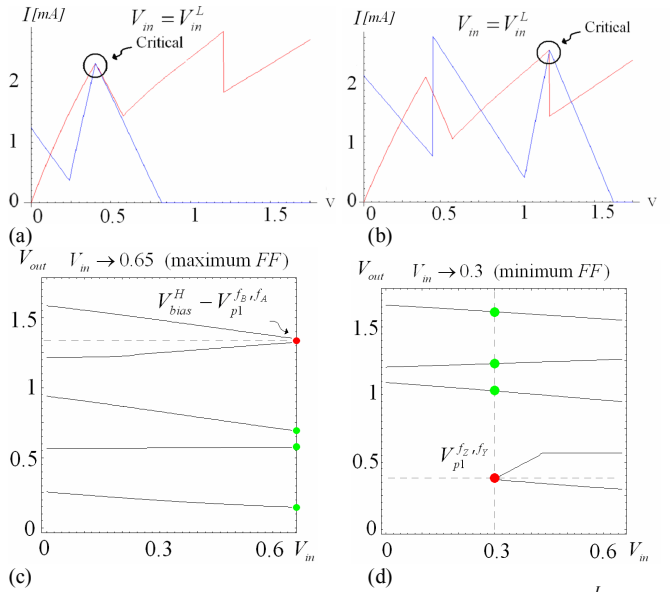


Figure 4. Critical situations for the evaluation problem when V_{in} = V_{in}^{L} for (a) first and (c) second transition. V_{in}-V_{out} plots pointing out the critical (in red) solutions to Eq. (2) when (c) V_{in} = V_{in}^{H}, (d) V_{in} = V_{in}^{L}.

Finally, to ensure that the next RTD to commute is RTD_A, the second peak current of the load has to be less than the first peak current of the driver,

$$f_Z I_p + FF \cdot I_{DS}\left[V_{in}^H, V_{p1}(f_Z, f_Y)\right] > f_A I_p \quad (10)$$

B. *Multistability constraints*

Two new restrictions to the feasible set of values of the circuit parameters can be derived through the analysis performed in Section III. Figure 4*c* depicts a V_{in}-V_{out} plot for V_{in} increasing from V_{in}^L to V_{in}^H, where the intersections with the left ordinate axis correspond to feasible solutions to Eq. (2) for the high value of the input. Upper point (in red) corresponds to a double solution to Eq. (2) and indicates the critical situation for which higher values of *FF* would entail an incorrect behaviour. Thus, an expression of a maximum value of *FF* is obtained,

$$g_D\left[V_{bias}^H - (V_{p1})_L\right] + FF \cdot I_{DS}\left[V_{in}^H, V_{bias}^H - V_{p1}(f_B, f_A)\right] < f_B I_p \quad (11)$$

When V_{in} decreases from V_{in}^H to V_{in}^L, the decision is taken around $V_{out} \cong V_{p1}^{f_Z, f_Y}$ (the red point in Fig. 4*d*) and must guarantee that the peak current of the driver is under the current of the load. Thus,

$$f_Z I_p + FF \cdot I_{DS}\left[V_{in}^L, V_{p1}(f_Z, f_Y)\right] > g_L\left[V_{bias}^H - V_{p1}(f_Z, f_Y)\right] \quad (12)$$

V. Simulation Results

In order to check our approach we have performed a comparison between our theorical approach and HSPICE simulation. Expressions (3-12) have been employed to analyze how the DC operation of a ternary inverter is modified when some key parameters are changed. HFET and typical parameters for the RTDs from the LOCOM technology have been used. Figure 5 shows the set of feasible values of *FF* (those which allow a correct evaluation and multistability preserving operation) obtained by varying Δ_1 (the difference between f_Z and f_Y and f_B and f_A), and $\Delta_2 = f_B - f_Y$, when f_Z=0.6. The first pair of plots depict the feasible pairs (Δ_2,*FF*) for different values of Δ_1 (0 and 0.15 in Fig. 5*a* and 0.08 in Fig. 5*b*). The green area corresponds to the region of feasible *FF* that has been derived theorically through (3-12). The black points represent the points obtained after performing HSPICE simulations. It can be observed the shrinking of the feasible region. For Δ_1>0.15 there are no inverters with a proper behaviour. A very close correspondence between both theoretical and simulation results can be also observed. In Figures 5*c* and 5*d* the effect of a variation of the peak voltage is analyzed. Feasible pairs (Δ_2,*FF*) for V_p=0.15 (Fig. 5*c*) and V_p=0.25 (Fig. 5*d*), show that the area of the correct operation region is increased when V_p does.

VI. Conclusions

A proper DC operation of MML circuits is not an inherent property to the circuit topology. Starting from a MML ternary inverter, two basic problems to size the inverter have been pointed: the evaluation fault and the multistability lack. To analytically study the problem, piecewise linear descriptions for the RTD driving point characteristics have been used. A procedure to calculate the relationships between circuit parameters in order to obtain correct DC operating regions has been derived.

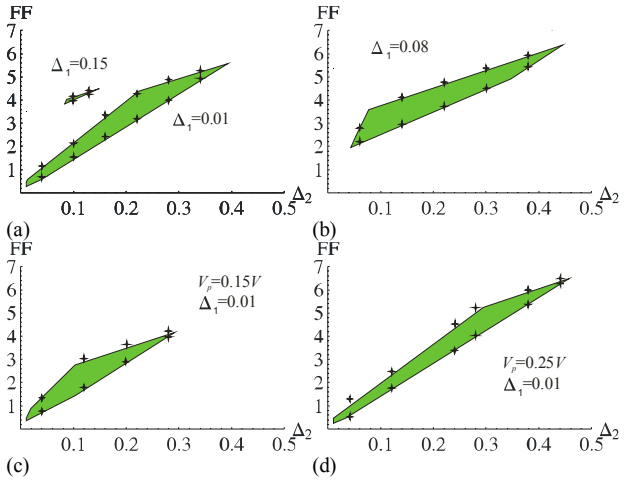


Figure 5. Set of feasible of values of *FF* vs $\Delta_2 = f_B - f_Y$ for $\Delta_1 = f_A - f_B = f_Y - f_Z$ = {0.01 and 0.15 (a), 0.08 (b) with f_Z=0.6}, marking in green the area derived through (3-12) and with the black points, the region obtained after performing HSPICE simulations with piecewise linear RTDs. (c)-(d) Region of correct DC after changing the value of the peak voltage to (c) V_p=0.15, (d) V_p=0.25.

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