OTA-C oscillator with low frequency variations for on-chip clock generation in serial LVDS-AER links

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***Abstract*— This paper presents the design and simulation of an OTA-C oscillator intended to be used as on-chip frequency reference. This reference will be part of the high speed clock generation circuit for Manchester serial LVDS-AER links. A Manchester LVDS receiver can adapt its operation in a limited range of frequencies, so the most important specification is the frequency stability over temperature and process variations. A novel design methodology is presented to design two oscillators in a 90nm technology using transistors with 2.5V supply voltage. Intensive simulations with temperature, process, supply voltage variations and mismatch effects were perfomed in order to analyze the validity of this approach, obtaining $\Delta f \approx 7\,\%$.**

I. Introduction

Computer capabilities for processing data have evolved at such high speed that the actual state of the art was unbelievable a few years ago. However, the sequential inspiration of the classic approach is not appropiate for certain applications (i.e. real-time vision processing). A possible solution to improve the processing efficiency is to emulate the human brain structure: a huge amount of computational units (neurons) with low processing capability, but massively interconnected between them. However, the physical interconnection of neurons in 2-D silicon systems is practically limited to a few neighbours.

AER (Address Event Representation) [1] is a neuromorphic protocol which allows the communication of a large array of neurons to another one using a reduced number of physical connections. Systems that use this protocol can be composed of a large amount of processing modules implemented in different chips that communicate between them using parallel buses [2]. Thus, one of the main drawbacks of present AER systems is poor scalability. A serial AER link has been proposed [3] to alliviate the connectivity constraints of the parallel solutions. The physical layer is based on the LVDS (Low Voltage Differential Signalling) standard.

In classic serial links the clock generation task is performed by a PLL (Phase Locked Loop) or DLL (Delay Locked Loop) that multiplies a reference provided by a quartz oscillator. This solution provides a very precise and low jitter clock. The receiver design proposed in [3] permits jitter and frequency deviations because it extracts the transmitted frequency from the received data edges. On the other hand, eliminating the external frequency reference would be desirable for simplifying the PCB design of AER systems. In this paper, the goal is to implement this time reference on-chip using an OTA-C (Operational transconductance amplifier-capacitor) oscillator designed to achieve low frequency drifts due to process and temperature variations. Compared to a conventional external crystal implementation, we have a less precise frequency ($\Delta f \approx 7\,\%$) and more jitter, but no off-chip complexity.

II. The ACM model

The design methodology is based on the ACM model [4], which provides single piece equations to describe the behaviour of MOS transistors in all regions of operation. Continuous weak to strong inversion models [4]-[5] exploit the inversion level concept, which is used to express the drain current as the difference between a forward I_F and reversed I_R components, such as $I_D = I_F - I_R = I_S\,(i_f - i_r)$. I_S is called specific current and can be written as:

$$I_S = \frac{1}{2}\frac{W}{L}\mu C'_{ox} n \phi_t^2 \tag{1}$$

where $\phi_t = KT/q$ is the thermal voltage and n is the slope factor. Terminal voltages are related to the inversion levels through a non-linear function $h(\cdot)$ as $V_P - V_S = \phi_t h\,(i_f)$ and $V_P - V_D = \phi_t h\,(i_r)$, where $V_p \approx (V_G - V_{T0})/n$ is the pinch-off voltage. For the ACM model this function is derived from physical principles and it can be expressed as:

$$h\,(i) = \sqrt{1+i} + ln\left(\sqrt{1+i} - 1\right) - 2 \tag{2}$$

III. The oscillator architecture

OTA-C oscillators can be designed as unstable second-order systems with some non-linear amplitude-control circuit. The most common implementations of an amplitude control circuit are a nonlinear resistor or an automatic gain control circuit. However, the non-linear characteristic of an OTA can be also used as an amplitude limiter [7]. For a transconductor with an input amplitude larger than its linear range, a third order Taylor-series expansion in terms of the input voltage can be done:

$$I_o \approx g_m V_{in}\left(1 - \left(\frac{V_{in}}{2v_L}\right)^2\right) \tag{3}$$

where g_m is the transconductance in the linear region and v_L is the linear range, which is defined as $v_L = \sqrt{3} n \phi_t$ in weak inversion and $v_L = \sqrt{2nI_{bias}/\beta}$ in strong inversion.

The architecture used, shown in Fig. 1, is composed of two linearized OTA's and a third non-linear OTA acting as an amplitude controller. The structure state-space equations respect to the reference voltage V_{ref} are:

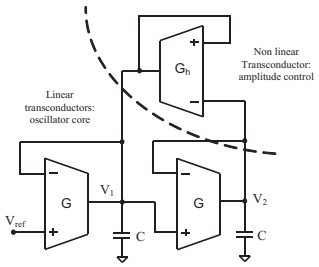

Fig. 1. Oscillator architecture

$$\begin{cases} C\frac{dV_1}{dt} = -GV_1 + G_h\left(V_1 - V_2\right)\left(1 - \left(\frac{V_1 - V_2}{2v_L}\right)^2\right) \\ C\frac{dV_2}{dt} = G\left(V_1 - V_2\right) \end{cases} \quad (4)$$

where G and G_h are the linearized and nonlinear OTA transconductance, respectively. By a change of variables, equation 4 can be reduced to a Van der Pol equation such as:

$$\frac{d^2y}{d\tau^2} - \epsilon\left(1 - y^2\right)\frac{dy}{dt} + y = 0 \quad (5)$$

where $\epsilon = G_h/G - 2$ is the Van der Pol parameter and

$$y = \frac{\sqrt{3G_h}}{2v_L\sqrt{G_h - 2G}}\left(V_1 - V_2\right) \quad (6)$$

The circuit has to ensure that $\epsilon > 0$ for oscillations start-up and, therefore, $G_h > 2G$. The Van der Pol equation has no closed-form solution, but it is a well-known and studied dynamic system. It is known that the steady state amplitude for variable y is 2 and the frequency and the amplitude of oscillation can be written as:

$$f = \frac{G}{2\pi C} = \frac{g_{mg}}{2\pi C} = \frac{g_{ms}}{2n\pi C} \quad (7)$$

$$Amp\left(V_2\right) = 4v_L\sqrt{\frac{\epsilon}{3\left(\epsilon + 2\right)}} \quad (8)$$

Two techniques were considered to control the OTA's input linear range: adding an attenuator at the OTA input or using the source degeneration technique. Both approaches cause a transconductance reduction in the OTA's, so the maximum achievable frequency is limited and the signal to noise ratio is degraded. In the first case, the input signal is attenuated to adapt the signal level to the OTA input linear range. Fig. 2 (a) shows the attenuator circuit [7] that uses a differential pair biased in strong inversion and two subthreshold diode-connected transistors. The attenuation factor is given by the ratio between the NMOS and the PMOS transistor transconductance [4]:

$$\alpha = \frac{(W/L)_n}{(W/L)_p}\frac{\sqrt{1 + i_{fn}} - 1}{\sqrt{1 + i_{fp}} - 1} \approx 2\frac{(W/L)_n}{(W/L)_p}\frac{\sqrt{i_{fn}}}{i_{fp}} \quad (9)$$

Fig. 2 (b) shows the source degeneration technique that was used to implement the second alternative. Transistors M_{lin} operate in ohmic region and behave as resistors, while M_1 and M_2 work in satuation. The resulting transconductance can be expressed as $g_m = g_{m1}/a$, where a is an attenuation factor that depends on geometrical parameters.

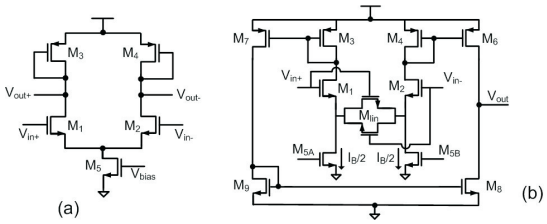

Fig. 2. (a) Fully differential attenuator (b) Linearized transconductor

IV. Design techniques

IV-A. Specific current extractor

The specific current in eq. (1) changes with process parameters and temperature. However, it can be proven that the ratio $g_m/\left(I_d\phi_t\right)$ depends only on i_f if the transistor is biased in saturation. That means that if the transistors operate with predetermined inversion levels, $g_m/\left(I_d\phi_t\right)$ is constant over temperature and process variations. To achieve this, we need to bias the transistors with scaled versions of the specific current.

The specific current extractor (adapted from [8]) shown in Fig. 3 was used for this purpose. The operation of this circuit is based on the properties of the tapped transistor, marked in the figure with dashed line. M_1 operates in ohmic region, M_2 in saturation and the pinch-off voltage of both transistors is the same because their gates are connected. Using these assumptions, it can be proven that the channel voltage for a tapped transistor is given by:

$$V_{ch1} = \phi_t\left(h\left(i_{f1}\right) - h\left(\frac{i_{f1}}{1 + S_2/S_1}\right)\right) \quad (10)$$

Eq. (10) has two asymptotes. They are the asymptotes of function $h\left(i\right)$ given by $ln\left(i/2\right)$ and $\sqrt{i}$ in weak $(i_f << 1)$ and strong inversion $(i_f >> 1)$, respectively:

$$V_{ch1} = \begin{cases} \phi_t ln\left(1 + \frac{S_2}{S_1}\right) & i_{f1} << 1 \\ \phi_t\sqrt{i_{f1}}\left(1 - \frac{1}{\sqrt{1 + S_2/S_1}}\right) & i_{f1} >> 1 \end{cases} \quad (11)$$

The basic current extractor is composed by two tapped transistors, one biased in weak inversion and the other one in strong inversion. The goal is to make the channel voltages of both tapped transistors equal using a high gain amplifier which creates a virtual ground between nodes V_{ch1} and V_{ch2}.

However, the channel voltage created by a single tapped transistor biased in weak inversion is very low and it is affected severely by threshold voltage mismatch. A way to increase this channel voltage while preserving reasonable area is to stack two tapped transisors, as it is shown in the left part of Fig. 3. If the current of both branches is the same, the resulting channel voltage is:

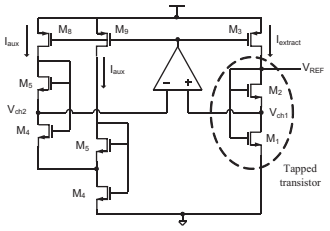

Fig. 3. Specific current extractor

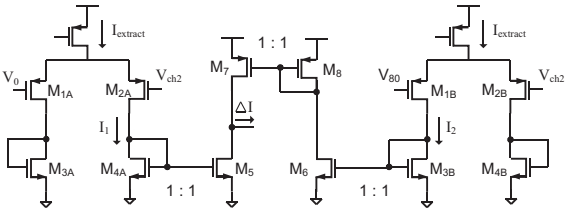

Fig. 4. Current interpolator for temperature compensation

$$V_{ch2} = \phi_t ln\left(\left(1+\frac{S_5}{S_4}\right)\left(1+2\frac{S_5}{S_4}\right)\right) \quad (12)$$

If voltages V_{ch1} and V_{ch2} are forced to be equal, the resulting inversion level can be written as:

$$i_f = \frac{1+S_2/S_1}{\left(\sqrt{1+S_2/S_1}-1\right)^2} ln^2\left(\left(1+\frac{S_5}{S_4}\right)\left(1+2\frac{S_5}{S_4}\right)\right) \quad (13)$$

which only depends on ratios between transistor sizes.

The accuracy of this circuit is limited by the mismatch between transistors. On the one hand, V_{ch1} will be slightly different from V_{ch2} due to the offset of the amplifier, so the input differential pair size has to be large and the bias current chosen properly. It is also important to ensure low mismatch between the two branches, specially in the branch operating in weak inversion. For this reason, the aspect ratios were implemented using the serial-parallel association of transistors [9]. A unitary transistor was defined as basic bulding block. A transistor N times wider was built by N unitary transistors connected in parallel. For a transistor M times longer, M transistors were stacked in series. Better mismatch performance is expected from these transistors due to the area increase.

IV-B. Capacitor implementation

On chip time references are imprecise because they are affected by the process variations, mismatch and temperature effects. To reduce these variations, the technique described in [9] to build accurate time references was implemented. MOS transistors are used as capacitors to cancel the effect of the oxide capacitance in the oscillations frequency. The main drawback of this technique is a poor linearity of the capacitor. For the present application this is not an important issue because we are not interested in generating a pure tone, but in low frequency variations. A MOS capacitor corresponds to a transistor with the drain and source terminals connected to ground and the gate acting as floating terminal. The total capacitance can be estimated as the sum of the total parasistic capacitances at the transistor gate.

$$C = C_{gs} + C_{gd} + C_{gb} = \frac{1}{n}\left(C_{gs} + C_{gd}\right) + \frac{n-1}{n}C'_{ox} \quad (14)$$

taking into account the ACM expressions for the MOS capacitors. A transistor with the drain and the source connected has $i_f = i_r = i_c$, so $C_{gs} = C_{gd}$ and eq. (14) can be simplified as:

$$C = A_c C'_{ox}\left(1 - \frac{1}{n\sqrt{1+i_c}}\right) \quad (15)$$

where A_c is the capacitor area and i_C its inversion level. Using this capacitance value, the oscillation frequency is given by:

$$f = \frac{\alpha\mu\phi_t\left(W/L\right)}{2\pi A_c}\frac{\sqrt{1+i_f}-1}{1-\frac{1}{n\sqrt{1+i_c}}} \quad (16)$$

where $\alpha < 1$ is the linear transconductor attenuation factor. Note that the only process parameter which appears in this expression is the mobility μ, because the inversion levels are properly set by the specific current extractor. To keep the CMOS capacitor inversion level controlled, the oscillator reference V_{ref} in Fig. 1 will be generated by the gate voltage of the tapped transistor used to extract the specific current in Fig. 3. Hence, the average gate voltage will be the same in both transistors, so the inversion factor will be similar.

IV-C. Temperature compensation

Eq. (16) shows that the oscillation frequency depends in μ, ϕ_t and the attenuation factor. These parameters are temperature dependent and make the frequency change from its nominal value. The idea to compensate the temperature effect is to add an extra current ΔI to the nominal bias current generated by the specific current extractor to correct the variations.

A temperature sensor is needed to generate ΔI. Eq. (12) shows that the channel voltage for a tapped transistor biased in weak inversion is proportional to the thermal voltage through a geometrical factor. Using this voltage, a current interpolator scheme can be adopted for the temperature compensation as shown in Fig. 4. In this circuit voltages V_0 and V_{80} represent the limits of the interpolation curves for 0^oC and 80^oC temperature. They should be constant over all operation conditions, so they would be generated from a bandgap circuit.

Analyzing the circuit of figure 4, the current correction can be expressed as:

$$\Delta I = \frac{\left(g_{m80}+g_{m0}\right)}{2}V_{ch2} - \frac{g_{m0}}{2}V_0 - \frac{g_{m80}}{2}V_{80} \quad (17)$$

where g_{m0} and g_{m80} are the transconductances of $M_{1A}-M_{2A}$ and $M_{1B}-M_{2B}$.

TABLE I

CORNER ANALYSIS

Corner [1]	Implementation I			Implementation II		
	f(KHz)	V_1(mV)	V_2(mV)	f(KHz)	V_1(mV)	V_2(mV)
TT/B0/C0/D0	226.1	126.1	95.4	135.6	126.7	92.8
FF/B2/C2/D1	226.1	111.8	84.4	135.5	124.6	91.3
SS/B1/C2/D2	223.2	115.7	87.5	133.8	129.1	94.8
SS/B2/C1/D2	222.4	152.7	115.9	134.4	128.0	93.6
FS/B1/C2/D1	224.6	114.6	86.7	138.8	109.4	80.1
FS/B2/C1/D2	224.5	149.8	113.7	139.8	96.7	70.4
SF/B1/C2/D1	224.8	114.1	86.1	130.9	143.4	105.3
SF/B2/C1/D2	225.0	149.2	112.9	131.6	147.6	108.0

Eq. (17) predicts a linear dependence between the temperature tracking voltage V_{ch2} and the current correction. The slope can be controlled with transconductances g_{m0} and g_{m80}. As the current corrections are small with respect to the bias current, a careful mismatch optimization is also required in this circuit by choosing large transistor sizes and a proper bias current. Another drawback is the transconductances variation with temperature. That distorts the linearity of the current-temperature curve, limiting the correction capability of the circuit. However, the temperature-frequency linearity is not a stringent requirement if the positive slope is maintained because the temperature-frequency curve is not linear either.

V. SIMULATION RESULTS

The proposed OTA-C oscillator was designed in the 90nm STMicroelectronics technology and simulated using the BSIM model provided by the manufacturer. All the circuits were implemented using 2.5V transistors. Standard 1-1.2V transistors were ruled out because of their high gate leakage and reduced dynamic range. Two versions of the oscillator were designed, one with a linearized transconductor (implementarion I) and the other with the attenuator (implementation II). The power consumption is 86.3 μW for the first version and 105.87 μW for the second one.

The circuit performance was tested on the technology corners and the results are listed in Table V. The relative error of the frequency with respect to the typical corner varied between -1.6 and 0.1 $\%$ (Imp I) and between -3.5 and 3.1 $\%$ (Imp II). In the corner analyses temperature effects and power supply variations are included besides process variations. If only the last effect is taken into account, the implementation I presents a relative error [-0.84,0.75]($\%$) and [-2.95,3.02]($\%$) for implementation II.

Fig. 5 shows a comparison between the temperature dependency of the frequency before and after the compensation. As a result of the compensation, the relative error in the oscillation frequency is [-0.62,0.09]($\%$) and [-0.66,0.29]($\%$) for implementation I and II, respectively. The frequency dependence on the supply voltage resulted in a [-0.18,0.18]($\%$) (Imp I) and [-0.44,0.44]($\%$) (Imp 2) of relative error. Finally, a Montecarlo mismatch analysis was performed with both architectures, obtaining $\sigma = 5{,}8KHz$ (Imp I) and $\sigma = 2{,}9KHz$ (Imp 2).

[1]FF/SS/FS/SF are the corners for the transistors, B refers to the value of resistors and capacitors, C to the temperature and D for the supply voltage. 0,1,2 denotes the typical, maximum and minimum cases, respectively.

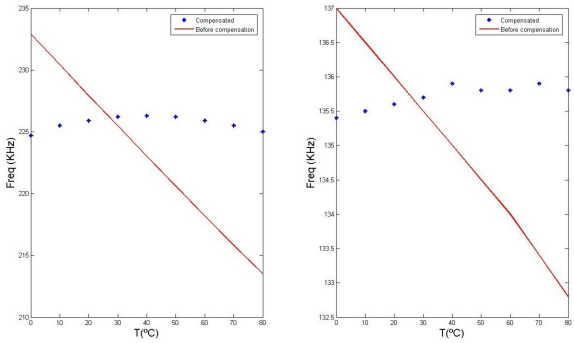

Fig. 5. Frequency-Temperature dependence with/without compensation

VI. CONCLUSION

An OTA-C oscillator design procedure for low frequency variations with temperature, process and supply voltage was described. Two oscillators were implementated in a 90nm technology using this approach. Intensive simulations verify that the oscillator has adequate frequency stability and thus can be used as a reference in serial AER links clock generation.

ACKNOWLEDGMENT

This work was supported by EU grant 216777 (NABAB), Spanish grant TEC2006-11730-C03-01 (SAMANTA II) and the local administration from Andalucía grant P06-TIC-01417 (Brain System). CZR was supported by a FPU grant.

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