On-chip Biased Voltage-Controlled Oscillator with Temperature Compensation of the Oscillation Amplitude for Robust I/Q Generation

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***Abstract*— In this work a CMOS 1.2V 5GHz low-power voltage-controlled oscillator (VCO) is proposed. It uses an on-chip biased LC-tank topology and introduces a temperature compensation technique which stabilizes the oscillation amplitude for a robust I/Q generation using a frequency divider-by-2. Compared to a standard design with constant bias, it reduces the oscillation variation by almost two orders of magnitude between 0ºC and 100ºC with negligible impact on the phase noise. Worst case estimations of the VCO phase noise after layout parasitic extraction are -110.1dBc/Hz and -126.6dBc/Hz at 1MHz and 5MHz offsets from the carrier, respectively. Its nominal current consumption is 198µA (plus 22.5µA for biasing) and it occupies 370x530µm^2.**

I. INTRODUCTION

The requirements of the VCOs in modern radio frequency (RF) applications are usually characterized at the system level by the phase noise and power consumption. In general it is assumed that the lower the phase noise is, the higher the power consumption. Although this trade-off becomes the dominant factor for defining the VCO total power in low phase-noise communication standards (e.g. GSM which needs –125.4dBc/Hz at 1MHz from the carrier), it is not strictly true for moderate and high phase-noise standards such as Bluetooth or ZigBee [1] (–114.4dBc/Hz and –72.0dBc/Hz at 1MHz, respectively). Actually, in these last cases with relaxed noise requirements, the trade-off between power consumption and the needed VCO oscillation amplitude (A_{osc}) becomes dominant, as the following equation shows,

$$Power \approx I_{tank} \cdot Vdd \quad ; \quad A_{osc} = I_{tank} \cdot R_{tank} \qquad (1)$$

where for a LC-VCO topology in the limited-current regime, I_{tank} can be particularized as the current through the tank, R_{tank} is its equivalent parallel resistance and Vdd is the power supply voltage.

In a traditional implementation the amplitude A_{osc}, and therefore, according to (1), the power consumption, are usually controlled by a constant current reference $I_{bias} = I_{tank}/M$. The particular value of I_{bias} must be determined according to the worst process and environmental operation conditions. Hence, this approach could lead to a non-optimal design in terms of power in the typical conditions.

Among the different contributions to the VCO performance degradation, the temperature is specially critical due to its great impact on the oscillation amplitude. In this context, an on-chip biased VCO with robust temperature compensation of the oscillation amplitude A_{osc} is presented in this paper. We will show how the use of a non-constant bias current with proper temperature dependence allows an important reduction of power consumption (when compared to the constant bias case). In addition, the on-chip reference generation overcomes the classical drawbacks associated to the external current reference generation at the printed-circuit board (PCB) level. Some of the on-chip generation advantages are: 1) it reduces the PCB cost, 2) it eliminates an additional pin for exciting the VCO, thus also reducing the package cost, and 3) it simplifies the blocking ladder design at the bias branch.

The proposed VCO with temperature compensation of the oscillation amplitude has been integrated in a 90nm RF CMOS process. The VCO has a centre frequency of 4.9GHz with a 10% tuning range from 4.65GHz to 5.15GHz. The prototype also includes a divider-by-2 (DIV2) as active load of the VCO for a robust generation of I/Q components in the 2.4GHz unlicensed ISM band. The VCO-DIV2 system fulfills the oscillator requirements for frequency synthesizers in the ZigBee standard. The included on-chip low-power bias current generator (BCG) exhibits a proportional-to-absolute temperature (PTAT) behavior which compensates the A_{osc} decrement when temperature increases. Its worst case power consumption and occupied die are just 16.3µW and 25x25µm^2, respectively. Compared to a standard design with constant bias, the proposed method reduces the A_{osc} variation up to two orders of magnitude with negligible impact on the phase noise. This

This work has been partially supported by the SR2- *Short Range Ratio* Catrene European Project and the Spanish TIC-927 Junta de Andalucía and TEC2007-68072 projects.

effect allows reducing the nominal power consumption a 14%, while maintaining a correct operation beyond 125ºC (for the classical constant current reference approach, the operation fails above 100ºC).

The paper is organized as follows. In Sect.II, the design of a CMOS 1.2V LC-VCO topology with classical constant current reference is described. This case of study illustrates the VCO problems for driving an active load, such as a frequency divider, for high temperatures. Section III presents the description of the self-biased current generator with emphasis on the PTAT behavior. It also introduces the selected implementation and its start-up circuit. Finally, the VCO with temperature compensated amplitude and the conclusions are shown in Sect.IV and Sect.V, respectively.

II. CLASSICAL LC-VCO WITH CONSTANT BIAS

In the previous section the closed relationship between power consumption and oscillation amplitude A_{osc} has been shown. In what follows, we will assume that the actual value of A_{osc} is the amplitude which guarantees a correct operation of the circuit at the output of the VCO. Notice that A_{osc} should be not confused with the minimum amplitude A_{osc}^{min} required to maintain a robust oscillation against process and environment variations, which can be estimated according to the effective transconductance and saturation voltage of the VCO active section (g_m, v_{dsat}), as follows,

$$A_{osc}^{min} \approx I_{tank}^{min} R_{tank} \approx (g_m v_{dsat})^{min} R_{tank} = (\alpha v_{dsat})^{min} \quad (2)$$

where the parameter α, usually $\alpha \in [2,3]$, comes from the oscillation condition [2], and defines the ratio between g_m and the tank conductance,

$$g_m = \frac{\alpha}{R_{tank}} \quad (3)$$

Actually, in most practical cases for moderate and high phase-noise standards, the actual oscillation amplitude A_{osc} could be significantly greater than A_{osc}^{min}. In other words, the current delivered to the tank, or equivalently the power consumption is fundamentally determined by the VCO load, instead of the oscillation condition given by (3). As an example, in our particular case of the study with a VCO followed by a frequency divider-by-2 (DIV2), the VCO power is basically defined by the particular divider realization instead of other target specifications, such phase noise or A_{osc}^{min}.

Figure 1 depicts a simplified schematic of the VCO and DIV2 system using a constant polarization current (I_{bias}). For an easy comparison with the implementation that will be shown in Sec. IV, a common design of these blocks has been considered through the paper. Here we focus on the VCO-DIV2 characteristics when is constantly biased. The VCO uses a LC-tank with complementary cross-coupled active negative resistances and PMOS current mirror (PCM).

Figure 2 shows the layout of the LC-VCO (approximately 370x530µm^2). This block has an average current consumption of 220µA (plus 25µA for the I_{bias}), a sensitivity of 250MHz/V and centre frequency of 4.9GHz. The inductor, which considers a symmetrical layout for better matching, has a

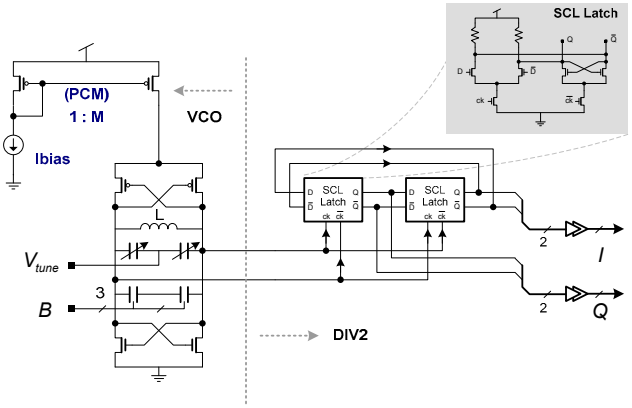

Figure 1. Simplified schematic of the LC-VCO with details of the active load in the case study (frequency divider-by-2).

nominal value of 2.15nH with a quality factor of 22@5GHz. PMOS varactors in accumulation mode and nominal capacitance of 42fF (Q = 53 @5GHz) give a fine tuning of around 100MHz. An extra MiM (metal-metal) capacitor array controlled by a 3-bit signal **B** provides an additional coarse tuning (up to 500MHz) for dealing with process and environment changes, as the post-layout simulation results after parasitic extraction in Fig. 3 show.

The frequency divider-by-2 (DIV2) considers two source-coupled (SCL) latches in a feedback configuration [3]. Each of the SCL latch drives in the worst case conditions 450µA from a dedicated pad power supply to reduce noise coupling to the VCO. The contribution of the frequency divider to total phase noise of the I/Q components (-110.1dBc/Hz and -126.6dBc/Hz at 1MHz and 5MH, respectively) can be neglected as it is fundamentally dominated by the VCO. After the SCL latches, two inverters reconstruct the logical levels, control the load matching and provide isolation. With a custom optimized design and dedicated layout, this topology has proven applica-

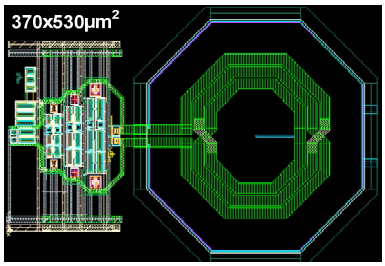

Figure 2. VCO layout with symmetrical inductor.

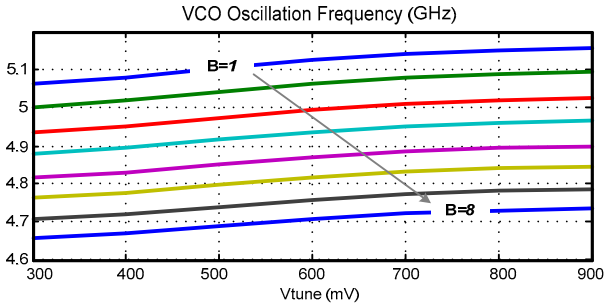

Figure 3. Fine and coarse tuning of the integrated VCO after layout parasitic extraction.

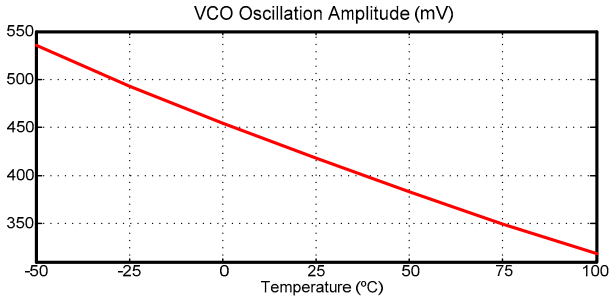

Figure 4. Temperature effect on the VCO oscillation amplitude A_{osc} after layout parasitic extraction.

bility for low-power design in current deep-submicrometer technologies [4]. However, the topology could be very sensitive to the VCO oscillation amplitude variations when temperature increases.

Figure 4 shows the temperature effect on the VCO oscillation amplitude A_{osc} in the typical conditions with layout parasitics. Notice that A_{osc} experiments a variation greater than 140mV from 0ºC to 100ºC, which could negatively affect to the functionality of the VCO load. Actually, in our particular case of study the operation of the DIV2 considering the worst process parameter (slow-pmos slow-nmos) fails above 100ºC due to the significant reduction of A_{osc}.

The theoretical justification for the A_{osc} behavior can be explained considering the temperature dependence of the tank resistance $R_{tank} = R_{tank}(T)$. Rewriting (1) for a fixed output bias current $I_{bias} = I_{tank}/M$, it is obtained,

$$A_{osc}(T) = I_{tank} \cdot R_{tank}(T) \tag{4}$$

where $R_{tank}(T)$ can be particularized for the considered LC-VCO topology, in the form [2],

$$R_{tank}(T) = 2 \cdot \left(R_{active}(T) \;//\; R_{var} \;//\; R_{MiM} \right) \;//\; R_{ind} \tag{5}$$

as a function of the effective resistances of: active cross-coupled pairs (R_{active}), varactors (R_{var}), MiM capacitor array (R_{MiM}) and inductor (R_{ind}). In this expression, the dominant contribution in terms of temperature comes from the active section $R_{active}(T)$. This term experiments a negative PTAT (NTAT) behavior (directly translated to A_{osc}) due to the conductance increment at high temperatures as more free charge carriers are available in a semiconductor [5].

III. On-Chip PTAT Current Reference

The principle of the proposed temperature compensation for the oscillation amplitude A_{osc} is quite simple. It considers an on-chip PTAT current reference generator (CRG) which corrects the $R_{tank}(T)$ dependence on temperature due to active section contribution,

$$A_{osc} = M \cdot I_{bias}^{NTAP}(T) \cdot R_{tank}^{PTAP}(T) \;\approx\; \text{constant} \tag{6}$$

The selected CRG scheme (which substitutes the I_{bias} in Fig.1) is based on the traditional self-biased current reference depicted in Fig.5a. This topology generates a nominal current which is approximately defined by the transistors aspect ratios and the resistor R. In order to achieve the wanted PTAT response, the coupled transistors $M_{1\text{-}2}$ can be polarized in weak-inversion [6]-[8]. Actually, taking into account that,

$$V_{GS2} = V_{GS1} + I_{out} \cdot R \tag{7}$$

and that the transistor current expression in weak inversion for a given geometric aspect (W/L) and current density I_o is,

$$I_D = \frac{W}{L} \cdot I_o \cdot e^{-V_{GS}/\phi_T} \quad ; \quad \phi_T = \kappa \cdot T \tag{8}$$

the output current (I_{out}) is obtained,

$$I_{out} = T/R \cdot \left(\kappa \cdot \ln(JK) \right) \tag{9}$$

where J is the current mirror factor, K is the transistor $M_{1\text{-}2}$ aspect ratio and κ is a technological constant. Obviously, the final dependence of I_{out} on the temperature T should consider the particular implementation of the resistor R, specially in a full on-chip realization. Taking into account this contribution the wanted PTAT behavior can be easily achieved with a proper circuit scaling.

Fig.5b shows the final CRG implementation with PTAT response (see simulation of Fig.6 for details). In this architecture the resistor R is constructed by an active device M_3. This transistor is polarized in the ohmic region thanks to the series connection with M_4 [6]. The CRG also considers: a) a simple start-up circuit to guarantee that the generator has the correct operation mode, b) an output programmable mirror which provides current selection flexibility, and c) an enable/disable circuit (omitted in the figure for simplicity) for power down the VCO. The total area and worst case power consumption of the generator core (excluding the output mirror) are 25x25μm^2

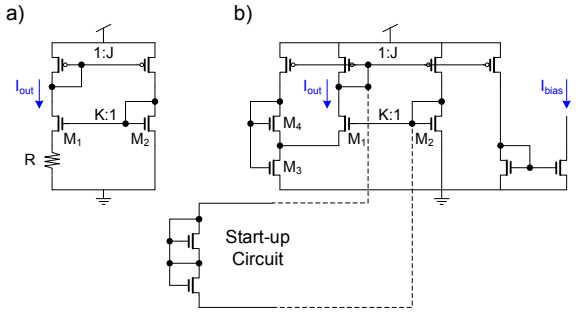

Figure 5. a) Traditional self-biased current reference; b) CRG generator with active internal resistance.

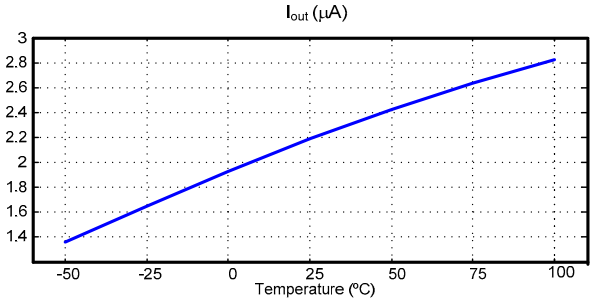

Figure 6. Simulation results of CRG showing the PTAT response of the output current I_{out}.

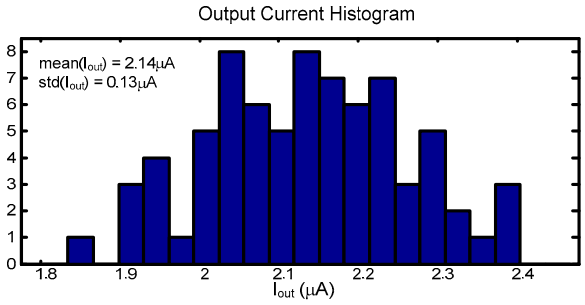

Figure 7. Output current histogram evaluated from a Monte-Carlo simulation with 100 runs.

and 16.3µW (for a 1.2V voltage supply), respectively. The reference current has a nominal value of 2.14µA with a standard deviation of 0.13µA as the Monte-Carlo simulations of Fig.7 shows (# runs = 100).

IV. Proposed VCO Implementation with Temperature Compensation of the Oscillation Amplitude

In this section the post-layout simulations for a temperature stabilized VCO-DIV2-CRG demonstrator are described. The prototype, which has been already fabricated in the TSMC CMOS 90nm RF process[1], will be one of the main building blocks of a transceiver for domestic use compliant with the ZigBee standard. The target temperature range for this application is from 0ºC to 100ºC.

Figure 8 shows a comparison between the proposed and the classical constant biased VCOs. Two different designs with temperature compensation are considered. The dashed curve corresponds to an implementation with 10% power reduction and almost complete cancellation of the oscillation amplitude dependence on temperature. This design reduces the of A_{osc} variation by almost two orders of magnitude between 0ºC and 100ºC (from 140mV to less than 5mV, respectively). In the second case of study, a VCO with PTAT amplitude behavior is considered to improve the DIV2 response at high temperatures. This effect allows reducing the nominal power consumption a 14%, while maintaining a correct operation beyond 120ºC (for the classical constant current reference approach, the operation fails above 100ºC). In both cases, the

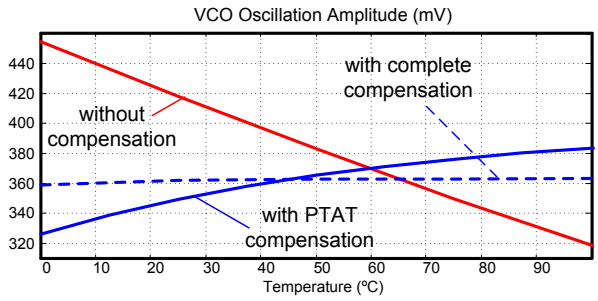

Figure 8. Comparison between the classical constant biased VCO and the proposed temperature compensation designs.

[1] The chip has been recently received and hopefully we will start obtaining experimental results by the end of the month.

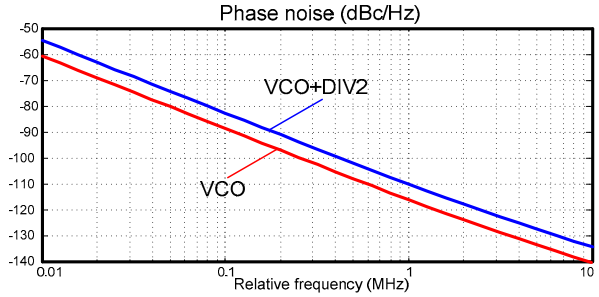

Figure 9. Phase noise of the VCO with and without the frequency divider (DIV2) after layout parasitic extraction.

CRG has negligible impact on phase noise (see Fig.9). The final layout is depicted in Fig. 10. The total core area including decoupling capacitors and testing buffers is 860x370µm^2.

V. Conclusions

In this work a fully integrated 1.2V 5GHz VCO with temperature stabilization of the oscillation amplitude has been implemented in a 90nm CMOS process. The chip uses a low-power compact PTAT current cell which compensates the tank resistance temperature variations. The approach improves the oscillator robustness at high temperature allowing a significant reduction of the nominal power consumption.

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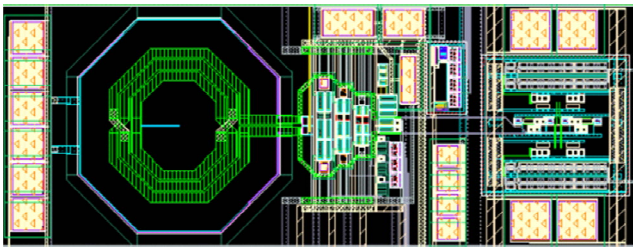

Figure 10. Chip demonstrator layout.