Low power 2.4 GHz quadrature generation for Body Area Network applications

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Abstract— This paper presents two implentations of low-power quadrature generation for the new Bluetooth low energy standard in the 2.4 GHz ISM band. Both implementation have been designed in a 90 nm CMOS technology for a 1 V supply voltage and post-layout simulation results are presented. The first implementation is a quadrature voltage controlled oscillator (QVCO) with 180 μW power consumption and a phase noise of -112.7 dBc/Hz @1MHz. It employs a new technique to reduce the influence of magnetic coupling between the two spiral inductors. The second implementation employs a VCO running at twice the frequency with a subsequent divide-by-2 stage. Its total power consumption is 320 μW and the phase noise at the quadrature outputs is -115.7 dBc/Hz @1MHz.

I. INTRODUCTION

Body area networks (BAN) based on miniature wireless sensors are expected to allow for a lot of new applications of wireless communication. They range from entertainment and automation to health care or human interface devices. In many of these applications, the need for ultra-low power consumption is prioritary since network nodes are supplied by small batteries or even rely on autonoumus energy scavenging techniques.

In order to cope with this operation conditions, the Bluetooth consortium has announced a low energy (LE) enhancement with relaxed radio specifications for the sensor nodes [1]. The increased channel spacing together with the reduced blocking requirements as compared to the core version of the standard, now allow for frequency synthesizers with much lower power consumptions. This is particularly important as the synthesizer has to be frequently turned on to detect and receive commands.

The power consumption of the frequency synthesizer is usually dominated by the voltage controlled oscillator (VCO) and the quadrature generation. Therefore, it is necessary to find the most power efficient solution both on circuit and on architecture levels. In this paper we first analyze the available oscillator topologies in section II and quadrature generation architectures in section III with respect to their power consumption. Then we present the implementation of two promising architectures for quadrature generation in section IV. In one of them, a new technique to reduce the effect of magnetic coupling between the inductors of two oscillator cores is described in detail. Section V presents post-layout simulation results and some concluding remarks are given in section VI.
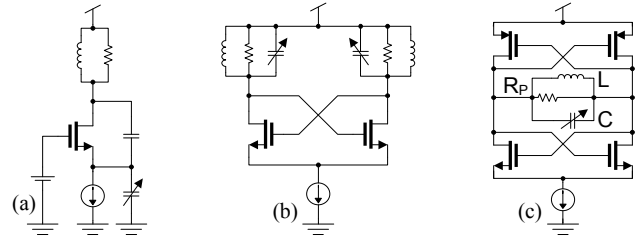

Fig. 1. Basic LC oscillators: (a) Colpitts LC VCO, (b) cross-coupled LC VCO, (c) current-reuse cross-coupled LC VCO

II. LOW POWER VCO TOPOLOGIES

The tradeoff between power consumption, occupied area and oscillator performance is the main design challenge for VCOs. The performance requirements of Bluetooth LE can be derived from the adjacent channel blocking capabilities. The resulting phase noise limit at a 2.5 MHz offset is approximately -105 to -110 dBc/Hz depending on the receiver implementation.

Thanks to the advances in speed of deep submicron digital CMOS technologies, simple ring oscillators may be used at frequencies in the GHz range. Moreover, a recent work has shown that phase noise requirements of wireless communication standards can be met using this very area efficient solution [2]. However, such ring oscillator topologies consume still more than 10 mW and are therefore not suitable for low power applications.

More power efficient oscillators can be designed using integrated spiral inductors. The two basic topologies are the Colpitts [Fig. 1(a)] and the cross-coupled LC oscillator [Fig. 1(b)]. The former has been shown to have superior phase noise performance because the noise current is injected when the sensitivity to noise is low [3]. However, the required transconductance to sustain oscillations in the Colpitts oscillator is larger compared to the cross-coupled structure.

Since power consumption is our main concern we will use the cross-coupled LC VCO together with current-reuse techniques as shown in Fig. 1(c). In this case the same bias current is used for a PMOS pair and an NMOS pair. Now, both pairs contribute their transconductance to cancel out the tank losses.

In order to minimize the required transconductance and, thereafter, power consumption, the losses of the LC tank must be reduce as much as possible. Usually tank losses are

dominated by the integrated inductor and can be approximated with

$$\frac{1}{R_P} \approx \frac{Q_L}{\omega_0 L(Q_L^2 + 1)} \tag{1}$$

where Q_L is the inductors quality factor at the oscillating frequency ω_0 [4]. This implies that apart from a high quality factor also a large inductance is needed. However, the inductance can only be increased until the parasitic capacitance precludes resonance at our design frequency. Bearing in mind this limitation we will select our inductor by searching for a minimum in (1).

III. ARCHITECTURES FOR QUADRATURE GENERATION

In order to demodulate the GFSK signals specified by Bluetooth LE, quadrature Local Oscillations (LO) have to be generated. Quadrature may be obtained by combining a VCO running at twice the desired frequency with a divide-by-2 circuit (VCO+DIV2), using a quadrature VCO with two coupled cores (QVCO) or by employing a passive RC-CR network. The latter option will not be considered in the following as it suffers from excessive power consumption required for buffering and cancellation of amplitude mismatches.

The most common approach is the VCO+DIV2 due to its area efficiency and simplicity. It requires only one VCO core and thus only one inductor. However, its operation at twice the frequency requires a smaller inductance which leads to an increased power consumption. Moreover, the divide-by-2 circuit usually consumes a significant amount of power due to its very high input frequency.

Therefore, the QVCO approach is generally regarded as the option that consumes less power [5], [6]. A divider-by-2 block is not needed and the lower oscillating frequency allows larger inductances, thus favoring tank losses reduction acording to (1). The main drawback is a larger area occupation because of the two required inductors. Another problem of the QVCO solution is the phase error due to magnetic coupling between the two inductors [7]. However, since this phase error is deterministic it may be reduced through a decoupling network as implemented in our solution presented in section IV.

IV. IMPLEMENTATION

The two quadrature generation techniques discussed in section III have been implemented using a 90nm CMOS process[1]. Both implementation have been taped out for fabrication and their delivery is expected in December 2009.

A. QVCO

The quadrature VCO, shown in Fig. 2, is implemented as two current-reuse VCOs coupled to each other by means of coupling transistors. The two 7-turn symmetrical inductors (L=13.3 nH, Q_L=12 @2.45 GHz) have been selected by minimizing tank losses according to (1). Consequently, a very low bias current of 90 μA per core is sufficient to obtain a single-ended amplitude of $\approx$150 mV. Coarse tuning to

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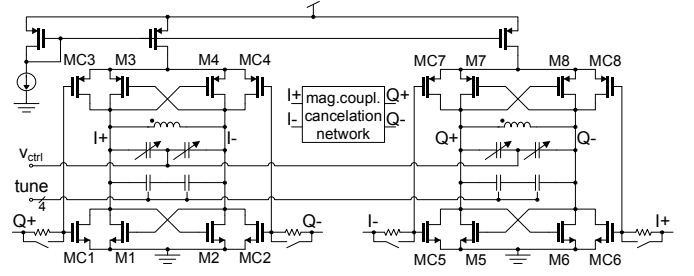[1]Triple-well process with 7 metal layers (2 thick top layers)
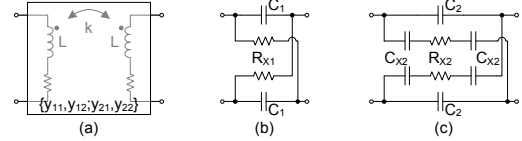

Fig. 2. Schematic of the implemented quadrature VCO

Fig. 3. Magnetic coupling cancelation: (a) Y-matrix representation of coupled inductors, (b) simplest cancelation network, (c) improved cancelation network

compensate process variations is achieved with a switched MOM-capacitor bank while PMOS varactors allow for fine frequency control within a phase-locked loop.

The coupling between the two cores at a phase difference of $90°$ is achieved by the parallel coupling transistors MCx. As shown in [8], phase shifting of ideally $90°$ in the coupling path reduces the phase noise and increases the oscillating amplitude. But since active phase shifting introduces additional power consumption we have implemented passive phase shifters of approximately $45°$ formed by a serial resistance and the gate capacitance of MCx. In order to allow measurements with and without phase shifting the resistances may be by-passed using switches.

While the decicated coupling mechanism forces the QVCO to operate in quadrature, the parasitic magnetic coupling tends to pull the QVCO towards in-phase or anti-phase operation. This problem may be avoided by using four inductors instead of two allowing for full symmetry with respect to the four quadrature phases [7]. Therefore, this solution is independent of the operating frequency and the magnitude of magnetic coupling. Alternatively, the magnetic coupling of the two-inductor QVCO may also be canceled. In the two-port representation of the coupled inductors [Fig. 3(a)] the magnetic coupling is represented by the transfer admittances y_{12} and y_{21}. Therefore, adding a shunt network with transfer admittances of equal magnitude and opposite signs cancels the coupling. Fig. 3(b) shows the simplest configuration of such a network with

$$C_1 = \frac{2 \, \mathfrak{Im} \{y_{21}\}}{\omega_0} \approx \frac{2k}{\omega_0^2 L} \tag{2}$$

$$R_{X1} = \frac{-1}{2 \, \mathfrak{Re} \{y_{21}\}} \approx \frac{Q_L \omega_0 L}{4k}. \tag{3}$$

Using this structure the required value of R_{X1} is approximately 50 kΩ. In order to reduce the required resistance to values in the order of 1 kΩ, the network of Fig. 3(c) is
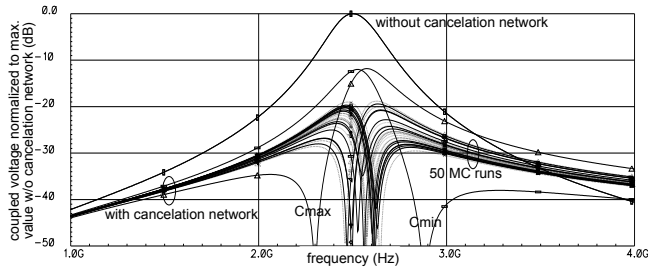
Fig. 4. Monte Carlo and worst-case simulation of magnetic coupling cancelation (normalized to uncanceled coupling)

Fig. 5. Layout of the quadrature VCO
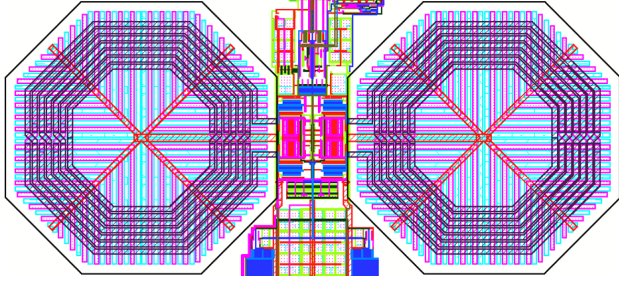

Fig. 6. Schematic of the implemented VCO with divider-by-2
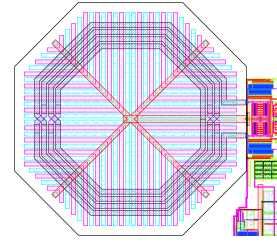
Fig. 7. Layout of the 5GHz VCO with divider-by-2

implemented instead.

$$C_{X2} = \frac{-4}{\omega_0 \, \Im\{1/y_{21}\}} \approx \frac{4k}{\omega_0^2 L} \tag{4}$$

$$R_{X2} = -\frac{1}{2} \, \Re\left\{\frac{1}{y_{21}}\right\} \approx \frac{\omega_0 L}{kQ_L} \tag{5}$$

$$C_2 = \frac{2 \, \Im\{y_{21} - 1/(y_{21}^{-1})^*\}}{\omega_0} \approx \frac{4k}{\omega_0^2 L} \tag{6}$$

This network consists of MOM-capacitors with $C_2 = C_{X2} = 16\,fF$ and high-resistive Poly resistors with $R_{X2} = 920\,\Omega$. Clearly, this cancellation technique is both frequency dependent and susceptible to process variations. Therefore, it may be used in narrow-band systems and only to reduce the phase error due to magnetic coupling to a tolerable level. Fig. 4 shows that the decoupling network achieves at least a 11.5 dB reduction of the coupled voltage from one inductor to the other (both resonating at 2.45 GHz) for the worst-case process corners which are mainly defined by the MOM capacitance variation. The layout implementation of the quadrature VCO with decoupling network is shown in Fig. 5.

B. VCO+DIV2

Also the VCO running at twice the frequency is implemented as a current-reuse cross-coupled LC VCO. The same inductor selection procedure as for the QVCO has lead to a symmetrical 4-turn inductor (L=4.6 nH, Q_L=12 @4.9 GHz). Due to the lower inductance compared to the QVCO solution an increased bias current of 150 μA is required to obtain a single-ended amplitude of $\approx$250 mV. Again, coarse and fine tuning has been implemented by a switchable capacitor bank and PMOS varactors.

For the divider-by-2 a master-slave configuration of two source-coupled-logic (SCL) latches is commonly used [9].
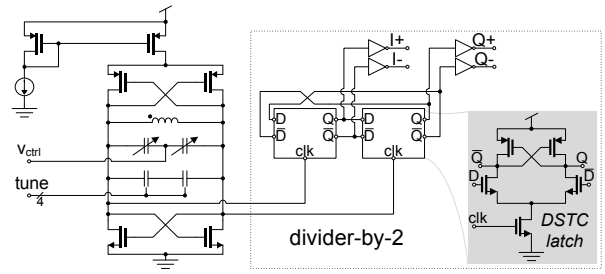
However, in order to lower the power consumption we have used dynamic single-transistor-clocked (DSTC) latches [10]. Two DSTC latches in a master-slave flip-flop configuration can be seen as a two-stage injection-locked differential ring oscillator. Such injection-locked dividers (ILD) have recently been demonstrated with extremely low power consumption [11], [12]. However, on contrast to these ILDs our DSTC based divider operates differentially and thus offers truly symmetrical output phases.

The circuit implementation of the VCO with the DSTC based divider-by-2 is shown in Fig. 6. Note that no buffering between the VCO and the divider is needed because the cross-coupled NMOS pair of the VCO already provides the required common mode voltage for the NMOS input of the divider with respect to process and temperature variations. Therefore, in the layout of the VCO+DIV2, shown in Fig. 7, these NMOS transistors are implemented as matched devices. The remaining transistors of the DSTC latches are almost minimum sized in order to reduce the power consumption of the divider.

The divider-by-2 block must be symmetrically laid out to achieve small phase errors. Still, a postlayout phase error smaller than 2° is hardly achievable. Moreover, mismatch between the minimum sized transistors of the divider introduces a significant statistical phase error with a standard deviation in the order of 4°.

V. POSTLAYOUT SIMULATION RESULTS

Both implementations including parasitics extracted from the layouts have been simulated using Cadence® SpectreRF. The simulations are performed with identical load conditions, i.e. in both cases the I and Q outputs have been loaded by output drivers and by the divide-by-4 input stage of a phase-switching prescaler. This divider is also based on the DSTC latches with differently sized input transistors and was also
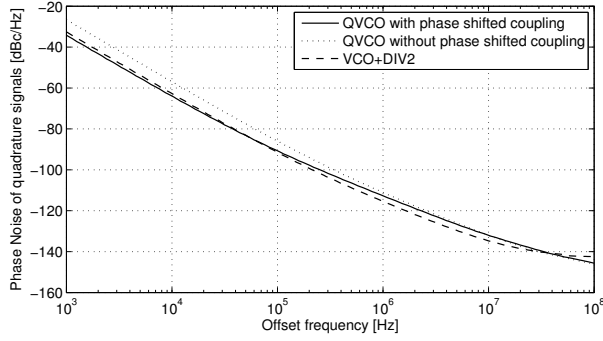
Fig. 8.   Postlayout phase noise simulation using SpectreRF®

TABLE I

PERFORMANCE SUMMARY BASED ON POST-LAYOUT SIMULATIONS WITH EQUAL LOAD CONDITIONS

Parameter	QVCO[a]	VCO+DIV2
Supply voltage (V)	1.0	1.0
Oscillator current (μA)	185	155
Divider current (μA)	N/A	165
Output amplitude (V)[b]	0.28/0.26	1.0
Output Phase Noise (dBc/Hz)	-90.7/-85.9 @100kHz -112.7/-111.1 @1MHz -120.7/-119.7 @2.5MHz	-91.4 @100kHz -115.7 @1MHz -124.3 @2.5MHz
Area (mm^2)	0.169	0.062
Phase error (°) deterministic standard deviation	-2.3/-1.1 1.3/1.5	-2.5 3.8

[a] Performance with/without phase shifting
[b] Single-ended peak-to-peak

simulated with extracted parasitics. Moreover, the magnetic coupling between the two QVCO inductors has been estimated using an electromagnetic solver (Momentum) at $k = 1.4\%$.

The phase noise simulation in Fig. 8 shows, that activating the phase shifting in the coupling path of the QVCO reduces the phase noise contribution of the coupling transistors at lower offset frequencies where the $1/f$-noise is dominating. The VCO+DIV2 phase noise is strongly dominated by the LC oscillator. Only at offset frequencies larger than $\approx$10 MHz the divider-by-2 contributes significantly to the overall phase noise. Comparing the two architectures, the VCO+DIV2 performs better at larger offset frequencies ($>$1MHz) which is also the critical frequency range as it is outside the PLL bandwidth.

Table I summarizes the important parameters of both implementations while table II compares the two designs to recently published work. The figure-of-merit (FoM), defined as in [5]

$$FoM(\Delta\omega) = 10\log\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{\mathcal{L}(\Delta\omega)}\frac{1mW}{P}\right], \quad (7)$$

relates the phase noise $\mathcal{L}$ at the offset frequency $\Delta\omega$ to power dissipation P and oscillating frequency ω_0.

VI. CONCLUSIONS

After revising low-power strategies of oscillators and quadrature generation two prototypes have been presented.

TABLE II

PERFORMANCE COMPARISON TO RECENT QUADRATURE GENERATORS

	[9]	[13]	[14]	This Work[*]	
CMOS Process (nm)	180	130	180	90	90
Architecture	VCODIV2	QVCO	QVCO	QVCO	VCODIV2
Frequency (GHz)	2.4	2.2	2.4	2.4	2.4
Power (mW)	8.8	0.6	1.2	0.18	0.32
Phase Noise (dBc/Hz@MHz)	-130 @10	-110.7 @1	-103.7 @1	-112.7 @1	-115.7 @1
FoM (dB)	168.2	179.8	170.5	187.8	188.3

[*] based on post-layout simulation

Although the QVCO approach requires much more area it consumes far less power than the VCO+DIV2 architecture and achieves a comparable phase noise performance. A new technique to reduce the deterministic phase error induced by magnetic coupling in the QVCO has also been presented.

VII. ACKNOWLEDGEMENTS

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