

Jitter-Power Minimization of Digital Frequency Synthesis Architectures

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Abstract— Digital intensive architectures allow for flexibly programmable frequency synthesis. Timing jitter and/or phase noise is an important quality criterion for synthesizers. This paper reviews fundamental limitations for jitter in digital frequency architectures, aiming at finding a basis to compare alternative architectures and optimize jitter performance. It motivates why the product of jitter variance and power consumption is a useful figure of merit (FoM) for optimization, based on fundamental physical limitations. Applying this FoM to multi-phase clock generation leads to the conclusion that circuits with low delay are preferred, favoring a shift register architecture (“ring counter”) over a Delay Locked Loop. For a PLL a Jitter-Power FoM is also defined and we show that significant improvements have been made during recent years.

I. INTRODUCTION

CMOS technology downscaling primarily benefits digital signal processing, making it increasingly attractive to exploit digital intensive architectures also for frequency synthesis. Such architectures can also offer flexible programmability. This is a vital asset for realizing a software defined radio or cognitive radio, where frequency synthesizers should cover multi-octave or even multi-decade frequency bands [1-2]. Architectures with programmable dividers can deliver such flexibility. Often multi-phase clocks are also needed, e.g. for image rejection and I/Q (de-)modulation, time-interleaved A/D conversion [3], and harmonic rejection [2, 4].

Low jitter timing is of critical importance for instance in A/D converters and communication receivers. Jitter, or its frequency domain counterpart phase noise, fundamentally limits the Signal-to-Noise ratio and hence the Bit Error Rate. Jitter can have many causes. Like any analog circuit, timing circuits are limited by fundamental physical limitations. Here we focus on random timing errors caused by 1) component mismatches and 2) noise. Noise is fundamentally associated with electron charge transport in MOS transistors. Component mismatches are introduced during production, e.g. due to dopant fluctuations, lithographic edge roughness or grain boundary effects [5]. Mismatch errors are “fixed during production” and hence render a fixed clock skew. However, if multiple digital signals contribute timing errors, e.g. via an edge combiner [6] or in multi-path mixers [4, 7], time variant patterns result which we will call “mismatch jitter” [8]. As the mismatch errors don’t vary with time, they can in principle be reduced by digital calibration techniques.

However, accurate detection and correction of (small) timing errors is not trivial and adds considerable cost and complexity. Here we aim at minimizing mismatch errors by architecture and circuit design. We will show that this can be done by minimizing the product of timing jitter variance and power consumption, which not only reduces mismatch jitter, but also thermal noise induced jitter, which calibration does not solve.

The contents of the paper are as follows. Section II motivates why the product of jitter variance and power is a useful Figure of Merit to minimize jitter [8-9]. This criterion FoM_{JP} is then evaluated for simple circuits to show that low delay is beneficial to reduce FoM_{JP} . In section III the insights are applied to multi-phase clock generator design and in section IV to PLL design, while conclusions are drawn in section V.

II. JITTER-POWER FUNDAMENTALS AND FoM_{JP}

Digital gates are at the basis of digital signal processing and can be constructed in different ways using CMOS technology (see Figure 1). Dynamic Transmission Gates (DTG) and Static CMOS logic are probably most common, whereas Current Model Logic (CML) is also used, e.g. for high frequency [6]. Digital signals passing through logic gates experience delay, and variation in this delay can represent jitter. To model jitter due to component mismatch and noise, it is useful to identify the basic delay mechanisms. Assuming the gates are driven by fast input edges, three mechanisms can be distinguished:

- In a transmission gate, the load capacitance C is charged via an equivalent resistor, related to MOSFET switch on-resistances.
- In static CMOS logic gates, an inverter largely acts as a current source charging a capacitor, where the delay is related to the load capacitance and the slew rate I_d/C [10].
- In CML gates, a current source is switched to a parallel RC load network, for which the RC time defines delay.

Variations in the switch resistance, transistor current, resistor value or capacitor value hence result in delay variation. Table 1 gives simple expressions for component mismatch and noise parameters. It uses the basic square-law text-book MOS model, which is far from accurate for modern technology but still useful to provide first order design insight. As digital circuits tend to be very broadband, noise induced jitter is dominated by thermal noise, and $1/f$ noise is neglected.

A. W-scaling and Jitter

Now consider what happens if we scale the width of a transistor during circuit design (“W-scaling”). If we do this for all components by a factor n this is equivalent to putting n identical circuits in parallel. This can also be referred to as impedance scaling [6] or admittance scaling [11]. W-scaling is useful for analog design, as it improves Signal-to-Noise ratio at the cost of power consumption, while not affecting many other properties like distortion and bandwidth. Similarly, W-scaling can be useful for low jitter design. Table 1 shows in the right column the effect of W-scaling by a factor n . We see that the *variance* of all *mismatch as well as noise* properties are *reduced by a factor n* , while the *current increases by a factor n* . Note that W-scaling does not affect the speed (delay) as capacitance is increased by the same factor than resistance goes down or current goes up. This W-scaling assumes that everything can be scaled simultaneously, which may be problematic at the boundary of a system (input and load). We return to this subject later. For now the conclusion is that W-scaling reduces jitter variance, while the power consumption goes up with the same factor.

B. Jitter Variance-Power Figure of Merit (FoM_{JP})

We saw that we can W-scale a circuit to improve jitter at proportional cost in power. When comparing circuits, we like to remove this systematic dependence from comparison data, by normalizing jitter variance to power consumption, similar to [6]. We hence define a Jitter-Power FoM_{JP} as:

$$FoM_{JP} = \sigma_t^2 \cdot P_d \quad (1)$$

where σ_t is the absolute rms-timing jitter due to mismatch or noise and P_d is the power dissipation of the circuit. Note that smaller FoM_{JP} indicates better performance.

C. Relation FoM_{JP} and Gate Delay

It is instructive to consider the simple case of a transmission gate modeled as a switch with series resistance charging a capacitive load. As switch resistance and load capacitance directly define delay, variation of delay can be expressed as:





$$\sigma_{t,TG}^2 = t_{d,TG}^2 \cdot \left[\frac{\sigma_C^2}{C^2} + \frac{\sigma_{Rsw}^2}{R_{sw}^2} \right] \quad (2)$$

Parameter σ_{Rsw} is again a function of the transistor mismatch parameters σ_{VT} and σ_β and the voltage V_{GS} (see Table 1). Thus we can derive more detailed expression, but for the purpose of first order design insight, it suffices to conclude that the jitter variance increases for increasing delay. From calculations and simulations (see also section III) we find this holds also for other logic families, at least for transmission gate logic, static CMOS logic and CML.

If we multiply eqn. (2) by power, estimation expressions for FoM_{JP} can be derived. Expressed in terms of delay, the results

differ a bit for different logic families. For current mode logic we find that FoM_{JP} increases linearly with delay [8], whereas for transmission gate logic and static CMOS logic the relation is closer to quadratic. As a design guideline, we conclude that Jitter-Power FoM_{JP} increases with delay, i.e. *minimizing delay is good for minimizing jitter*.

Table 1: Mismatch and noise parameters and the effect of W-scaling

Original Circuit	Effect W-scaling by n
<p>MOSFET with size W/L used as switch</p>  $I_D \approx \beta V_{GS} - V_T V_{DS}$ $r_{ds} = 1 / (\beta V_{GS} - V_T)$ $\sigma_{vn}^2 = 4kT \cdot r_{ds} \cdot \Delta f$ $\sigma_{VT}^2 = A_{VT}^2 / (W \cdot L)$ $\beta = \mu \cdot C_{ox} W / L$ $\sigma_{\Delta\beta/\beta}^2 = A_\beta^2 / (W \cdot L)$	<p>MOSFET size nW/L</p> $I'_D = n \cdot I_D$ $r'_{ds} = r_{ds} / n$ $\sigma_{vn}'^2 = \sigma_{vn}^2 / n$ $\sigma_{VT}'^2 = \sigma_{VT}^2 / n$ $\sigma_{\Delta\beta/\beta}'^2 = \sigma_{\Delta\beta/\beta}^2 / n$
<p>MOSFET with size W/L used as current source</p>  $I_D = \frac{1}{2} \beta V_{GS} - V_T ^2$ $g_m = \beta V_{GS} - V_T $ $\sigma_{vn}^2 = 4kT \gamma \Delta f / g_m$ $\sigma_{VT}^2 = A_{VT}^2 / (W \cdot L)$ $\beta = \mu \cdot C_{ox} W / L$ $\sigma_{\Delta\beta/\beta}^2 = A_\beta^2 / (W \cdot L)$	<p>MOSFET size nW/L</p> $I'_D = n \cdot I_D$ $g'_m = n \cdot g_m$ $\sigma_{vn}'^2 = \sigma_{vn}^2 / n$ $\sigma_{VT}'^2 = \sigma_{VT}^2 / n$ $\sigma_{\Delta\beta/\beta}'^2 = \sigma_{\Delta\beta/\beta}^2 / n$
<p>Resistor</p>  $\sigma_{vn}^2 = 4kT \cdot R \cdot \Delta f$ $\sigma_{\Delta R/R}^2 = A_R^2 / area$	$\sigma_{vn}'^2 = \sigma_{vn}^2 / n$ $\sigma_{\Delta R/R}'^2 = \sigma_{\Delta R/R}^2 / n$
<p>Capacitor</p>  $\sigma_{\Delta C/C}^2 = A_C^2 / area$	$\sigma_{\Delta C/C}'^2 = \sigma_{\Delta C/C}^2 / n$

III. MULTI-PHASE CLOCK GENERATOR DESIGN

We will now apply the insight that delay minimization is good for FoM_{JP} to design a multiphase clock generator.

A. Logic Family and jitter-power

Let's now consider differences between logic families, which exhibit different delay mechanisms (the discussion above considered W-scaling “within a logic family”). To compare different logic families with respect to FoM_{JP} we simulated a four phase generator implemented using three well-known flip-flop topologies as shown in Figure 1. We used 90nm CMOS at $V_{dd}=1.2V$, with minimum length flip-flop transistors and W as indicated in the figure. A differential input clock with 50% duty-cycle is used at 4GHz and 48V/ns slewrate. Two loading conditions are considered: 1) by a buffer (CML or CMOS inverter) of equal size than the flip-flop devices; 2) by a buffer with three times wider devices. CMOS inverters are used as clock buffers for static CMOS and DTG, with 2.5 times smaller

Table 2: Simulation results of four phase generator with CML, static CMOS and dynamic transmission gate flip-flops.

Flip-flop Topology	Delay [ps]	Power [mW]	Mismatch Jitter [fs ²]	Thermal Noise Jitter [fs ²]	Mismatch FoM _{PJm} (W*fs ²)	Noise FoM _{PJn} (W*fs ²)
Load capacitance is a buffer with same size as the flip-flop device size						
CML	14.5	12.2	(139) ²	(15) ²	236	2.93
Static CMOS	29	3.1	(149) ²	(7) ²	69	0.152
Dynamic TG	12.5	3.33	(65) ²	(4.2) ²	14	0.06
Load capacitance is a buffer with 3 times of flip-flop device size						
CML	19.2	12.21	(166) ²	(19) ²	336	4.41
Static CMOS	36	3.65	(191) ²	(8.8) ²	133	0.283
Dynamic TG	20.5	3.98	(103) ²	(5.9) ²	42	0.139

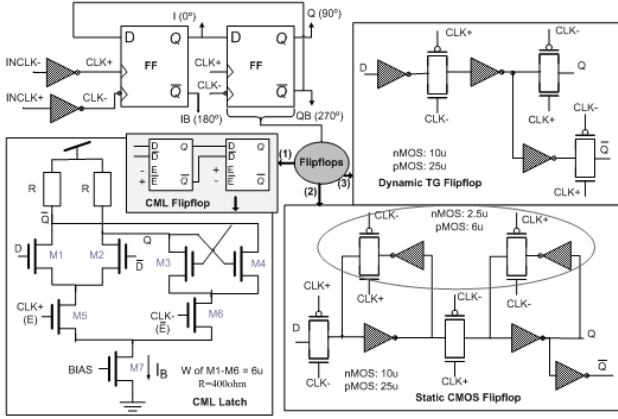


Figure 1: 4-Phase clock generators using 3 CMOS flip-flop implementations

W than the sum of the W of their load devices. The latches in the CML flip-flop use a voltage swing of 600 mV ($R=400\ \Omega$, $I_B=1.5\ \text{mA}$). For the CML clock buffer (not shown in figure), $R=150\ \Omega$ and $I_B=4\ \text{mA}$ is chosen after some iterative simulations to improve the FoM_{JP}.

Despite the CML optimization, we find a DTG flip-flop FoM_{JP} which is significantly better than for the other logic families. This difference in performance is primarily due to two factors: (1) The low delay of digital gates compared to CML in deep submicron technologies (note that DTG delay is even lower than for CML even with 1.5mA of current when loaded by the same sized buffer). (2) The low static power consumption of DTG compared to CML gates, which makes CML power wasting for a medium and low frequency range of operation.

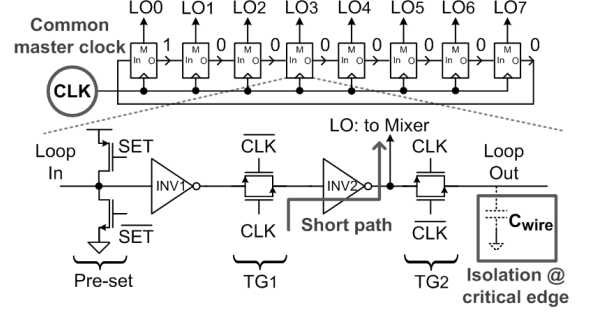


Figure 2: Multi-Phase Clock Generator with low phase error achieved by minimizing delay (short path and isolation of C_{wire} during the critical edge).

B. Divider-DLL comparison for multi-phase generation

Based on the Jitter-Power FoM, different multi-phase clock generator architectures can be compared. In [8] this has been done for a Delay Locked Loop to a shift register. A DLL needs to make a delay equal to the required time-shift between multi-phase outputs. In contrast, a shift register can use low-delay latches or flip-flops, which have much lower Jitter-Power FoM. This leads to the conclusion that a shift registers divider, also referred to as a “ring counter”, is preferred over a DLL with respect to FoM_{JP} [8].

C. Low Phase Error Multi-Phase Clock Generator Design

In section II-B we discussed why a multi-phase clock generator based on a ring counter has better FoM than a DLL and in the section III-A we showed that transmission gate logic can achieve a better FoM_{JP} than current mode logic.

These two insights lead to the architecture in Figure 2, a ring counter with transmission gate latches clocked by a central clock. Eight outputs (LO0-LO7) are generated, running at 1/8 of the CLK frequency, with 1/8 duty cycle, used as LO drivers for a harmonic rejection mixer requiring low phase error [4]. One cell is shown in detail, indicating there is a short path to the LO-output. To minimize the delay and hence optimize FoM_{JP}, TG1 and INV2 are placed close to the mixer (small wire capacitance). Moreover, the (long) capacitive lines and input capacitance of the next cell in the chain is isolated from the LO-output node by TG2 during the critical edge (e.g. rising edges of CLK; falling edges are used to connect to the next cell).

Monte Carlo simulations of the phase deviation from 45° between two adjacent 0.8GHz LO-phases due to mismatch were done, including the contribution from mixer switches. A $\sigma=0.024^\circ$ was found, i.e. 0.08ps for 0.8GHz. At 0.8GHz LO, the power consumption of the ring counter is 5.4mA at 1.2V supply, while the CLK input buffers consume 8.9mA driven by 6.4GHz differential input clocks. Thus, using this FoM driven design we were able to achieve >60dB harmonic rejection, about 20dB better than previous designs [4].

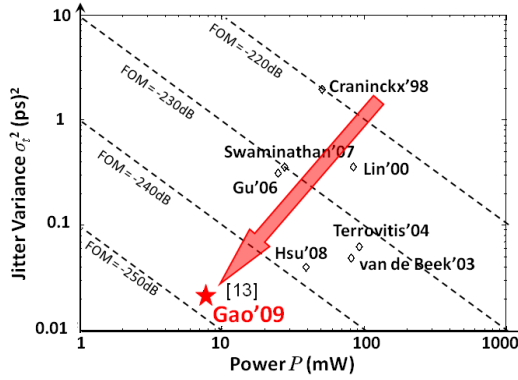


Figure 3: Jitter versus power plot of low-Jitter PLL designs published at ISSCC

IV. PLL OPTIMIZATION – PLL FOM

Let's now consider our work on PLL design [9, 12-13]. In contrast to multi-phase clock generators, a PLL usually has only one output. Then mismatch is not defined, but noise induced jitter is important. We can now again use the W-scaling argument of section II, but now apply it to minimize noise induced jitter. In [9, 13] a traditional PLL structure was analyzed. Assuming $1/f$ noise can be neglected, the long term absolute jitter was estimated by integrating the phase noise of the PLL over frequency. The main phase noise contributions in a traditional type-II PLL are: 1) VCO phase noise with $1/f_m^2$ roll-off, which is high-pass filtered in the PLL; 2) "In-band" loop noise with a white spectrum introduced by the loop components which detect and control the phase error. This noise is low-pass filtered by the loop. It can be shown that minimum integrated jitter occurs at a certain optimum loop bandwidth f_c [9, 14]. For this optimum condition, both noise contributions are equally important and the Jitter-Power FoM for the VCO is equally important to the Loop Component Jitter-power FoM. Based on this assumption a Jitter-Power FoM can be defined for PLLs which is compatible with the well-known FoM for Oscillator phase noise resulting in [9].

$$FoM_{PLL} = 10 \cdot \log \left(\frac{\sigma_t^2 P_{PLL}}{(1s)^2 \cdot 1mW} \right) \propto FoM_{VCO} + FoM_{loop} \quad (3)$$

Exploring different integer-N architectures aiming at low FoM_{PLL} , we discovered that direct sampling of the VCO output by a reference clock allows for achieving very low in-band phase noise (very high detector gain), while also requiring no divider, saving power. Low delay reference buffers are used to achieve very low jitter achieving superior FoM (see Figure 3).

V. CONCLUSIONS

In this paper we reviewed ways to minimize jitter in digital frequency synthesis focusing on two fundamental limitations:

- 1) jitter between multiple outputs due to component mismatch
- 2) jitter in a single output induced by thermal noise.

We showed that W-scaling allows for reducing jitter at the cost of power consumption. The figure of merit FoM_{JP} normalizes for this effect, which is useful to evaluate jitter performance, insensitive to this scaling effect. We discussed that FoM_{JP} for logic circuits increases with circuit delay. Architectures and circuits that exploit low delay circuits can achieve lower FoM_{JP} , i.e. can achieve lower jitter for a given power budget. This FoM is also the basis for the PLL-FOM defined in [9]. It has been a design guideline used for the design of several low jitter digital intensive CMOS architectures. The designs have been verified by silicon realizations published at ISSCC[13] and in JSSC [4, 12].

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