A Preamplifier for the Front-End Readout System of Particles Tracking in Secondary Electron Detectors

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***Abstract*—This paper presents the design and characterization of a preamplifier used in the electronic front-end of low-pressure gaseous secondary electron detectors. The circuit – implemented in a printed circuit board as a proof of concept – has been designed to cope with the specifications of the readout electronics used in spatial resolution measurements. Experimental results show a transimpedance gain of 80dB, an overall voltage gain of 18 dB, a peak signal-to-noise ratio of 36.5 dB and a *shaping* time frame of 140-170ns. These features improve the performance of previous reported approaches to the problem, and allow us to minimize the overlapping probability in secondary electron detections for radioactive ion beams tracking, achieving a counting rate higher than 10^6 particles per second[1].**

I. Introduction

Next generation of particle accelerators will provide low-energy Radioactive Ion Beams (RIB) with less than 10MeV per nucleon and counting rates of 10^6 particles per second (pps). These beams will allow to get a deeper understanding of the nuclear structure as well as the reaction mechanisms of new isotopes. The principle of operation is based on the reconstruction of ions tracks before the target impact, in order to properly identify the initial conditions of the particles which give rise to nuclear reactions. That track reconstruction requires suitable electronic readout systems for both spatial and time detection [1].

One of the most challenging circuits in these readout systems is the preamplifier. The design of this building block is specially critical due to its early position at the front-end interface connected to the detector [2]. An approach to implement the preamplifier is based on the principle of charge amplification, in which the preamplifier output voltage is a function of the input charge coming from the detector as well as the integration time and the value of the capacitor used to integrate the charge. This kinds of preamplifiers have been successfully applied in the past for experiments on CP-violation of kaon particles at Low Energy Antiproton Ring (CPLEAR), which were carried out at CEA-Saclay laboratories [3]. However, their performance may be severely degraded as the counting rate increases, which demands looking for alternative solutions [2].

This paper contributes to this topic and presents a 4-channel preamplifier system intended for spatial resolution measurements in a very specific kind of low-pressure gaseous detectors [4], named Mini Secondary electrons Detector (Mini-SeD) [1]. The circuit – based on the combination of a TransImpedance Amplifier (TIA) and a shaper filter – achieves faster operation than previous approaches and minimizes the probability of overlapping among signals coming from detected particles as the counting rate increases in beam tracking detectors. The system has been implemented in a Printed Circuit Board (PCB) and several experimental results – considering different experiment conditions – validate the preamplifier system presented in this paper.

II. System-Level Design

Fig. 1 shows a block diagram of the spatial detection system used in Mini-SeD detectors. The analog signal provided by the silicon detector and the anode output signal provided by the Mini-SeD are amplified and compared with a threshold voltage that must be higher than the system noise floor level in order to avoid capturing false events. This way, when a particle is detected, an active pulse known as "integration gate" is generated in order to set the integration time, as a first step to digitize the signal. A Charge-to-Digital Converter (QDC) is used as a digitizer in order to obtain the charge value at the output of the detectors cathodes. This way, the charge distribution around X and Y axis cathodes constitute the two-

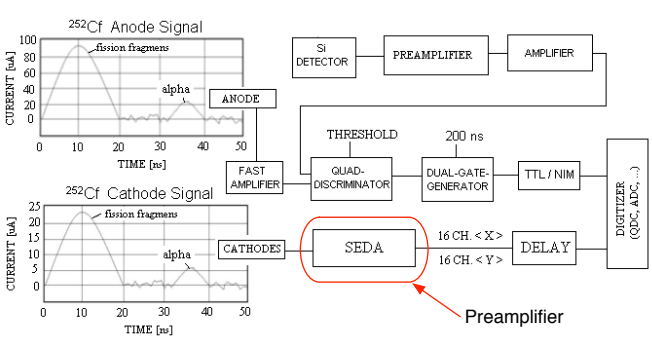

Fig. 1. Block diagram of the spatial detection system.

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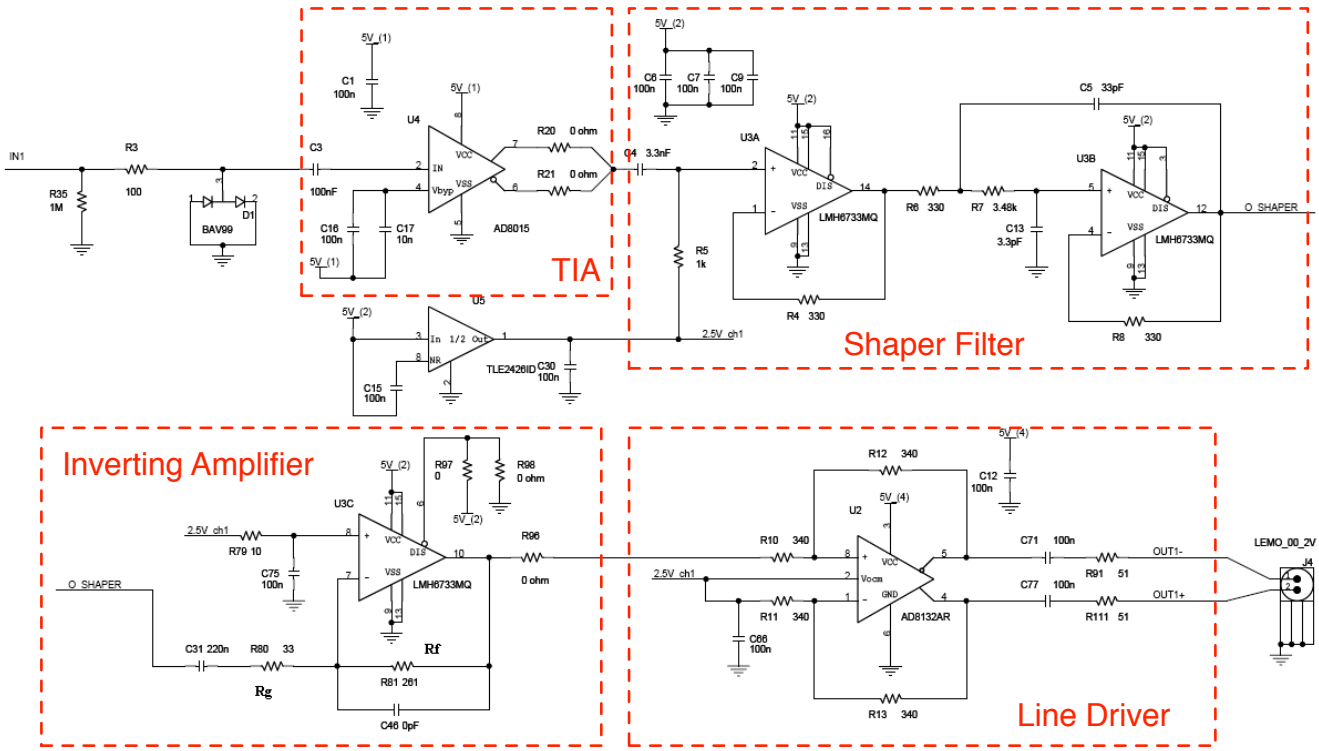

Fig. 2. Schematic of the proposed preamplifier (one channel).

dimensional spatial coordinates corresponding to a detected particle, also referred to as a *valid event*. The trigger indicates when an event takes place, i.e. when a particle is detected, and then, the QDC integrates a valid current provided by each channel of the preamplifier.

The proposed preamplifier, named Secondary Electrons Detector preAmplifier (SEDA) in Fig. 1, has been designed to process charge signals coming from Mini-SeD cathodes, tracking high counting rates of RIB with around 1μs of average *arrival time* between two consecutive particles. Thus, when a particle is detected, current signal waveforms coming from cathodes have approximately a 10ns rise/fall time. In order to relax the bandwidth specifications, these current signals waveforms are *shaped* so that they can be digitized by the QDC during an integration time period of 200ns, which in our case corresponds to a 20% of the average particles arrival time. Another important design specification is the Signal-to-Noise Ratio (SNR), which should be high enough to discriminate signal currents peaks generated in the cathodes when particles are detected, typically in the order of tens of μA.

One of the main limiting factors in Fig. 1 is the parasitic capacitance associated to the cable connections used in the experimental set-up environment. These parasitics may severely degrade the signal bandwidth and corrupt the detected signal due to the additional noise sources caused by the coupling effect of electromagnetic interferences. Therefore, the preamplifier should be placed as close as possible to the detector in order to minimize the impact of the mentioned parasitics. However, this is not always possible in practice due to spacing problems imposed by the vacuum chambers.

The preamplifier in this work has been designed to work outside the vacuum chamber. This forces using cables to connect each preamplification channel to the detector, with an associated input parasitic capacitance per channel of approximately 30pF. Another important design restriction imposed by cable connection is that the preamplifier output impedance should match with the cable input impedance, 50Ω in this case.

III. Preamplifier Architecture

Fig. 2 shows the schematic of one of the four (identical) channels of the proposed preamplifier. The system is composed of a TIA circuit, a shaper filter, an ac-coupled inverting amplifier and a line driver. An ElectroStatic Discharge (ESD) diode-based protection circuit is placed at the input node to avoid damages caused by high voltage sparks and other experimental set-up interference signals.

The preamplifier system in Fig. 2 has been implemented using commercial Integrated Circuits (ICs) as a proof of concept, as a previous step to design an ASIC. The different building blocks have been selected and configured in order to fulfill the system level performance in terms of voltage gain, transient response (characterized by fall- and rise time) and SNR. To this purpose, a simulation-based top-down design methodology has been followed – from system-level specifications to building-block specifications and final PCB implementation.

A. Transimpedance Amplifier

The TIA building block in Fig. 2 was implemented using the AD8015 IC. Using a transimpedance of 10kΩ, this circuit transforms the current signals coming from detector cathodes into voltage signals with a transimpedance gain of 80dB within a 240-MHz bandwidth, keeping the same rise/fall time and minimizing the probability of overlapping signals. In this configuration, this block has an input referred noise spectral density of $3\text{pA}/\sqrt{\text{Hz}}$ – in good agreement with the overall SNR specification.

The effect of parasitic capacitance on both signal bandwidth and noise figure have been taken into account in the simulations. Thus, considering a 30pF input parasitic capacitance, the TIA output total noise power is 3.35mV rms within a 32.7-MHz signal bandwidth.

B. Shaper Filter

As stated in previous section, a shaper filter is needed in order to slow down the preamplifier output signal so that it can be digitized by the QDC. To this purpose, a biquad filter configuration has been considered, made up of a RC High-Pass (HP) filter, a buffer and a second-order Low-Pass (LP) filter. The cut-off frequency of the RC HP filter was set to 50kHz in order to reduce the TIA output offset error and flicker noise. Both the buffer and the biquad filter were implemented using LMH6733 operational amplifiers configured with 0dB gain, yielding a shaping time lower than 200ns – in agreement with system-level required performance.

Multiple simulations were carried out in order to find out the optimum performance in terms of SNR, rise/fall time and cut-off frequency. We considered a 30pF parasitic capacitance an a current source with the same characteristics as Mini-SeD output current waveform signals, i.e., 10ns rise/fall time, 20μA current peak and 1μs period. Table I sums up the simulated performance, showing the main features for different values of the LP cut-off frequency. The 20-MHz bandwidth configuration was chosen, which corresponds to a peak SNR of 34.92dB, 70ns rise/fall time and 170ns shaping time.

C. Inverting Amplifier

The gain of the preamplifier is provided by the fourth block in Fig. 2, implemented as an ac-coupled inverting amplifier based on the LMH6733 opamp. This inverting configuration was designed to have a gain of 18dB, although this gain can be adjustable by changing resistors R_f and R_g. Since the preamplifier has both lower and upper saturation limits at 0V and 5V respectively, a 2.5V dc input voltage is needed to induce such offset value at the output of this block. Thanks to the aforementioned inverting configuration, the output offset error was reduced to 11mV. In the same conditions, single output signals from line driver were compatible with the ones obtained at the shaper output.

TABLE I. SHAPER OUTPUT PARAMETERS FOR DIFFERENT LPF CUT-OFF FREQUENCY VALUES

Shaper Output Parameters	**Biquad Cut-off Frecuency (MHz)**					
	10	**15**	**20**	**25**	**30**	**35**
Total Noise (mV_{rms})	1.60	1.61	1.63	1.68	1.78	1.89
Peak Voltage (mV)	54	81	102	118	130	140
SNR (dB)	30.5	34.1	35.9	36.9	37.2	37.4
Fall-time (ns)	38	35	33	30	29	27
Rise-time (ns)	91	63	37	27	26	25
Shaping Time (ns)	300	200	170	160	160	160

D. Line Driver

The last building block used in the preamplifier chain of Fig. 2 is a differential line driver. This block – implemented by using the AD8132 IC – was designed to properly transmit the required high-speed signals over 50Ω coaxial cables connecting the preamplifier and QDC in Fig. 1, with minimal line attenuation and reduced effects of ground noise.

IV. CIRCUIT IMPLEMENTATION AND EXPERIMENTAL RESULTS

The preamplifier system was implemented in a PCB, which is illustrated in Fig. 3. Different experiments were carried out in order to verify the performance of the circuit under different signal and environment conditions.

A. Pulse Generator Experiment

The first experiment was performed using a pulse generator, which emulates the Mini-SeD anode input signal. An impulse signal with an amplitude of 1.5V and 20ns rise-time was used in order to induce the same quantity of charge in all the cathodes, thus emulating a particle detection event. The cathodes output current signals were transmitted through the cable to a vacuum chamber flange. The other side of the flange was connected to the proposed (SEDA) preamplifier. For comparison purposes, the preamplifier used in CPLEAR experiment was also connected in parallel. Outputs from both preamplifiers were conected to a 15.56dB gain (differential-to-single) line receiver.

Fig. 4 compares the waveforms measured in an oscilloscope that were obtained at the single output of both preamplifiers, SEDA and CPLEAR, without using the line receiver. Note that both signals have a similar voltage peak (200mV) and shaping time (140ns). However, the output signal of the proposed preamplifier (depicted in channel 4 in Fig. 4) has a slower rise-time (40ns) than that obtained with the CPLEAR preamplifier,

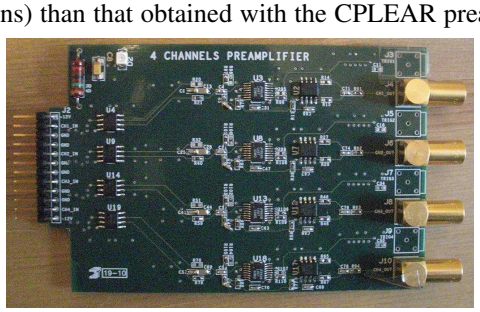

Fig. 3. 4-Channel preamplifier PCB.

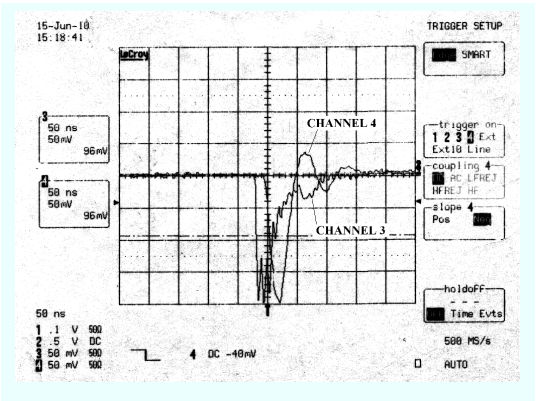

Fig. 4. Single output wave forms of the proposed preamplifier (channel 4) and the one used in the CPLEAR experiment [3] (channel 3).

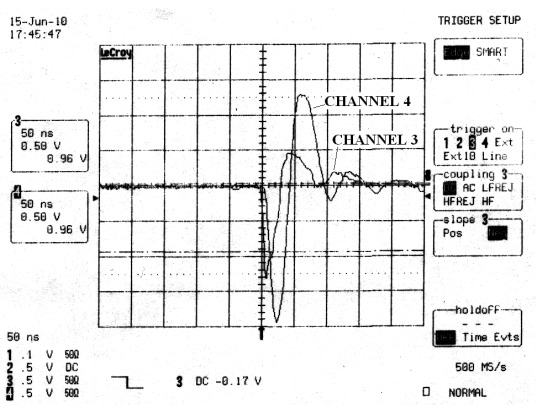

Fig. 5. Line receiver outputs for SEDA (channel 4) and CPLEAR (channel 3).

which results in a better digitization in the QDC. The noise measured in channel 4 is 3mV rms, which gives a peak SNR at the output of the proposed preamplifier around 36.47dB. These results are in good agreement with simulated performance and are suitable for the target application.

Fig. 5 compares the differential output signals of the proposed (SEDA) and CPLEAR preamplifier provided by the line receiver. Channel 4 in Fig. 5 shows the output of the proposed preamplifier after the line receiver, showing a 1.92-V peak voltage, 40-ns rise/fall time and 140-ns shaping time, which is less than integration time frame. Channel 3 shows the output of the CPLEAR after the line receiver, which has a 1.23V voltage peak, a 10-ns rise/fall time with the same shaping time as the proposed preamplifier (140ns). The noise measured in channel 4 is 18mV rms, which gives a SNR for the proposed preamplifier of 40.56dB.

B. Californium Source Experiment

The second experiment was carried out using a Californium source (^{252}Cf) emitting 96.91% of α particles and a 3.09% of fission fragments with around 1.55MeV/u over an emissive foil [5]. Due to the interactions with the emissive foil, secondary electrons are generated and then detected by the Mini-SeD. As in the first experiment, cathodes output current signals were transmitted through the cables to the chamber flange and, on

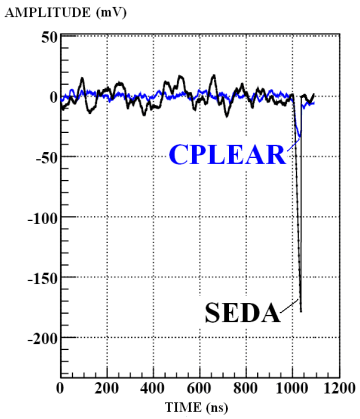

Fig. 6. ADC output signals.

the other side of the flange, both preamplifiers were compared. After the line receiver, an Analog-to-Digital Converter (ADC) was used to digitize both differential output signals.

Fig. 6 shows the ADC output in both cases under study. Note that both signals present voltage peaks caused by set-up noise, interferences and fission fragments. In this experiment, the spatial resolution is only interesting in fission fragments detection, since α particles can not be triggered due to their low amplitude comparable to the noise level. It can be noted that both signals have almost the same shaping time (100ns), but fission fragments voltage peak coming from the proposed preamplifier (SEDA) is higher (-175mV) than fission fragments voltage peak coming from CPLEAR (-35mV). In other words, the Dynamic Range (DR) between the fission fragments and noise voltage peaks obtained by the proposed preamplifier is 19.75dB, in contrast to 12.80dB obtained by CPLEAR preamplifier.

CONCLUSION

A preamplifier intended for the front-end electronic system used in spatial resolution detection in secondary electrons detectors has been presented. Measurement results of a PCB implementation considering different experiments have been shown that demonstrate better performance in terms of gain, SNR and transient response than previously reported preamplifiers used for this application. The proposed approach is a promising solution to minimize the overlapping probability in particles spatial detection for radioactive ions beams with counting rates higher than 10^6 pps. Therefore, a proof of concept has been verified and is being developed for a future integrated system.

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