SAR ADC USING SINGLE-CAPACITOR PULSE WIDTH TO ANALOG CONVERTER BASED DAC

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SAR ADC USING SINGLE-CAPACITOR PULSE WIDTH TO ANALOG CONVERTER BASED DAC

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Thesis

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ABSTRACT

This work presents a successive-approximation-register (SAR) analog-to-digital converter (ADC) using a single-capacitor-pulse-width-to-analog converter-based digital-to-analog (DAC). In the proposed SAR ADC, the single-capacitor DAC is realized by partially charging or discharging the sampling capacitor with a DC reference current. The charge and discharge time is determined by the pulse width of the control signal. As a result, a SAR ADC can be realized by using a single capacitor, a current source, a current mirror, a comparator, and control logic; the result is a significant reduction in the circuit area and a simplified switch control scheme, compared to conventional SAR ADCs using capacitor DACs. A 6-bit 500kS/s SAR ADC is designed using CMOS 0.35μm technology, and the operation is verified through circuit level simulations.

The effect of non-idealities including capacitor error, comparator offset, and current mismatch are analyzed, where ADC INL and DNL with each error are obtained. The power consumption of the ADC core was 22.6μw, which is lower than other designs. Aside from the low power consumption, with the single capacitor switching technique, the chip size is significantly reduced. The chip size of the proposed SAR ADC is around $0.01mm^2$, which is 60% to 80% smaller than other recent SAR ADC architectures.

DEDICATION

I would like to dedicate this thesis to my parents and Dr. Lee. This thesis would not have been possible without their support.

ACKNOWLEDGEMENTS

I would like to acknowledge my thesis advisory committee, Dr. Kye-Shin Lee, Dr. Seungdeog Choi, and Dr. Arjuna Madanayake, for their technical input and support throughout the conception, realization and culmination of this thesis project.

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CHAPTER I

INTRODUCTION

1.1 Motivation

An analog-to-digital converter (ADC) translates an analog input into digital output code. ADCs are used in data transforming, signal sensing and control systems [1]. The successive approximation resister (SAR) ADC architecture is chosen for medium-to-high-resolution applications with sample rates under 5 mega samples per second (mS/s). The resolution of SAR ADCs generally ranges from 6 to 16 bits, and they provide lower power consumption compare to other ADC architectures such as flash or pipeline ADC [2]. This combination of features makes the SAR ADC ideal for a wide variety of applications. They are frequently used in biomedical devices, such as pacemakers, implantable cardiac defibrillators, electroencephalography (EEG) and electrocardiography (ECG) sensor frontends [2-3]. Although high speed and high resolution are not required for such applications, small chip size and low power consumption are very important.

When SAR ADCs are used in biomedical sensing systems such as pacemakers and implantable cardiac defibrillators, low power consumption between 10 to 200 μW and resolution between 6 to 10 bits are required [1-4]. Thus, pacemakers and implantable cardiac defibrillator applications generally employ a SAR ADC with very low

frequency signal bandwidth within the range of 10 kHz and with a conversion rate up to 100kS/s [6, 8]. However, since multiple capacitors are being used in conventional SAR ADC design, the chip size and power consumption increase as the resolution increases. As a result, although a conventional SAR ADC has a lot of advantages such as high accuracy and high resolution, reducing the chip size and power consumption is a challenging task.

In order to overcome the drawbacks of the conventional SAR ADC a SAR ADC with a single capacitor pulse width to analog converter based DAC is proposed in this work. The single-capacitor DAC is realized by partially charging or discharging the sampling capacitor with a DC reference current, which will lead to significant capacitor area reduction. In addition, a capacitor charging and discharge selecting scheme is applied, which consumes less power than the conventional SAR ADC with multiple capacitor-controlling scheme. Therefore, the proposed SAR ADC is well qualified for use in pacemakers and implantable cardiac defibrillators.

1.2 Contribution and goal

ADC is the heart of bio-medical sensing systems. The goal of this design is to design a compact SAR ADC for pacemaker applications. In order to avoid using a big battery, low power is the most critical demand for such devices. In addition, the chip size is another critical factor for a compact implantable biomedical device. In order to achieve low-power and compact chip size, the designer needs to come up with a compromise between speed and resolution. For biomedical applications, in order to accurately detect the biomedical signals, the SAR ADC requires a resolution of at least 6 bits; however, for

the conversion speed, 500kS/s is good. This is because body signals such as the heartbeat pulse have a moderate frequency around 10kHz [6, 8].

To achieve this goal, a 6-bit, 500kS/s SAR ADC using single-capacitor pulse width to analog converter based DAC is proposed. Since only one capacitor is being used instead of multiple capacitors, the area can be significantly reduced. As well as reducing the area, the single capacitor approach can reduce the switching power consumption, which is a problem when multiple capacitors are used. As a result, this approach can be a good solution for low-speed applications where the area and power are the main design constraints. The proposed SAR ADC architecture is designed using CMOS 0.35µm technology with voltage supply of 3.3V. Cadence Design Systems was used for the circuit design, and simulation. The basic characteristics of the SAR ADC, including DNL and INL, were measured. In addition, various non-ideality analyses were performed. They are important for the thesis because they give us a better understanding of the proposed SAR ADC performance. The goal of this work is to realize a 6-bit, 500kS/s SAR ADC with core size less than 0.01 mm^2 and power consumption lower than 30µw [9].

1.3 Thesis organization

Chapter 2 presents background information related to the proposed SAR ADC. A conventional SAR ADC and several previous designs are described.

Chapter 3 describes the proposed SAR ADC design in detail. The basic concept of the single-capacitor DAC is presented, and the proposed SAR ADC architecture and operation are also mentioned. Furthermore, the advantages as well as disadvantages of the proposed SAR ADC architecture are analyzed.

Chapter 4 presents the circuit implementation of the proposed 6-bit SAR-ADC using single-capacitor pulse width to analog converter based DAC. The circuit level simulations are performed, and DNL and INL plots are given.

Chapter 5 presents the effects of non-idealities. Three major non-idealities including capacitor error, current mirror mismatch and comparator offset error are described.

Chapter 6 mentions the conclusions and future work.

CHAPTER II

BACKGROUND

This chapter presents the background information related to the proposed SAR ADC. In section 2.1, the SAR ADC theory is introduced, where we use the balance weighing algorithm to explain the SAR ADC operation. The SAR ADC block diagram is shown followed by an operation example of a 4-bit SAR ADC. In section 2.2, the conventional charge redistribution SAR ADC architecture is presented. Moreover, two other SAR ADC architectures are presented in section 2.3 and 2.4.

2.1 SAR ADC Theory

The SAR ADC is a type of analog to digital converter that converts a continuous analog input signal into a digital output code. The SAR architecture uses the binary search algorithm. A binary search locates an item in a sorted array by repeatedly dividing the search interval in half. The initial interval includes the entire array. If the value of the search key is less than the item in the middle of the interval, then the next interval will be the lower half of the current interval. If the value of the search key is greater than the middle item, then the next interval will be the upper half. The search process repeats until the item is found or the search interval is empty. The algorithm is very similar to weighing an item by using a balance and a weight set. The algorithm is shown in Fig. 2.1 where the unknown weight is 45 lbs, with a search interval of 64 lbs. In this

algorithm, first attempt compares X with half of the search interval, which is 32lbs. If X is greater than 32lbs, the next attempt compares with current interval plus half of the current interval. If X is less than 32lbs, the next attempt compares with current interval plus $^1/_4$ of the current interval. The balance scale analogy is used to demonstrate the algorithm [1].

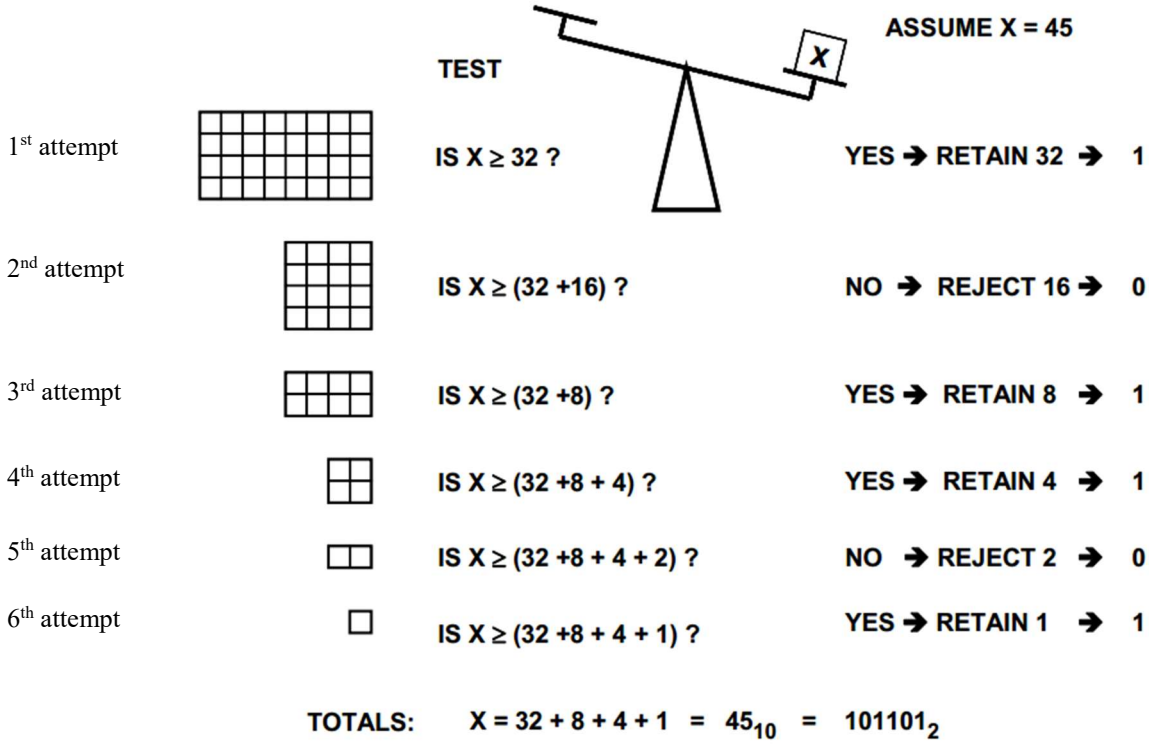


Figure 2.1 Balance weighing algorithm to explain the SAR ADC [1].

The conventional SAR ADC can be realized using the above balance scale method. The SAR ADC architecture consists of the comparator, DAC and control logic. Fig. 2.2 shows the block diagram of the SAR ADC.

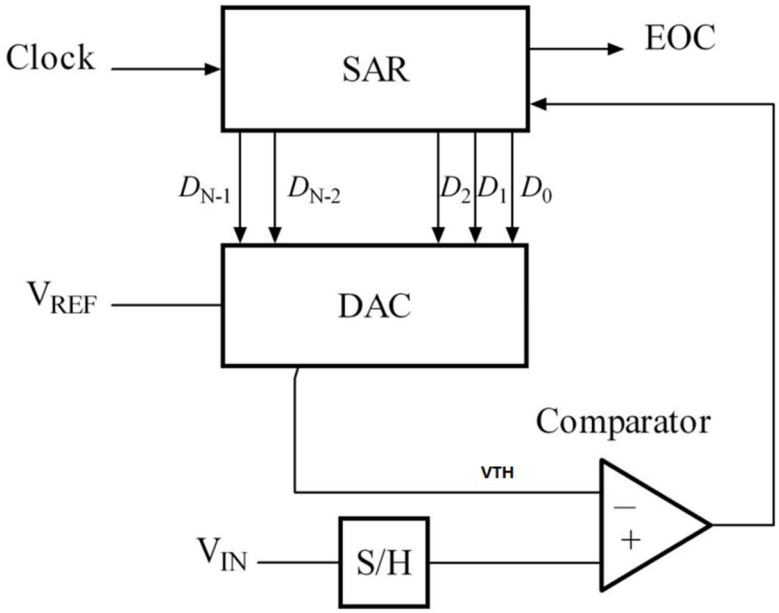


Figure 2.2 SAR ADC block diagram [1].

There are three operations involved in the SAR analog to digital conversion: input signal sample and hold, generating decision levels and making comparison. The first step of the conventional SAR ADC operation shown in Fig. 2.2 is the sample and hold circuit to acquire the input voltage V_{IN}. In the second step the input voltage V_{IN} is compared with half of the reference voltage $^{VREF}/_{2}$, and the comparator generates the digital output code that goes back to the DAC as a control signal, which will generate the next comparator threshold level V_{TH} for the next comparison. In this case, if the comparison result is higher, the next attempt compares with current reference voltage plus half of the current reference voltage. If the comparison result is lower, the next attempt compares with current reference voltage plus $^{1}/_{4}$ of the current reference voltage. By repeating each step in the same manner, the digital outputs D_{N-1} to D_0 will be generated, and the conversion will be completed.

As an example, the operation of a 4-bit SAR ADC with V_{IN} = 0.85V is shown in Fig. 2.3 (Input range = 1V). In the first clock cycle DAC input is 1000 and it sets the reference voltage to $V_{REF}/2$, then the input voltage is compared with $^1/_2V_{REF}$ and based on the comparison result, D_3 is set to 1. In the next clock cycle, which makes the reference voltage to ¾V_{REF}. D_2 result in 1, since V_{IN} is larger than ¾V_{REF}. For the next bit the DAC input is set to 1110, which makes the reference voltage to $^7/_8V_{REF}$. Based on comparison, D_1 is set to 0 since V_{IN} is smaller than $^7/_8V_{REF}$ and finally for determining D_0, the DAC input is set to 1101. D_0 is 1 because V_{IN} is larger than $^{13}/_{16}V_{REF}$. Therefore, the analog input 0.85V is converted into the digital output code 1101 in four clock cycles.

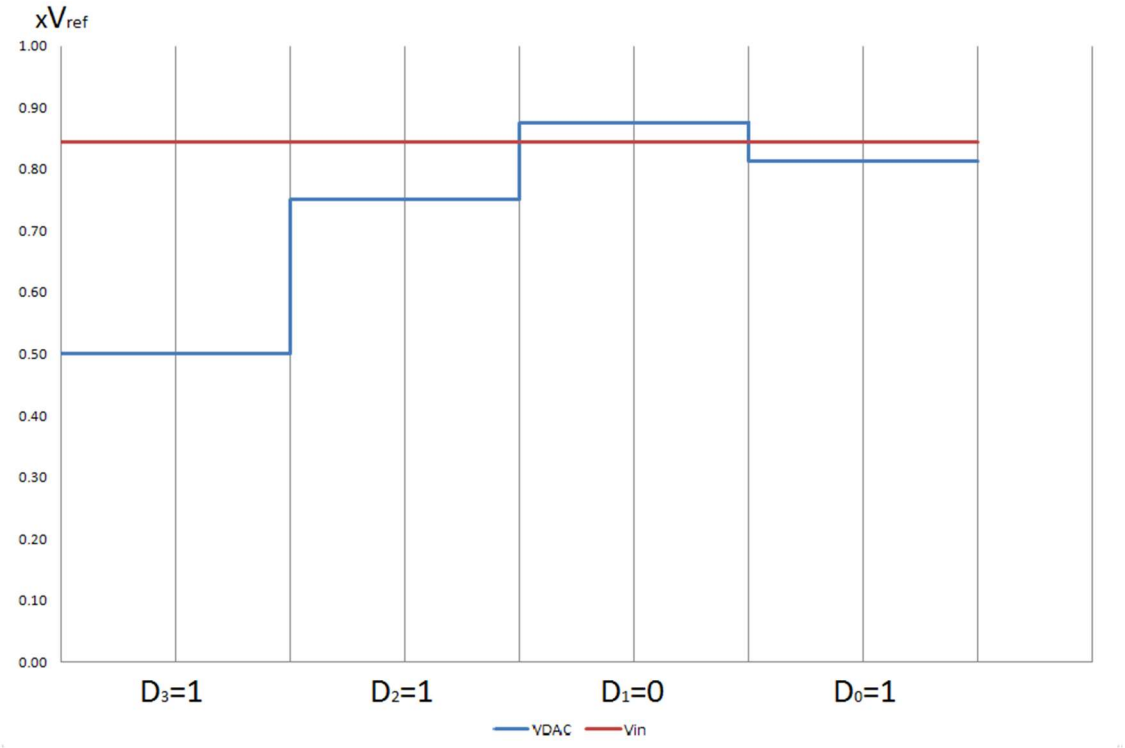


Figure 2.3 A 4-bit SAR ADC operation example [1].

2.2 Charge-redistribution SAR ADC architecture

The most common SAR ADC is the charge-redistribution SAR ADC which uses a charge scaling DAC. The charge scaling DAC simply consists of an array of individually switched binary-weighted capacitors. The amount of charge upon each capacitor in the array is used to perform the binary search in conjunction with a comparator internal to the DAC and the successive approximation register [1].

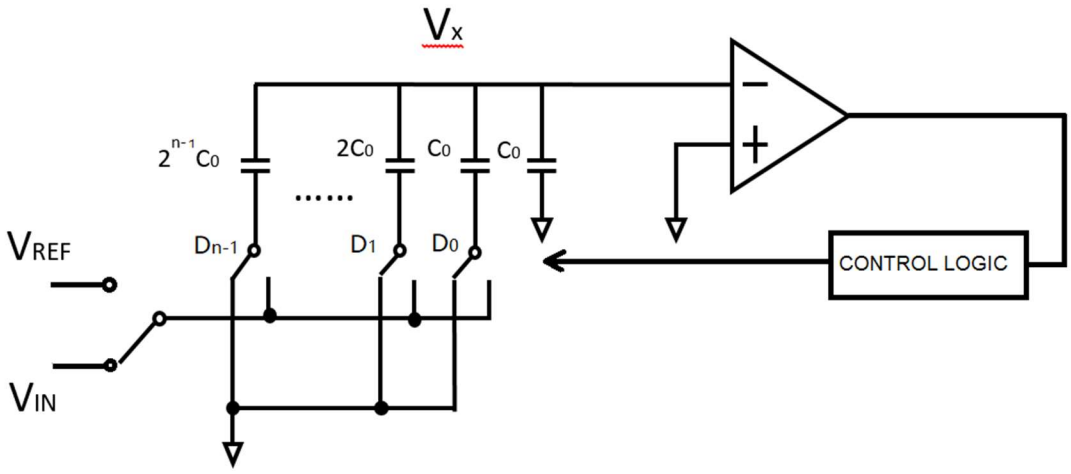


Figure 2.4 N-bit charge-redistribution SAR ADC circuit [7].

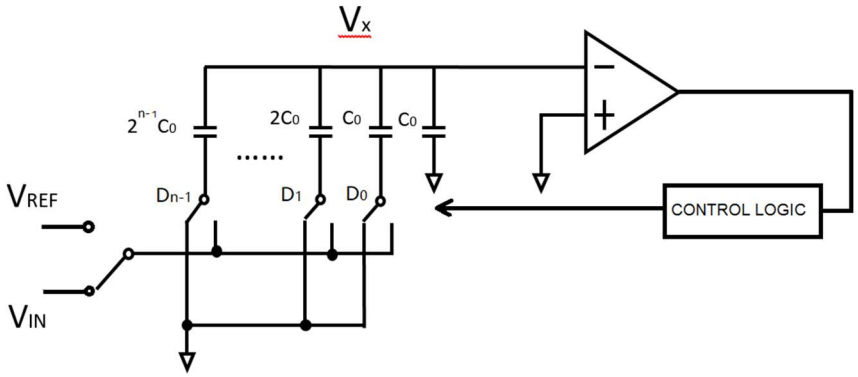
Fig. 2.4 shows the charge–redistribution SAR ADC. The first step of the circuit operation is completely discharging the capacitor array by connecting all the capacitors to GND. Next, all the capacitors in this array are switched to the input signal V_{IN}. In the third step, the capacitors are then switched to GND so that this charge is applied across the comparator's input, creating a comparator input voltage V_x equal to $-V_{IN}$. Then, the actual conversion process proceeds. First, the MSB capacitor is switched to V_{REF}, which corresponds to the full-scale range of the ADC. Due to the binary-weighting of the array

the MSB capacitor forms a 1:1 charge divider with the rest of the array. Thus, the comparator input V_x is now $-V_{IN} + V_{REF}/2$. Subsequently, if V_{IN} is greater than $V_{REF}/2$ then the comparator outputs a digital 1 as the MSB, otherwise it outputs a digital 0 as the MSB. When Vo = 1, the comparator input voltage will remain at $-V_{IN} + V_{REF}/2$, and if Vo = 0, the MSB capacitor will be connected to ground, which making the comparator input voltage V_x to $-V_{IN.}$ Each capacitor is tested in the same manner until the comparator input voltage converges to the threshold voltage 0, or at least as close as possible given the resolution of the DAC [1-2].

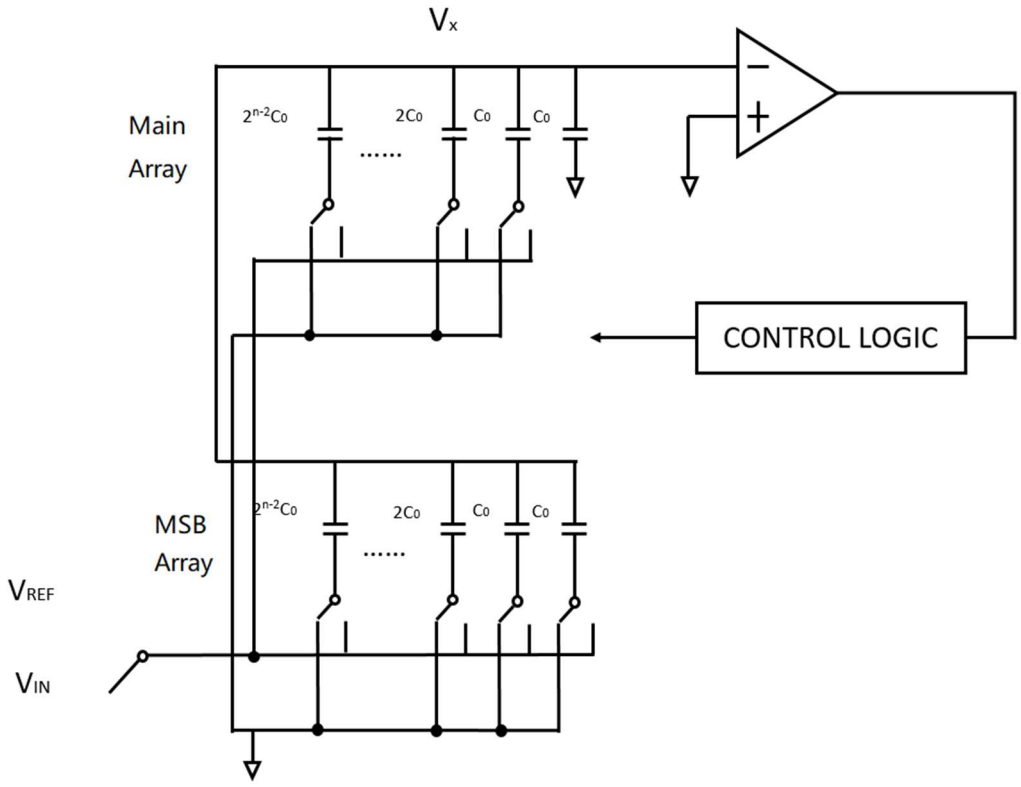
2.3 Split capacitor SAR ADC architecture

In order to reduce the power consumption of SAR ADCs, people made effort on researches and found different ways to reach the goal. Among them the capacitor splitting theory is an outstanding one. By using the capacitor split technique, the energy could be saved over 30% compared to the conventional switching technique [7].

Split capacitor SAR ADC architecture splits the MSB capacitor into N-1 binary weighted sub-capacitors. As a result, the MSB capacitor has been split into an identical copy of the rest of the array. Fig. 2.5 presents an N-bit split capacitor SAR ADC circuit, which shows how the MSB capacitor is split into N-1 binary weighted sub-capacitors [7].



(a)



(b)

Figure 2.5 N-bit split capacitor SAR ADC circuit (a) A conventional N-bit CR-SAR ADC; (b) A N-bit split capacitor array CR-SAR-ADC [7].

The first cycle of the N-bit split capacitor SAR ADC operates similar to the conventional SAR ADC, where the input is sampled. The split capacitor array operation is similar to a conventional charge-redistribution SAR ADC during up operation and differs during down operation. The up operation refers to charging the largest capacitor in the main array when the input voltage is greater than the previous node voltage. The down transition represents discharging the largest capacitor in the MSB array when the input voltage is lesser than previous node voltage. For i^{th} up transitions, the i^{th} capacitor in the main array should be switched to V_{ref}, and for the down transitions, i^{th} capacitor in the MSB array should be switched to ground.

In order to better understand the operation by capacitor splitting technique, an example of a 2-bit ADC with capacitor splitting technique is presented below. In Fig. 2.6, V_x represents the node voltage, V_{in} and V_{ref} are the analog input signal and voltage reference respectively, C_0 denote the unit capacitor and MSB capacitor C_2 which is split into $C_{2,1}$ and $C_{2,2}$ respectively. In this figure from (a) to (e) presents the operation flow of a 2-bit split capacitor SAR ADC circuit [7].

Charge redistribution based successive approximation ADC has the advantage of low power operation since the split capacitor array approach avoids throwing away the charge that has been stored on to the array by charge re-utilization during the down transition. With this skill, more than 30% energy could be saved.

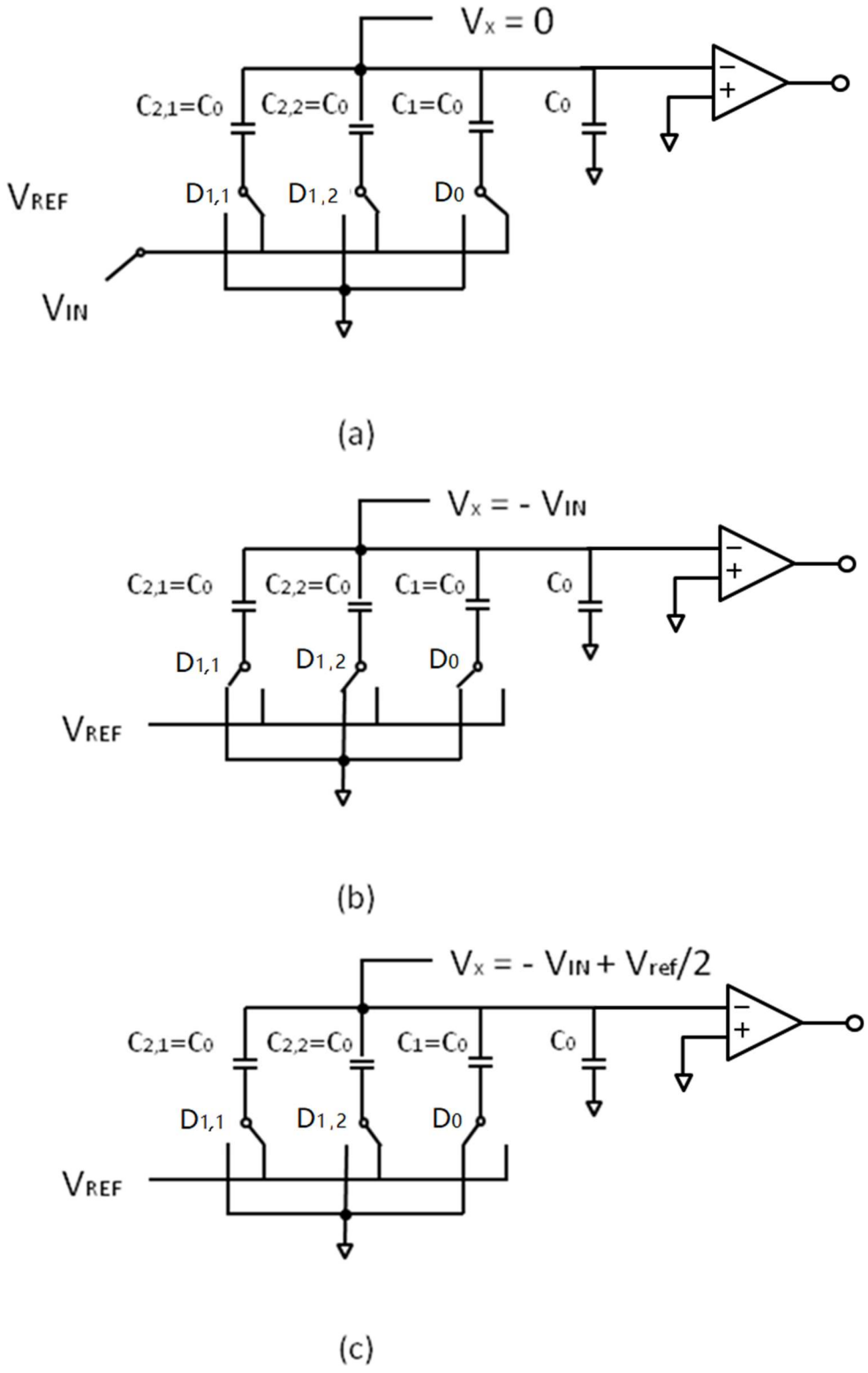
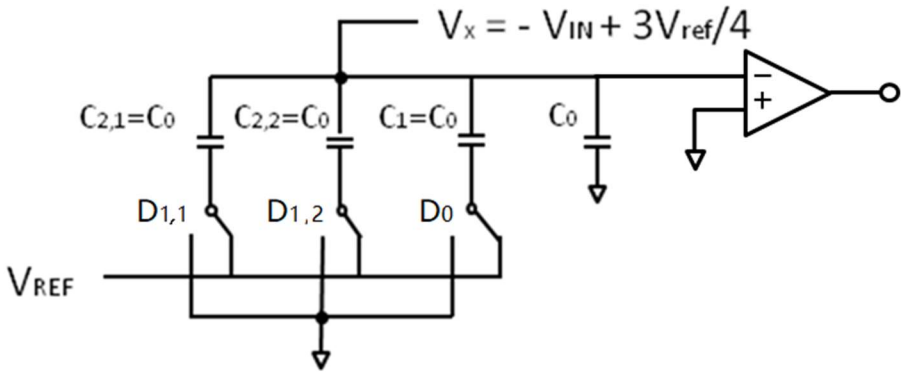
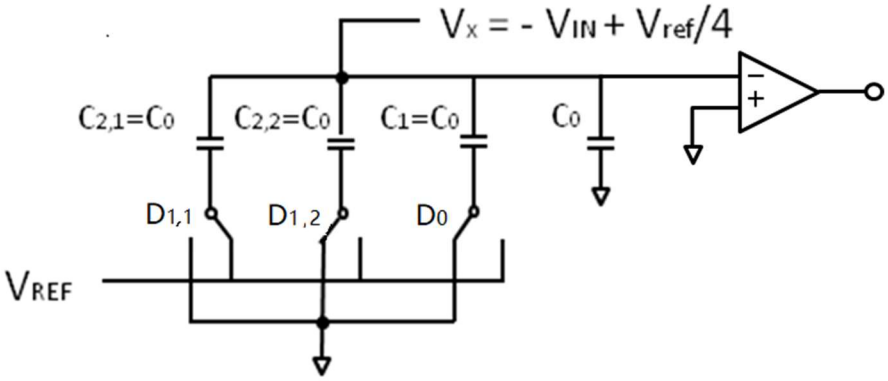


Figure 2.6 A 2-bit split capacitor SAR ADC circuit example [7].

(a) Discharge capacitor array; (b) Sampling V_{in} to capacitor array; (c) MSB operation.



(d)



(e)

Figure 2.6 A 2-bit split capacitor SAR ADC circuit example [7], continued.

(d) 1st up transition if MSB = 1; (e) 1st down transition if MSB = 0

2.4 2-bit per cycle SAR ADC architecture

In this section, the 2-bit per cycle SAR ADC architecture is presented. As an improved architecture of conventional SAR ADC, the 2-bit per cycle method doubles the ADC operating speed which can overcome the speed limitations of the conventional SAR

ADC. However, based on this method, the power consumption is increased. The block diagram of the conventional 2-bit/step SAR ADC is shown in Fig. 2.7 [5].

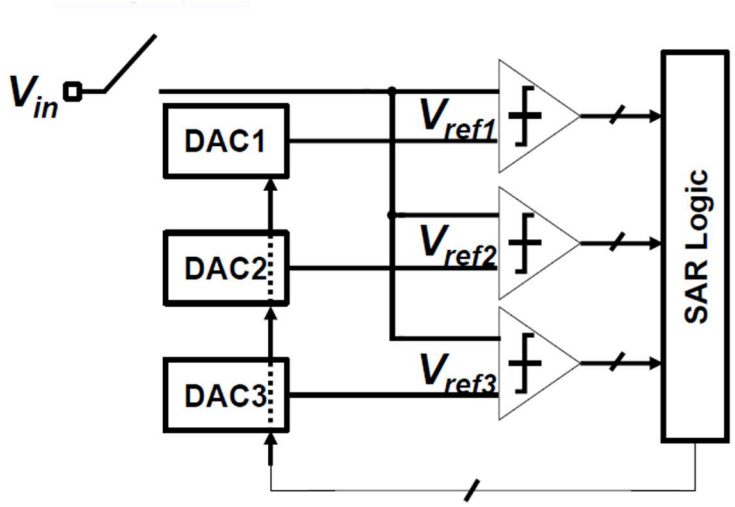


Figure 2.7 Conventional 2-bit per cycle SAR ADC block diagram [5].

In a 2-bit per cycle SAR ADC architecture, a multiple voltage generating DAC is required which takes N/2 clock cycles to convert N-bits. As presented in Fig. 2.7, every clock cycle 2 bits will be generated. In Fig. 2.8, a three-reference-voltage generating scheme is presented [5].

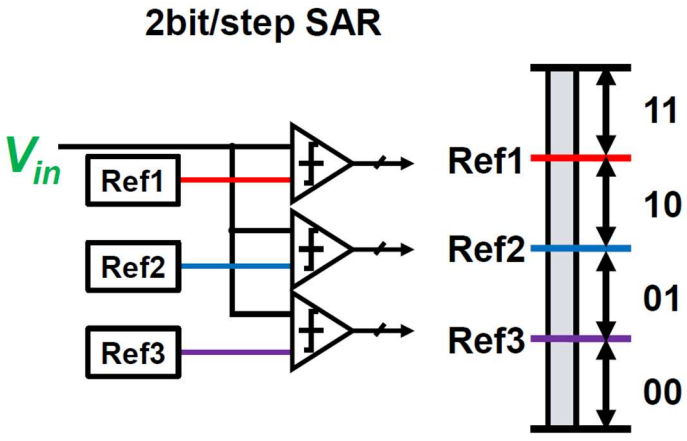


Figure 2.8 2-bit per cycle SAR ADC reference voltage generating scheme [5].

In the first conversion cycle, depending on the SAR ADC input voltage range, three reference voltages separate this range in to four equal sub-ranges. In this voltage range, four sub-ranges represent 00, 01, 10, 11, respectively, and which indicate the first two digital output code of the SAR ADC. In the following cycle, according to the sub-range V_{in} belongs in during cycle 1, three new reference voltages are generated by the DAC; they separate the sub-range which the input voltage was in during first cycle into four more sub-ranges, so that we can find out the following 2-bit digital output codes. According to this method, finally the D_0 to D_{N-1} is the output digital codes generated and the analog to digital conversion is completed.

In Fig. 2.9, a 2-bit per cycle 4-bit SAR ADC is presented as an example. As the input voltage range is from 0V to 1V, and V_{in} is set at 0.6V, during the first cycle the range from 0V to 1V is separate in to four sub-range by the three reference voltages $^{12}/_{16}$V, $^{8}/_{16}$V, and $^{4}/_{16}$V. Since V_{in} = 0.6V belongs in the sub-range from $^{12}/_{16}$V (0.75V) to $^{8}/_{16}$V (0.5V) and since this sub-range corresponds to the digital output code 10, 10 is the first two digital output codes. In the second cycle, we divide the sub-range $^{12}/_{16}$ V to $^{8}/_{16}$V into four more sub-ranges by three reference voltages $^{11}/_{16}$ V, $^{10}/_{16}$V and $^{9}/_{16}$V, since V_{in} = 0.6V belongs in the sub-range from $^{10}/_{16}$ V (0.625V) to $^{9}/_{16}$V (0.5625V) and since this sub-range corresponds to the digital output code 01, 01 is the last two digital output codes.

While the 1-bit per cycle SAR ADC generates only one reference voltage in each cycle, the 2-bit per cycle SAR ADC uses multiple DACs to generate three reference voltages and which are needed for a 2-bit conversion. As a result, the N bit SAR clock

cycle is cut down to N/2. The demerit of the 2-bit per cycle method is the power efficiency which drops significantly. Since three DACs and comparators are required, they consume 1.5 times as much power compared to the 1-bit per cycle SAR ADC. Furthermore, using multiple DACs will lead to area increase when designing high resolution ADC [5].

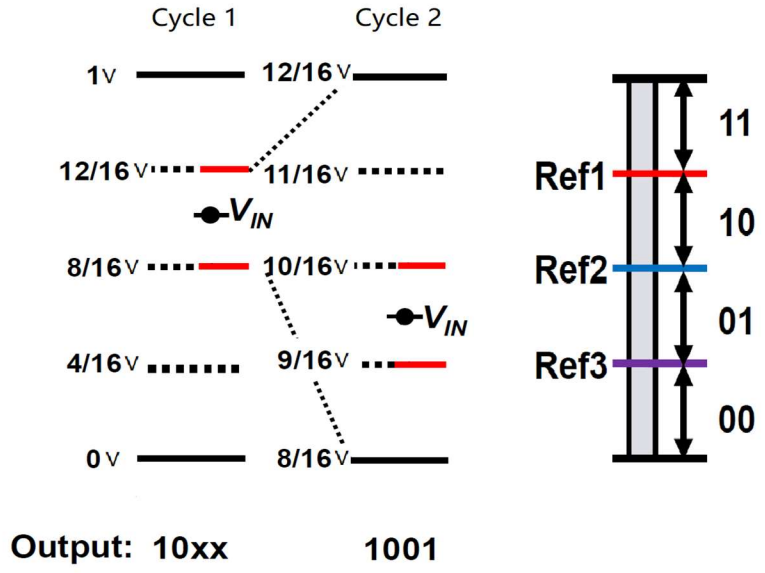


Figure 2.9 An example of 2-bit per cycle 4-bit SAR ADC [5].

In this chapter, the basic concept of the SAR ADC and the circuit block diagram are covered. In addition, three different SAR ADC architectures including the charge redistribution SAR ADC, split capacitor SAR ADC, and 2-bit per cycle SAR ADC have been reviewed.

CHAPTER III

PROPOSED SAR ADC ARCHITECTURE

This chapter presents the proposed SAR-ADC architecture. The basic concept of this design is presented, followed by the complete architecture details and flow graph. The single-capacitor DAC is realized by partially charging or discharging the sampling capacitor with a DC reference current, which will lead to significant capacitor area reduction. The capacitor will be charged or discharged with a certain amount of voltage, which will be added to or subtracted from the pre-charged voltage.

The concept of the single-capacitor DAC and the proposed SAR ADC architecture is described in 3.1 and 3.2. In 3.3, the SAR ADC operation including the flow graph is presented.

3.1 Single-capacitor DAC

The single-capacitor pulse width to analog converter based DAC consists of a DC reference current, switch, and sampling capacitor. Fig. 3.1 shows the basic concept of the DAC which performs the charge and discharge operation. The capacitor is assumed to be pre-charged with voltage V_P, where T_C and T_D indicate the charge and discharge period, respectively. As a result, the voltage across the capacitor for the charge and discharge case are given as

$$V_O = \frac{I_{REF} \cdot T_C}{C} - V_P \quad (\text{Charge})$$

$$V_O = -\frac{I_{REF} \cdot T_D}{C} + V_P \quad (\text{Discharge})$$

As shown from equations above, the voltage across the capacitor can be arbitrary changed by controlling the charge or discharge period. Furthermore, the charge operation adds a voltage to V_P whereas the discharge operation subtracts a voltage from V_P. Therefore, this simple circuit can be used as a DAC for SAR ADCs by combining the charge and discharge operation [9].

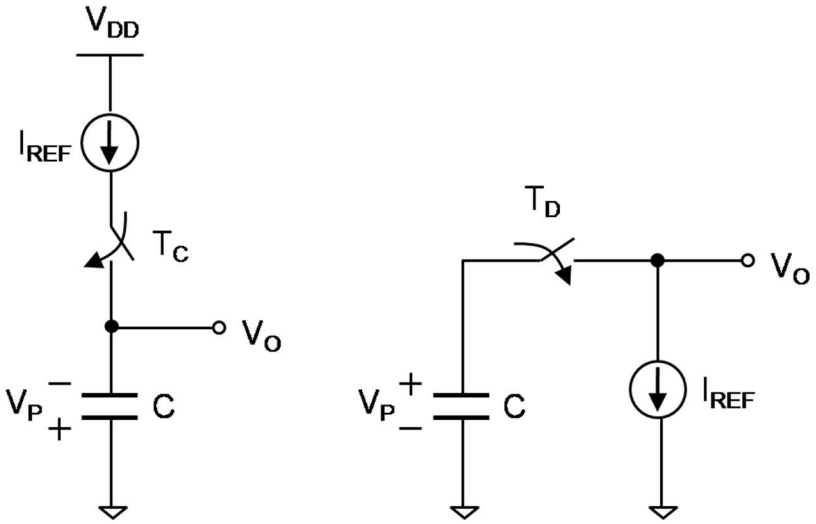


Figure 3.1 Basic concept of the single capacitor DAC [9].

3.2 SAR ADC architecture

Fig. 3.2 shows the proposed SAR ADC architecture which includes the input sampling block, DAC, comparator, and control logic which generates the digital output bits and the switch control signals [9].

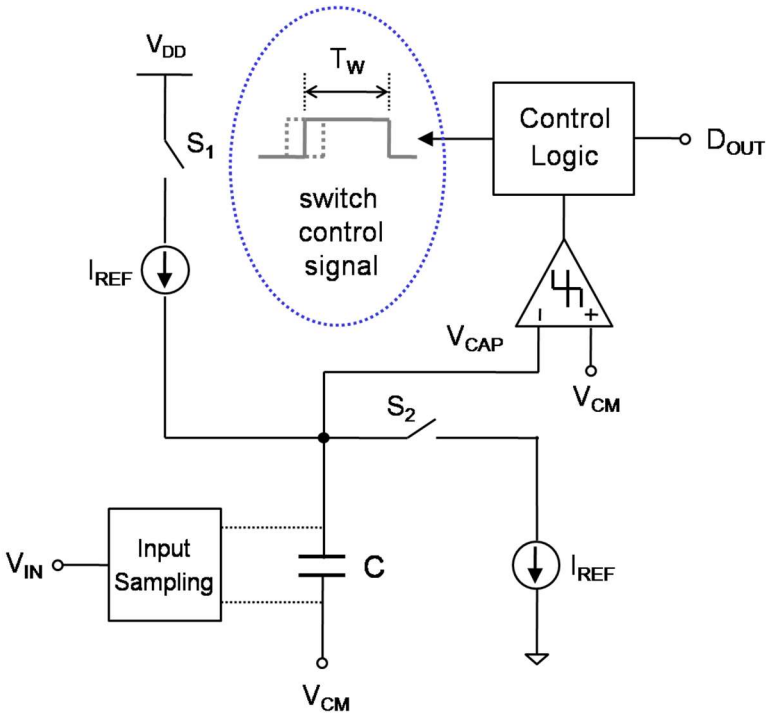


Figure 3.2 SAR ADC architecture [9].

When S_1 and S_2 are all turned off, the ADC performs the input sampling operation. In this case, the input voltage V_{IN} is sampled in capacitor C.

When S_1 is turned on, and S_2 is turned off, this architecture performs the charging operation, where the reference current charges the capacitor and the charge time depends on the switch control signal timing T_W. On the other hand, when S_2 is turned on, and S_1 is turned off, the ADC performs the discharging operation, the top plate of the capacitor connects to

the ground so that the reference current discharges the capacitor and the discharge time depends on the switch control signal timing T_W.

After performing the charging or the discharging operation, the capacitor voltage V_{CAP} is compared with a common voltage V_{CM}. Because V_{CAP} is connected to the negative node of the comparator and V_{CM} is connected to the positive node the comparator, when V_{CAP} is larger than V_{CM}, the comparator output should be low; conversely when V_{CAP} is smaller than V_{CM} the comparator output should be high. The control logic uses the comparator output to determine the right operation sequence (charge or discharge) and the timing for the next conversion cycle [9].

3.3 SAR ADC operation

The operation of an N-bit SAR ADC consists of total (N+2) cycles, where the final cycle is for ADC output latch. Fig. 3.3 shows the SAR ADC flow graph. In the 1st-cycle, the input signal V_{IN} is sampled and the capacitor is pre-charged. The remaining N cycles perform the bit cycling where the digital output is generated in each cycle. During bit cycling, in addition to generating the digital output bits, the capacitor will be charged or discharged with a certain amount of voltage which will be added to or subtracted from the pre-charged voltage. At the same time, the capacitor voltage V_{CAP} will be compared with a threshold level V_{CM} to determine the digital output bit. However, during the 2nd-cycle (1st-bit cycling), it is not required to charge or discharge the capacitor – only V_{CAP} is compared with V_{CM} to generate the digital output which is the MSB bit. In addition, for each bit cycling (excluding the 1st), the charge or discharge operation is determined by the digital output bit of the previous cycle. That is, if the previous cycle output is high which means the capacitor

pre-charge voltage V_{CAP} is less than the V_{CM}, charging operation is performed, and vice versa [9].

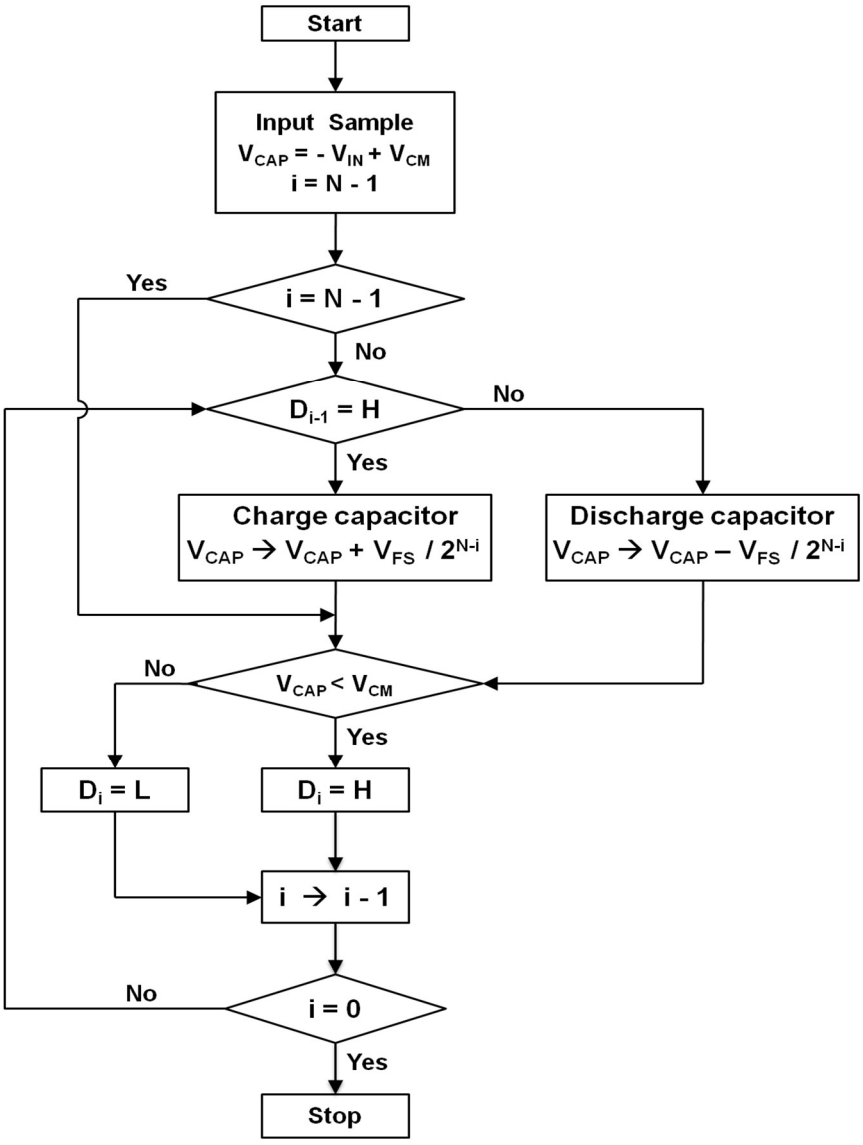


Figure 3.3 SAR ADC flow graph [9].

The basic concept, architecture, and operation of the proposed single-capacitor SAR ADC have been described in this chapter. The actual circuit implementation and simulation results of the proposed SAR ADC including DNL and INL plots will be shown in the next chapter.

CHAPTER IV

CIRCUIT IMPLEMENTATION

This chapter presents the circuit implementation of the proposed SAR-ADC. The proposed SAR ADC was designed using CMOS 0.35μm technology, where the circuit is presented in 4.1, and the transient simulation results are discussed in 4.2, and DNL and INL plots are shown in 4.3.

4.1 Proposed SAR ADC Circuit

Fig. 4.1 shows the transistor level circuit of the analog portion which includes the reference current generator, charge/discharge current source, input sampling block, and comparator. The reference amplifier is realized using a differential pair with NMOS input devices, and the comparator is built using a differential pair with NMOS input devices followed by an S-R latch. The proposed SAR ADC was designed using CMOS 0.35μm technology with supply voltage of 3.3V.

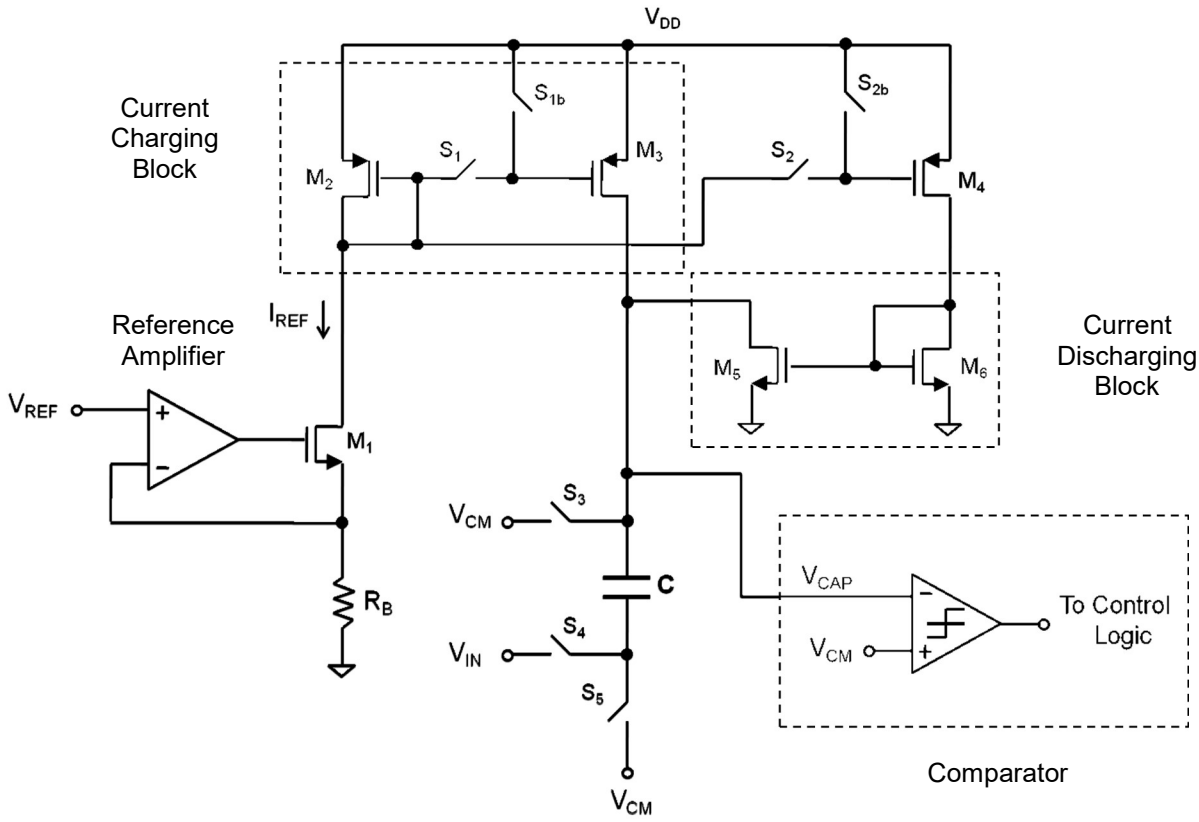


Figure 4.1 Proposed SAR ADC circuit [9].

The digital control block that generates the control pulse for all the switches $S_1 \sim S_5$, and the digital output bits of the SAR ADC, consists of a counter, flip-flops, and switch control logic. The reference current generator generates a reference current $I_{REF} = V_{REF}/R_B$, where V_{REF} and R_B was set to 1V and 250kΩ, respectively. This makes a 4uA current which is copied by current mirrors M_2 - M_3 and M_2 - M_5 to charge and discharge the capacitor C. In addition, both PMOS and NMOS current mirrors used minimum width, long channel devices to improve current matching and minimize the current variation with V_{CAP} level change. The charge operation is enabled by switch S_1 whereas the discharge operation is enabled by switch S_2. Switches S_{1b} and S_{2b} simply use the inverted version of the control signals for S_1 and S_2. This switching scheme which directly controls the current mirror

transistors was employed to reduce the switch channel charge injection, instead of placing the switch at the top plate of C. For better performance, CMOS transmission gates with minimum sized PMOS and NMOS transistors were used for switches S_1 and S_2. Switches S_{1b} and S_{2b} are simply realized with minimum sized PMOS transistors.

The input sampling switch S_3 and S_4 are only on for the 1st conversion cycle (input sampling). The input signal V_{IN} is applied to the bottom plate of the capacitor, where C is pre-change relative to V_{CM} (0-2V). In addition, switch S_5 is always on except for the input sampling cycle, which connects the bottom plate of C to V_{CM}. For the remaining cycles, excluding cycle-2, C is either charge or discharged depending on the digital output bit of the previous cycle. In case the previous cycle output bit is H, C will be charged, since $V_{CAP} < V_{CM}$ (according to the flow graph, Fig. 3.3). Similarly, C will be discharged in case the previous cycle output bit is L, since $V_{CAP} > V_{CM}$. Table 1 shows the summary of the switch status during each conversion cycle. Noticing N is the ADC resolution with output bits of $D_{N-1} \sim D_0$, cycle-1 performs input sampling, cycles-2 to (N+1) are for bit cycling, and cycle-(N+2) is the extra cycle for ADC output latch.

Table 1. Each switch status for each conversion cycle

Switch	Conversion Cycle			
	Cycle - 1	Cycle - 2	Cycle - i (i = 3 ~ N+1)	Cycle - (N+2)
S1	Off	Off	On (D_{N-i+2} = H) Off (D_{N-i+2} = L)	Off
S2	Off	Off	Off (D_{N-i+2} = H) On (D_{N-i+2} = L)	Off
S3, S4	On	Off	Off	Off
S5	Off	On	On	On

4.2 Transient Simulation Results

The operation of the 6-bit SAR ADC is verified through circuit level simulations. Fig. 4.2 shows the switch S_1 and S_2 control signals and V_{CAP} waveforms. The left half is for V_{IN} of 2.65V (maximum input level) and the right half is for V_{IN} of 0.65V (minimum input level). For V_{IN} = 2.65V, V_{CAP} level becomes 0.65V ($-V_{IN} + V_{CM}$), during the input sampling cycle, and C is charged for each cycle. Therefore, only switch S_1 is active and V_{CAP} level gradually increases in each cycle.

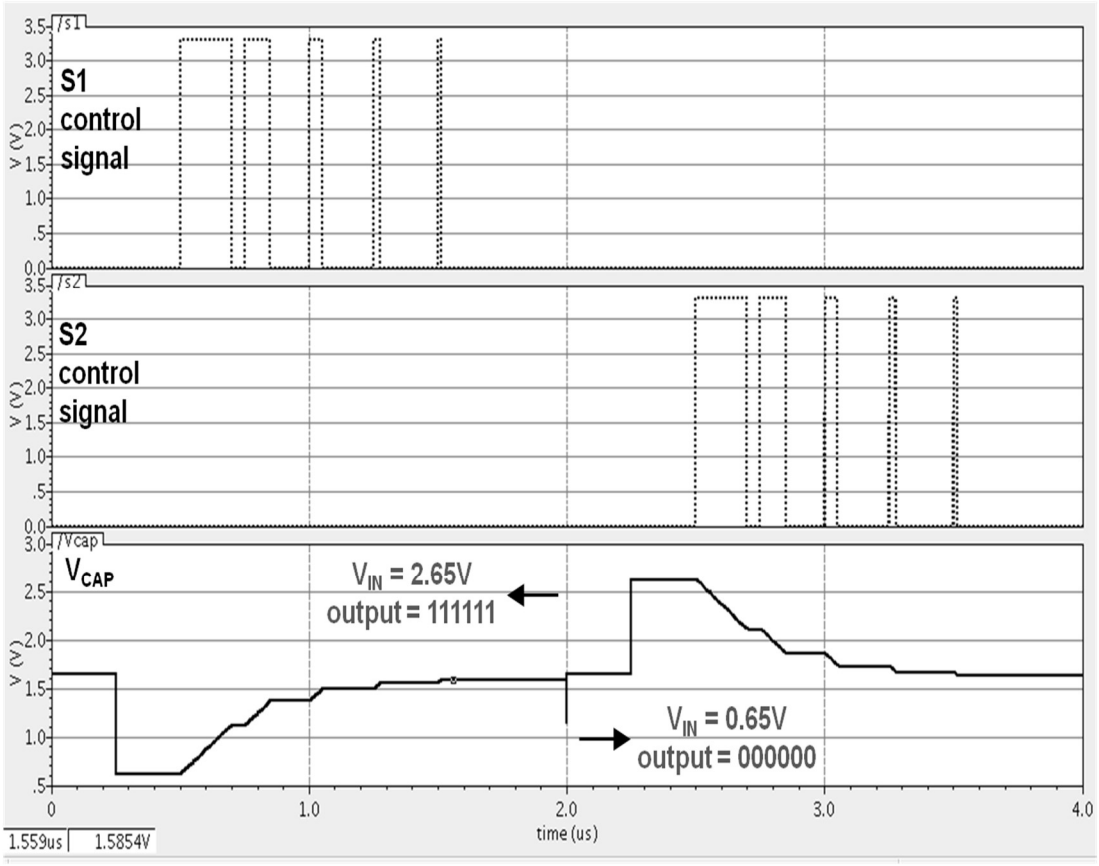


Figure 4.2 Simulation waveforms for S_1, S_2 control signals and V_{CAP} [9].

In addition, it is shown that V_{CAP} changes proportional to the switch control signal pulse width which reduces to half for each cycle. This will lead to a digital output of 111111 which is latched at the 8th cycle. On the other hand, for V_{IN} = 0.65V, only switch S_2 is on, and C is discharge for each cycle. As a result, V_{CAP} level decreases proportional to the switch S_2 control signal pulse width. This will lead to a digital output of 000000.

Since the proposed ADC is a 6-bit ADC, the output range is from 000000 to 111111, so there should be 64 output levels. In order to verify the ADC output levels, we convert the digital output signals into analog signals, which leads to 64 distinct voltage levels. Fig. 4.3 shows the analog voltages corresponding to the ADC output levels. As shown, the analog voltage corresponding to the digital output codes from 000000 to 111111, has a range from 0.65V to 2.65V, which is identical to the ADC input range.

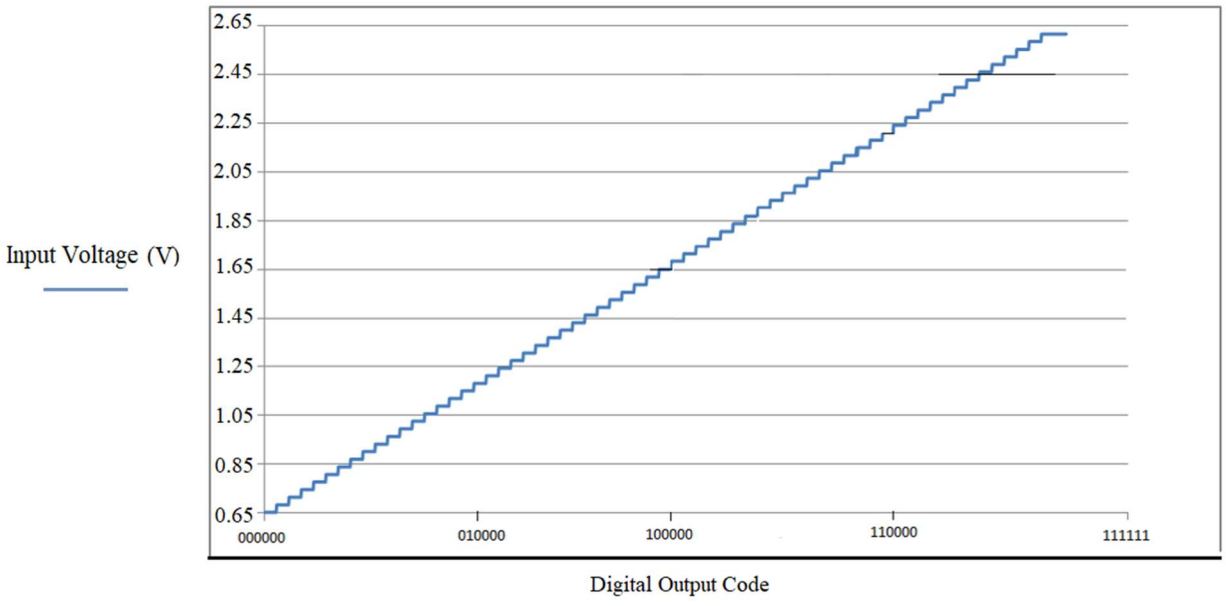


Figure 4.3 Simulation waveform for output analog voltage.

4.3 INL and DNL Plots

INL and DNL are crucial performance characteristics for any ADC. Fig. 4.4 and 4.5 show the DNL and INL plot for proposed SAR ADC architecture. The maximum DNL and INL values with 5% charging and discharging current mismatch are 0.42LSB and 0.32LSB, respectively. This indicates the proposed SAR ADC can tolerate 5% current mismatch to achieve a 6-bit resolution. However, in order to suppress the current mismatch below 5%, the length of the charging and discharging current mirror transistors (M_2, M_3 AND M_5, M_6 shown in Fig. 4.1) were set to 5 times the minimum length.

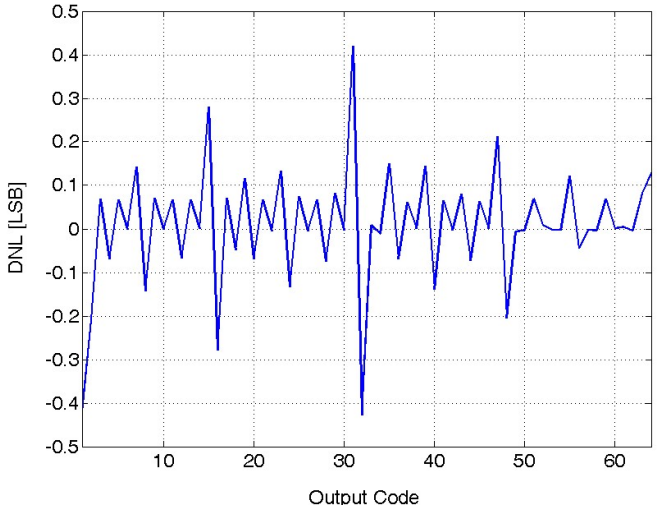


Figure 4.4 DNL plot of proposed architecture [9].

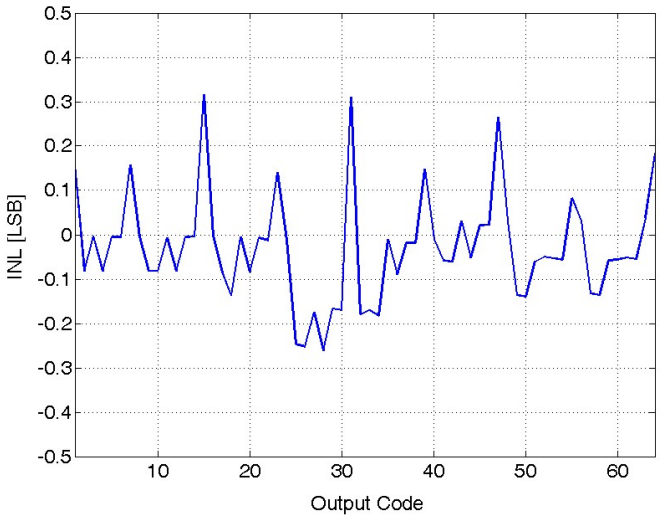


Figure 4.5 INL plot of proposed SAR ADC [9].

The basic operation of the proposed SAR ADC is verified through circuit level simulations. However, in the proposed SAR ADC architecture, the mismatch between the capacitor charge and discharge current can degrade the performance of the proposed ADC, since it causes un-even V_{CAP} levels for the same switch control pulse width. The effect of other ADC non-idealities are further analyzed in chapter 5.

CHAPTER V

THE EFFECT OF NON-IDEALITIES

This chapter explores the effects of proposed SAR ADC non-idealities. In order to analyze the effect of each non-ideality, the ADC circuit was simulated using Cadence Design Systems by adding different amount of error for capacitance variation, current mirror mismatch and comparator offset, where the DNL and INL characteristics are measured.

5.1 Capacitance variation

A SAR ADC commonly suffers from capacitance variation, which is the deviation between the ideal capacitance value. By changing the capacitor value of the proposed SAR ADC design, we can figure out how capacitance variation affects the performance of the proposed SAR ADC. Fig. 5.1 shows the maximum DNL and INL by adding variation to the single-capacitor C, in increments of 1%, 5%, and 10%.

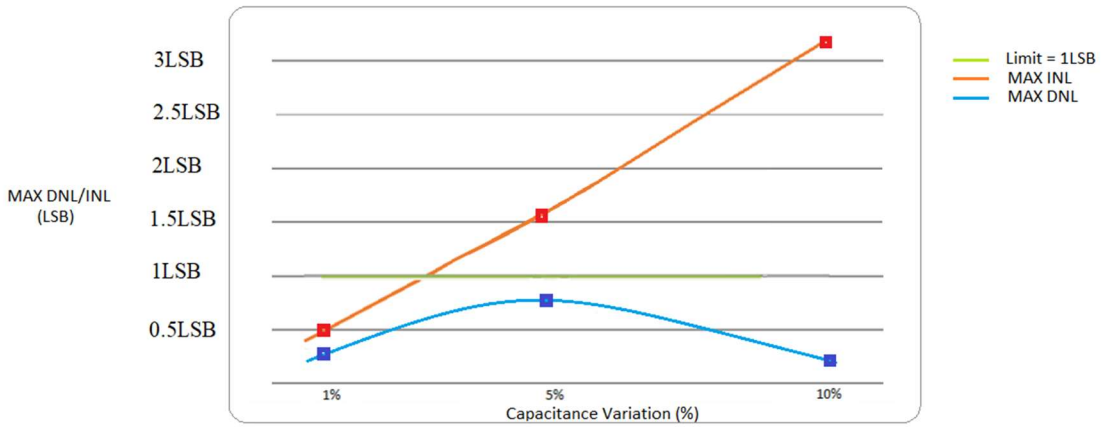


Figure 5.1 The influence of capacitance variation on DNL and INL.

Results show that INL suffers a lot from capacitor variation, which reaches 3LSB when we add 10% error to the capacitor. As a general rule, the error is too much if the DNL or INL exceed 1LSB. A value of 1LSB or greater implies that an output code of the ADC is missing. As shown in Fig. 5.1, the maximum acceptable INL error is seen for capacitor error of about 2.5%. If the circuit do not stray beyond this limit, the INL error would increase beyond 1LSB.

5.2 Current mirror mismatch

In the proposed SAR ADC circuit, two current mirrors are used to copy the bias current. As shown in Fig. 4.1, current I_1 is copied for charging the capacitor while the other I_2 is copied for discharging the capacitor. Current mirror mismatch may result in I_1 and I_2 mismatch, which will lead to uneven charging and discharging of C. Fig. 5.2 shows the maximum DNL and INL, by changing the mismatch between the current I_1 and I_2, in increments of 1%, 5%, and 10%.

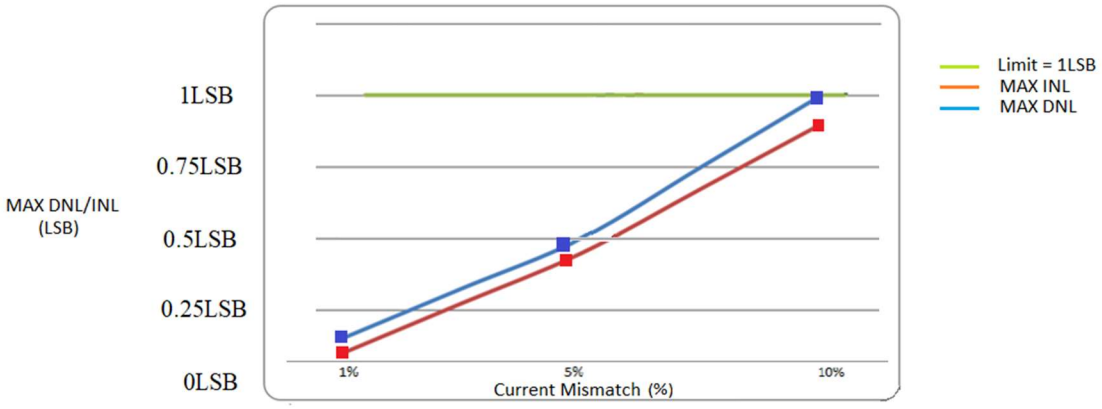


Figure 5.2 The influence of current mirror mismatch on DNL and INL.

Results show that DNL reaches 1 LSB when we add 10% mismatch between currents I_1 and I_2. As show in Fig. 5.2, the maximum error allowed for current mirror mismatch is about 10%. If the circuit were to stray beyond this limit, the DNL would increase beyond 1LSB.

5.3 Comparator offset

The input offset voltage of a comparator can change the output from one logic level to the other. It can be caused by device mismatch or may be inherent to the design of a comparator. In the proposed design a comparator is used in the circuit. Fig. 5.3 shows the maximum DNL and INL by changing the comparator offset for 1mv, 5mv and 10mv.

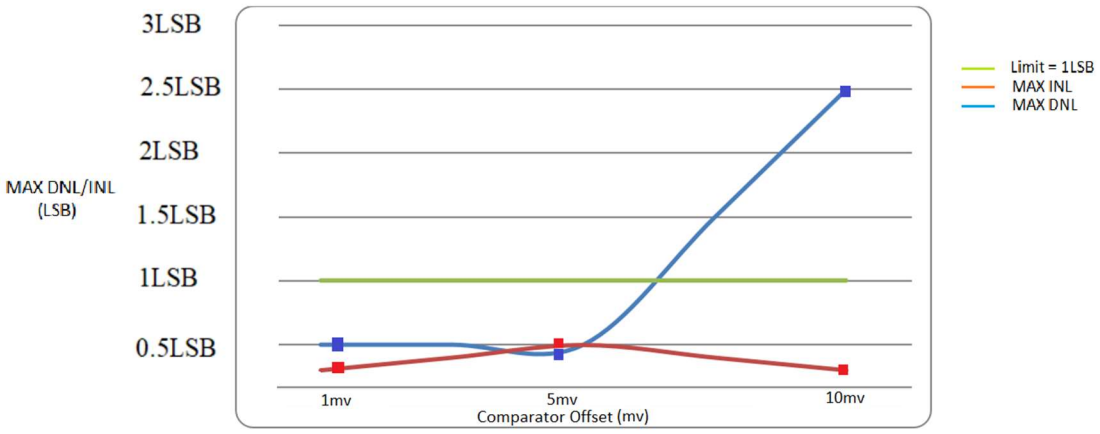


Figure 5.3 The influence of comparator offset on DNL and INL.

Result shows that DNL suffers a lot from comparator offset error, which reaches 2.5LSB with comparator offset of 10mv. As show in Fig. 5.3 the maximum error allowed for comparator offset error is about 7mv. If the circuit were to stray beyond this limit, the DNL would increase beyond 1LSB.

5.4 Interpretation of the results

So far, we analyzed the errors which may influence the performance of the proposed SAR ADC. In order to keep the proposed single-capacitor SAR ADC working properly, each component error should not exceed the limit.

To summarize, the maximum error allowed for each component in the single-capacitor-based SAR ADC is shown in Table 2. If the values go beyond these limits, a voltage level is lost and there are certain analog voltages that the circuit will not convert correctly to the digital output code.

Table 2. Maximum errors for each component

Max capacitance variation	2.5%
Maximum current mirror error	5%
Maximum comparator offset error	7mv

The single-capacitor-based SAR ADC is a valid circuit to convert analog voltages to a digital representation. Any fabricated circuit will have errors that will affect the performance. The proposed design, however, is robust enough to support some internal variation of errors and still operate within the limits without missing any digital output codes.

5.5 Performance comparison with other SAR ADCs

The core area of the proposed SAR ADC is obtained by estimating the area of each circuit block including the comparator, capacitor, reference amplifier, resistor, digital logic, and switches. The area of the circuit blocks are estimated by considering the component size and the inter-connection area of the layout. The floorplan of the proposed SAR ADC based on the estimated area is shown in Fig. 5.4, and the estimated area of each circuit block is shown in Table 3. The estimated core area of the proposed ADC is 0.006 mm^2.

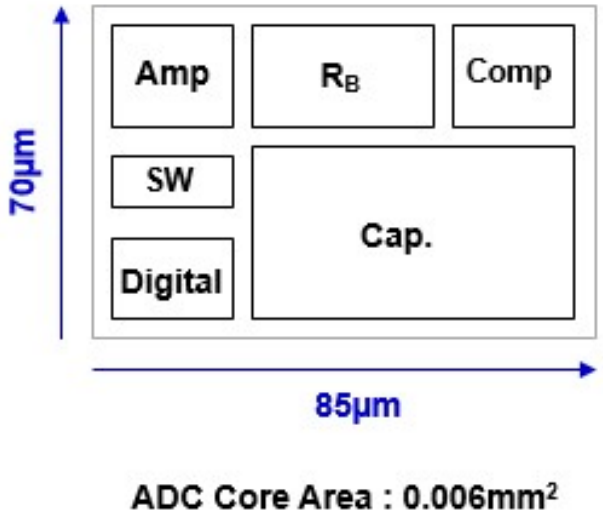


Figure 5.4 Circuit block layout and area estimation

Table 3. Estimated area of the proposed SAR ADC

Circuit block	Area (mm^2)
Reference Amplifier	0.0007
Capacitor	0.0028
Comparator	0.0007
Digital block	0.0005
R_B	0.001
Switches	0.0003
Total	0.006

The power consumption of the proposed ADC is obtained from the circuit simulation, where it is averaged over the conversion period of 500ns (this corresponds to 500kS/s conversion rate), which showed 22.6 μW. Table 4 shows the power consumption of the ADC broken down into each sub-block. In order to reduce the power consumption

of the ADC, the comparator and the reference amplifier power was minimized, since the two blocks consume most of the ADC power. The power consumption of the reference amplifier and comparator are determined by the tail bias current of the differential pairs. For the proposed design, the tail bias currents were set to 1µA and 2µA for the reference amplifier and comparator, respectively. This is the minimum value to satisfy the bandwidth requirement of the reference amplifier and the comparator, which leads to minimum power for both circuit blocks.

Table 4. Power consumption of the proposed SAR ADC

Circuit block	Power consumption (µW)
Comparator	10
Reference Amplifier	7
DAC	2.6
Digital block	3
Total	22.6

Table 5 shows the performance of the proposed SAR ADC compared to other SAR ADCs with similar resolution and speed. As shown in Table 5, the proposed design has the smallest ADC area which is due to the single capacitor switching scheme. The other three ADCs have larger area due to the multiple capacitors in their DAC capacitor array. The power consumption of the proposed SAR ADC is not the lowest compare to other designs' power consumption. However, by using the single capacitor switching

scheme, the power consumption of proposed design is also significantly reduced, which is less than the power consumption of Ref. [11] and Ref. [12].

Table 5. Performance comparison with other SAR ADCs [10-12]

Ref.	[10]	[11]	[12]	This work
Technology	CMOS 0.18µm	CMOS 0.18µm	CMOS 0.18µm	CMOS 0.35µm
Resolution (bits)	8	8	10	6
Speed	500kS/s	370kS/s	500kS/s	500kS/s
Area (mm^2)	0.08	0.073	0.23	0.006
Power (µW)	7.75	32	42	22.6

In the proposed design, we reached our design goal to build a SAR ADC with power consumption less than 30µW and core area less than 0.01 mm^2. The performance of the proposed SAR ADC makes it stand out from other designs.

CHAPTER VI

CONCLUSION AND FUTURE WORK

In this work, a SAR ADC using single-capacitor pulse width to analog converter based DAC is proposed. With this approach, a SAR ADC can be realized by using a single-capacitor, current source, current mirror, comparator, and control logic which can significantly reduce the circuit area and simplifies the switch control scheme compared to conventional SAR ADCs using capacitor DACs.

The mismatch between the capacitor charge and discharge current can degrade the performance of the proposed ADC, since it causes un-even V_{CAP} levels for the same switch control pulse width. The most critical non-ideality is the charge and discharge current source mismatch. The maximum DNL and INL values with 5% current mismatch are 0.42-LSB and 0.32-LSB, respectively. The power consumption of the ADC core is 22.6μW with estimated area of 0.006mm^2.

Although the feasibility of a 6-bit 500kS/sec ADC is shown in the work, the resolution can be further increased by adding more conversion cycles which require additional switch control signals with different pulse widths. In addition, a current mismatch calibration scheme can be considered for high resolution ADCs.

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