

Partial Sums Computation In Polar Codes Decoding

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Abstract—Polar codes are the first error-correcting codes to provably achieve the channel capacity but with infinite code-lengths. For finite code-lengths the existing decoder architectures are limited in working frequency by the partial sums computation unit. We explain in this paper how the partial sums computation can be seen as a matrix multiplication. Then, an efficient hardware implementation of this product is investigated. It has reduced logic resources and interconnections. Formalized architectures, to compute partial sums and to generate the bits of the generator matrix $\kappa^{\otimes n}$, are presented. The proposed architecture allows removing the multiplexing resources used to assigned to each processing elements the required partial sums.

Index Terms—FEC, polar codes, hardware architecture, successive cancellation decoding

I. INTRODUCTION

POLAR codes [1] are a new class of error correction codes. These linear block codes are proven to achieve the capacity of any symmetric memoryless channel under successive cancellation (SC) decoding [2]. Nevertheless, they require a very large code length ($N = 2^n > 2^{20}$, [1]) in order to actually approach the channel capacity. Consequently, the practical interest of polar codes highly depends on the possibility to design efficient encoder and decoder architectures for large code-lengths.

When implemented in hardware ([3] and [4]), an SC decoder is composed of three main units: the *processing unit* (PU), the *memory unit* (MU) and the *partial sums unit* (PSU) as seen in Fig. 1. The decoded bits, \hat{u}_m , are generated one after the other by the PU which needs (i) Log likelihood ratio (LLR) values (λ) stored in the MU, and (ii) partial sums (S) calculated in the PSU. In SC decoding, the partial sums, which are used to carry on the decoding, are a combination of the previously decoded bits and are updated whenever a bit is decoded.

As shown in previous works [5] and [6], the hardware implementation of SC decoders is constrained by the partial sums computation unit which occupies a major part of the area and limits the maximum working frequency, especially as N grows. In [7], a method to compute partial sums is proposed but the best of our knowledge it has not been implemented. In [8], an efficient partial sum unit architecture was proposed and experimentally validated. However, no formal description of the concept has been given. The purpose of the paper is to bring some analytical contributions to [8]. The proposed formalism could then be used with arbitrary kernels and extended to the structure of [8].

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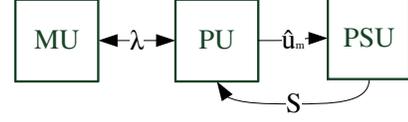


Fig. 1. Typical SC decoder structure.

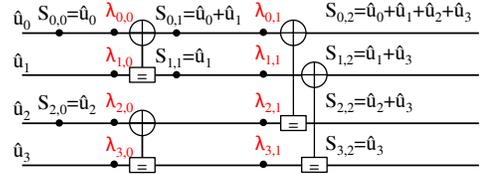


Fig. 2. Factor graph for $N = 4$ polar code.

II. SUCCESSIVE CANCELLATION DECODING

For a code of length ($N = 2^n$), after being sent over the transmission channel, the noisy version Y of the codeword X is received. Each sample y_m is converted into log likelihood ratio (LLR) format. These LLRs are denoted λ_m , with $0 \leq m \leq N - 1$. The decoder successively estimates every bit u_m based on the channel observation vector (λ_0^{N-1}) and the previously estimated bits (\hat{u}_0^{m-1}). In order to estimate each bit u_m , the decoder computes the following LLR value:

$$\lambda_{m,0} = \log \frac{\Pr(y_0^{N-1}, \hat{u}_0^{m-1} | u_m = 0)}{\Pr(y_0^{N-1}, \hat{u}_0^{m-1} | u_m = 1)}. \quad (1)$$

The estimated bit \hat{u}_m is calculated based on the following rule:

$$\hat{u}_m = \begin{cases} 0 & \text{if } \lambda_{m,0} > 0 \\ 1 & \text{otherwise.} \end{cases} \quad (2)$$

As proposed by Arkan in [1], the factor graph representation of polar codes can be used to efficiently compute the $\lambda_{m,0}$. For a code of length ($N = 2^n$), the associated factor graph has n columns and N rows. SC decoding can be seen as an instance of belief propagation decoding where LLRs are propagated on the factor graph of the code with a particular scheduling. In SC decoding, bits \hat{u}_m are processed sequentially and the decision is then fed back into the graph for the decoding of subsequent bits. In Fig. 3, the decoding on the factor graph of a simple $N = 2$ polar code is represented. The graph is composed of a check node (CN or \oplus) and a variable node (VN or \equiv). In

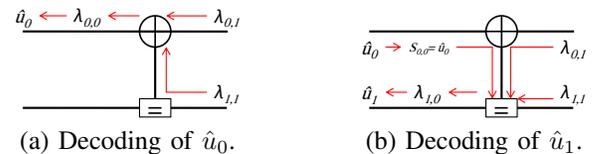


Fig. 3. $N = 2$ polar code decoding example.

general, the decoder successively estimates the bits \hat{u}_m from the computation of LLRs of the indexed edges. The LLR of edge (m, q) is computed such as:

$$\lambda_{m,q} = \begin{cases} f(\lambda_{m,q+1}, \lambda_{m+2^q,q+1}) & \text{if } B(m, q) = 0 \\ g(\lambda_{m-2^q,q+1}, \lambda_{m,q+1}, S_{m-2^q,q}) & \text{if } B(m, q) = 1, \end{cases} \quad (3)$$

with:

$$\begin{cases} f(a, b) & = \text{sgn}(ab) \times \min(|a|, |b|) \\ g(a, b, s) & = b \oplus (-1)^s a. \end{cases} \quad (4)$$

where $B(m, q) \equiv \lfloor \frac{m}{2^q} \rfloor \bmod 2$, $0 \leq m < N$ and $0 \leq q < n$. $S_{m,q}$ represents the *partial sum*, located at the m^{th} row and q^{th} column of the factor graph. It corresponds to the propagation of decisions back into the factor graph. The partial sum set is denoted

$$\mathcal{S} = \{S_{m,q} | m \in \llbracket 0; N-1 \rrbracket, q \in \llbracket 0; n \rrbracket\}.$$

The elements of the partial sum set \mathcal{S} are not all used during the SC decoding, only those such as $B(m, q) = 0$. For example $S_{2,1} = \hat{u}_2 + \hat{u}_3$ is updated two times, when \hat{u}_2 and \hat{u}_3 are generated by the PU.

III. FROM MATRIX PRODUCT TO REGISTER-BASED ARCHITECTURE

A. Matrix product representation

We now wish to prove that the set composed of the bits of $P_n(t)$, for $0 \leq t < N$, contains all the elements of the set \mathcal{S} . Let us define the proposition \mathcal{Q}_n : “All the partial sums of the factor graph are included in the set that contains the values of the vector $P_n(t)$, for $N = 2^n$ and $0 \leq t < N$ ”, for all $n \in \mathbb{N}^*$.

Let us verify that \mathcal{Q}_1 is true.

- when $t = 0$

$$P_1(0) = \hat{U}_1(0) \times \kappa^{\otimes 1} = [\hat{u}_0; 0] \times \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} = [\hat{u}_0; 0] = [p_0(0) p_1(0)].$$

One can notice that $p_0(0) = \hat{u}_0 = S_{0,0}$ as seen in Fig. 2.

- when $t = 1$

$$P_1(1) = \hat{U}_1(1) \times \kappa^{\otimes 1} = [\hat{u}_0; \hat{u}_1] \times \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} = [\hat{u}_0 \oplus \hat{u}_1; \hat{u}_1] = [p_0(1) p_1(1)].$$

One can notice that $p_0(1) = \hat{u}_0 \oplus \hat{u}_1 = S_{1,0} = S_{1,1}$ and $p_1(1) = \hat{u}_1 = S_{0,1}$ as seen in Fig. 2.

The computations of $P_n(t)$ for $t = 0$ and $t = 1$ generate all the required partial sums to decode a code of size $n = 1$. Therefore \mathcal{Q}_1 is true.

Assuming that, for $n \in \mathbb{N}^*$, \mathcal{Q}_n is true, let us show that \mathcal{Q}_{n+1} is true as well. Let us define two N -bit vectors:

- $\hat{V}_n(t) = \hat{u}_0^t$ for $0 \leq t < N - 1$,
- $\hat{W}_n(t) = \hat{u}_N^t$ for $N \leq t < 2N - 1$,

such as $\hat{U}_{n+1}(t) = [\hat{V}_n(t); \hat{W}_n(t)]$. During the decoding of the N first bits, $\hat{U}_{n+1}(t)$ is equivalent to the concatenation of two N -bit vectors $\hat{V}_n(t)$ and 0_N , such that $\hat{U}_{n+1}(t) = [\hat{V}_n(t), 0_N]$.

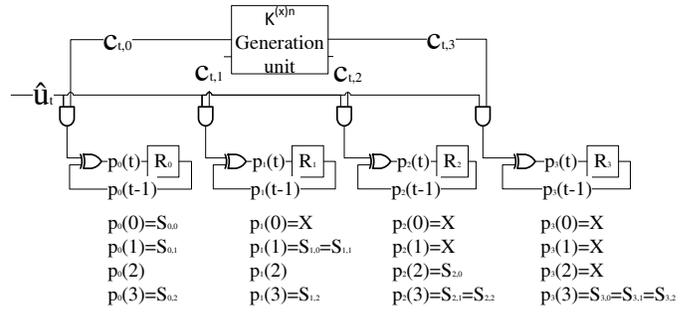


Fig. 4. Register-based architecture for partial sums computation ($N = 4$).

The matrix multiplication between $\hat{U}_{n+1}(t)$ and $\kappa^{\otimes(n+1)} = \begin{bmatrix} \kappa^{\otimes n} & 0 \\ \kappa^{\otimes n} & \kappa^{\otimes n} \end{bmatrix}$, for $t < N$, becomes:

$$P_{n+1}(t) = \hat{U}_{n+1}(t) \times \kappa^{\otimes(n+1)} = [\hat{V}_n(t) \times \kappa^{\otimes n}, 0_N]. \quad (5)$$

Since \mathcal{Q}_n is assumed true, all partial sums of the N first rows and n first columns of the factor graph are located in the N leftmost bits of $P_{n+1}(t)$ ($0 \leq t < N$): $\hat{V}_n(t) \times \kappa^{\otimes n}$.

Similarly, during the decoding of the N last bits, $\hat{U}_{n+1}(t)$ is equivalent to the concatenation of two N -bit vectors $\hat{V}_n = \hat{V}_0^{N-1}$ and $\hat{W}_n(t)$, such that $\hat{U}_{n+1}(t) = [\hat{V}_n, \hat{W}_n(t)]$. The matrix product between $\hat{U}_{n+1}(t)$ and $\kappa^{\otimes(n+1)}$, for $t \geq N$, becomes:

$$P_{n+1}(t) = [(\hat{V}_n \oplus \hat{W}_n(t)) \times \kappa^{\otimes n}, \hat{W}_n(t) \times \kappa^{\otimes n}]. \quad (6)$$

Since \mathcal{Q}_n holds, every partial sum of the N last rows and n first columns of the factor graph is located in the N rightmost bits of the resulting vector ($N \leq t < 2N$): $\hat{W}_n(t) \times \kappa^{\otimes n}$.

Finally, when $t = 2N - 1$ the resulting vector of the product contains the partial sums of the last column of the factor graph. Therefore, \mathcal{Q}_{n+1} is true. As a consequence, every partial sums of the factor graph of a code of size n are generated by computing $P_n(t)$, for $0 \leq t < N$.

B. Register-based structure

$P_n(t)$ is composed of N bits $p_j(t)$, for $0 \leq j < N$. Each bit is the result of a matrix multiplication and can be rewritten as

$$p_j(t) = \sum_{l=0}^t (\hat{u}_l \times c_{l,j}) \pmod{2} \quad \forall (j, t) \in \llbracket 0; N-1 \rrbracket^2$$

where $c_{i,j}$ are the elements of the matrix $\kappa^{\otimes n}$. This sum can be split into two finite sums. The first one for $l \in \llbracket 0; t-1 \rrbracket$, and the second one for $l = t$, l being the index of the sum of $p_j(t)$. Therefore, the previous equation can be rewritten as:

$$p_j(t) = p_j(t-1) \oplus \hat{u}_t \times c_{t,j}. \quad (7)$$

Equation (7) is a recurrent series which can be implemented by the register-based structure shown in Fig. 4 for $N = 4$. Since $P_n(t)$ is an N -bit vector, an N -bit register is required to store $p_j(t)$, for $0 \leq t < N$, along with N XORs and N ANDs elements. Every $p_j(t)$, for $0 \leq t < N$, is stored in the j^{th} DFF, R_j . One can notice that the partial sums of the j^{th} row of the graph are computed by $p_j(t)$. Therefore, the partial sums, $S_{m,q}$, located on the m^{th} row of the graph are

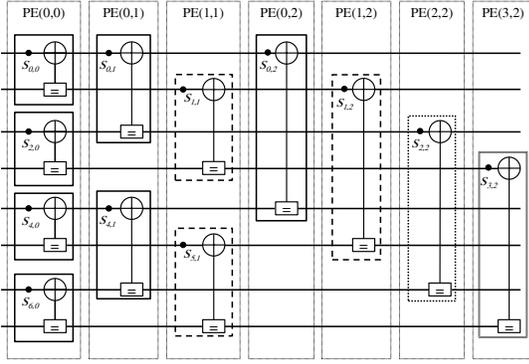


Fig. 5. Factor graph with identification to PE and the required partial sums ($N = 8$).

successively stored in R_m .

IV. SHIFT-REGISTER BASED STRUCTURE

In a tree SC decoder [9], a PE can be assigned to the processing of one or more nodes in the graph. A PE is identified as $PE(x, y)$ such that $0 \leq y \leq n - 1$ and $0 \leq x \leq 2^y - 1$. For instance, in Fig. 5, the partial sums $\{S_{0,0}, S_{2,0}, S_{4,0}, S_{6,0}\}$ are assigned to $PE(0, 0)$. Moreover, in the register-based architecture given in Fig. 4, the partial sum $S_{m,q}$ is stored in the DFF R_m . This means that a PE may be connected to multiple DFFs. Complex multiplexing resources are then necessary to select the partial sums for a given PE. The main purpose of this section is to modify the PSU architecture detailed in Fig. 4 so that all the partial sums required by a given PE are located in the same DFF. Such a structure would avoid any kind of multiplexing between a PE and the DFFs containing the required partial sums.

A. Partial sum location

The proposed structure is derived from the regular architecture depicted in Fig. 4. Instead of updating the current DFF value and store it back in the same DFF, it is possible to update and store this value in the next DFF as shown in Fig. 6 for $N = 4$.

The shift of the $p_m(t)$ values produces the exact same result as long as the coefficient of $\kappa^{\otimes n}$ are shifted accordingly. In this section we consider that the $c_{i,j}$ bits are shifted as well in order to compute the same partial sums and are denoted $c'_{i,j}$. Note that the generation of $\kappa^{\otimes n}$ is further detailed in section V.

As shown in the previous section, without shift, the m^{th} DFF contains the values $p_m(t)$, then the partial sum $S_{m,q}$. In the proposed architecture, due to the shift, $p_m(t)$ is not necessarily located in the m^{th} DFF, thus neither is $S_{m,q}$. For example in Fig. 6, at time $t = 0$, $p_0(0)$ is in R_0 . At time $t = 1$, $p_1(1)$ is in R_0 and $p_0(1)$ is in R_1 . More generally, at time t , $p_m(t)$ is in R_{t-m} . This means that $S_{m,q}$ needs to be located, that is to say, one needs to determine the time of availability, τ , such that $p_m(\tau) = S_{m,q}$. In APPENDIX A it is shown that the partial sum $S_{m,q}$ is generated at time:

$$\tau = (\lfloor \frac{m}{2^q} \rfloor + 1) \cdot 2^q - 1. \quad (8)$$

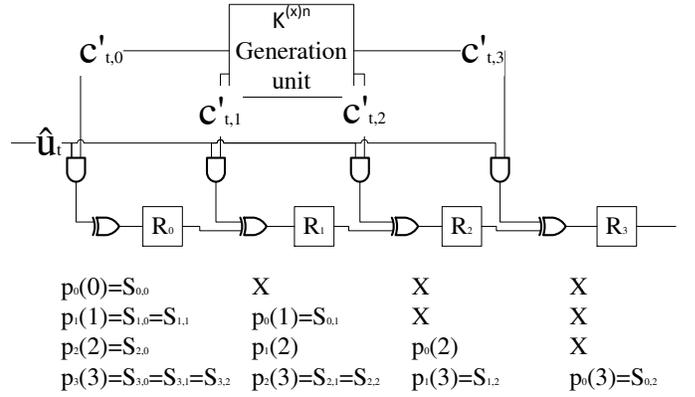


Fig. 6. Shift-register-based architecture for partial sums computation ($N=4$).

In other words, at time τ , the partial sum $S_{m,q}$ is located in the DFF $R_{\tau-m}$.

B. DFF-PE direct connection

It is now possible to know where and when any needed partial sum is located. However, the set of the partial sums that are required by a given PE has to be found in order to show that its elements are generated in the same DFF.

In Fig. 5, a $PE(x, y)$ requires all the partial sums that verify $S_{x+k \cdot 2^{y+1}, y}$ with k chosen such that $0 \leq x + k \cdot 2^{y+1} \leq N - 1$. For instance, $PE(0, 1)$ requires $S_{0,1}$ ($k = 0$) and $S_{4,1}$ ($k = 1$). In the shift-register-based structure, the partial sum $S_{m,q}$ is located in the DFF $R_{\tau-m}$. This means that the set of partial sums required by $PE(x, y)$ are located in $R_{\tau-(x+k \cdot 2^{y+1})}$. By replacing the expression of τ , one can show that the set of DFF required by a $PE(x, y)$ are indexed by the expression $-(x \bmod 2^y) + 2^y - 1$. This index is independent of k . In other words, the partial sums required by $PE(x, y)$ are all located in the same DFF.

Moreover, as $0 \leq y \leq n - 1$, therefore $0 \leq 2^y \leq \frac{N}{2}$. With these considerations, the previous expression of the DFF index ranges from 0 to $\frac{N}{2} - 1$ ($0 \leq -(x \bmod 2^y) + 2^y - 1 \leq \frac{N}{2} - 1$). As a consequence, the $\frac{N}{2}$ first DFFs are sufficient to memorize all the required partial sums during the decoding of code of length N .

The proposed architecture can easily be applied to line SC decoders by grouping the PE which are assigned to the same DFFs ([9]). The shift-register-based architecture may also be employed for a semi-parallel SC decoder architecture by adding multiplexing.

V. $\kappa^{\otimes n}$ MATRIX GENERATION UNIT

The partial sums calculations, for a code of length $N = 2^n$, require the values of $\kappa^{\otimes(n-1)}$ two times as seen in equations (5) and (6), in section III, but for a code size of (2^{n+1}) instead of 2^n . The first time to calculate the partial sums of the first half of the rows in the graph. The last one is for the remaining partial sums. The generation of the bits of the rows of $\kappa^{\otimes n}$ can be seen as a finite state machine with as many state as there are rows to generate. Each state represents a row of the matrix. Every row could be stored in a ROM but

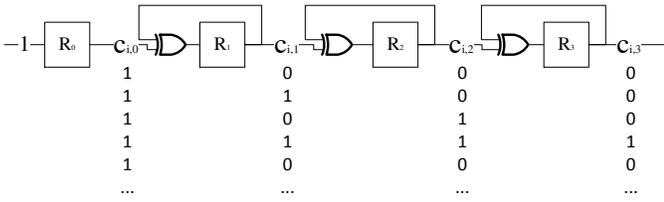


Fig. 7. $\kappa^{\otimes 2}$ matrix generation for a code of size $N = 8$.

this architectural solution would become impractical for code length reaching 2^{20} bits. Another approach is to compute the value of the future state using the current state value. To apply this proposition, a quick observation of the matrix $\kappa^{\otimes(n-1)}$ is necessary. Two main properties can be highlighted:

$$c_{i,0} = 1 \quad \forall i \in \llbracket 0; \frac{N}{2} - 1 \rrbracket$$

$$c_{i,j} = c_{i-1,j-1} \oplus c_{i-1,j} \quad \forall (i,j) \in \llbracket 1; \frac{N}{2} - 1 \rrbracket^2$$

The first property means that the first bit is always one, which is immediate due to the Kronecker power definition. Therefore, this bit does not require recalculations when changing state. The second property is the most important because it is exploited to compute the future state from the current state bit values.

The rows of $\kappa^{\otimes(n-1)}$ are generated one after the other. Therefore, in $c_{i,j}$, the index i represents the time t , while j corresponds to the DFF index, in which the value is stored. The second property is the equation of the construction and can be rewritten as $M_j(t) = M_{j-1}(t-1) \oplus M_j(t-1)$. To implement such an equation, an AND logic gate and a DFF are sufficient. The $\frac{N}{2}$ DFFs are connected one to the other as seen in Fig. 7.

The shift-register based structure, used to compute the partial sums, requires that the bits of $\kappa^{\otimes n}$ are shifted accordingly. One can verify that the diagonals and the columns are equal. Therefore, the proposed structure generates the bits of $\kappa^{\otimes n}$ that can be employed as they are for the shift-register based architecture.

VI. CONCLUSION AND PERSPECTIVES

Designing efficient hardware decoders for polar codes would result in their potential inclusion in future digital telecommunication standards. State of the art works propose efficient successive cancellation decoder hardware designs whose limiting element is the partial sum unit. This paper brings contribution to formalizing the structure proposed in [8], reducing the hardware complexity. The shift-register based architecture can be extended to line SC decoder. It can also be applied to semi-parallel architectures by adding more multiplexing resources.

The proposed computation method opens the way for additional works such as the extension of this architecture to higher kernels or the enhancement of parallelism in this structure.

APPENDIX A

TIME OF AVAILABILITY FOR A PARTIAL SUM

Any partial sum, $S_{m,q}$, can be seen as an element of a sub-codeword $SCW(m, q)$. This sub-codeword is the encoded version of the sub-code $\hat{u}_a^b \in \hat{U}$. All the elements of $SCW(m, q)$ are valid whenever all bits of \hat{u}_a^b are valid. Since the bits are decoded sequentially, a partial sum $S_{m,q}$ is valid when the bit \hat{u}_b is available, that is to say when $\tau = b$. The main purpose is then to find the expression of b . We already know q , thus a is the only remaining variable to find before getting the expression of b . The following equality comes from the length of $SCW(m, q)$, which is the same as the length \hat{u}_a^b .

$$2^q = b - a + 1. \quad (9)$$

Since a is the starting index, it is a multiple of 2^q . The following expression returns the value of a :

$$a = \lfloor \frac{m}{2^q} \rfloor * 2^q. \quad (10)$$

Now the only remaining variable is b . Using equation (9) and (10) it follows:

$$b = 2^q - 1 + \lfloor \frac{m}{2^q} \rfloor * 2^q.$$

Finally, $S_{m,q}$ is only valid when $\tau = b$, that is to say:

$$\tau = b = (\lfloor \frac{m}{2^q} \rfloor + 1) * 2^q - 1.$$

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