On the Calibration of a SPAD-Based 3D Imager with In-Pixel TDC Using a Time-Gated Technique

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***Abstract*—The optical characterization of a CMOS 64×64 single-photon avalanche-diode (SPAD) array with in-pixel 11b time-to-digital converter (TDC) is presented. The overall full-width half-maximum (FWHM) of the detector ensemble SPAD plus TDC is 690ps. The sensor has been fabricated in a 0.18µm standard CMOS technology which features an average dark-count rate (DCR) of 42kHz at 1V excess voltage (V_e) and room temperature. The detector successfully uses its time-gating capability to mitigate this large amount of noise enabling the sensor for accurate time-of-flight (ToF) measurements. The effectiveness of the time-gating technique is experimentally demonstrated. According to measurements, a time window of 400ns is enough to ensure that the TDC is triggered by light rather than by spurious events.**

Keywords*—*time gating; time-of-flight; single-photon avalanche diode; time-to-digital converter; 3D imager

I. Introduction

The integration of **S**ingle-**P**hoton **A**valanche-**D**iodes (SPAD) in standard CMOS technologies has been proved to be feasible [1]. The design of low-noise SPAD is strongly related with the technological process which needs to have extremely low-defect density and low-doped epilayer [2]. This kind of devices is suitable to build 3D imagers capable to estimate the depth of a scene for applications involving low light [3]. With a higher environmental light, additional techniques like spatial correlation will be required to skip events triggered by the background light. Nevertheless one has to take into account that these technologies are very expensive. This is a strong enough reason to explore the possibility to use standard processes. In this case one has to deal with the large amount of noise featured by SPADs built in standard CMOS processes [4].

This paper reports promising experimental results of **T**ime-of-**F**light (ToF) estimation performed by a SPAD-based 3D imager which has been designed and fabricated in a standard 0.18µm CMOS technology [5]. The maximum value of the **P**hoton **D**etection **E**fficiency (PDE) is 2% at 1V excess voltage and room temperature. In the same conditions, an average **D**ark-**C**ount **R**ate (DCR) of 42kHz has been measured. The sensor can be successfully applied for ToF estimation. The overall FWHM jitter of one single pixel detector is 690ps. Although the imager has a relatively high noise, it is still able to acquire depth images with a spatial resolution small enough to retrieve the coarse profile of a scene. This is one of the most important challenges of the design.

The principle of operation of a 3D imager based on SPADs is depicted in Fig. 1. A pulsed laser illuminates the sample through a diffusive material while the synchronicity signal is delivered to the detector. The SPAD array detects the arrival of the pulses form the different points in the object. This detection triggers the in-pixel TDC that will stop with a global synchronization signal. Then 3D shape can be reconstructed, outside of the chip, from the time intervals associated to each point in the focal plane.

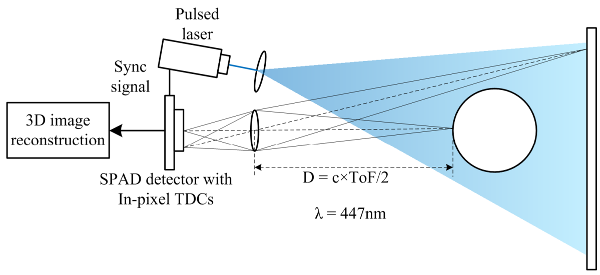

Fig. 1. Time-of-Flight principle of operation

With this setup the operation of the array as a ToF detector has been characterized. It yields a high noise rejection ratio, obtained by applying time-gating to the detector array. Also good uniformity has been observed in the SPAD ensemble, without any calibration at the pixel level.

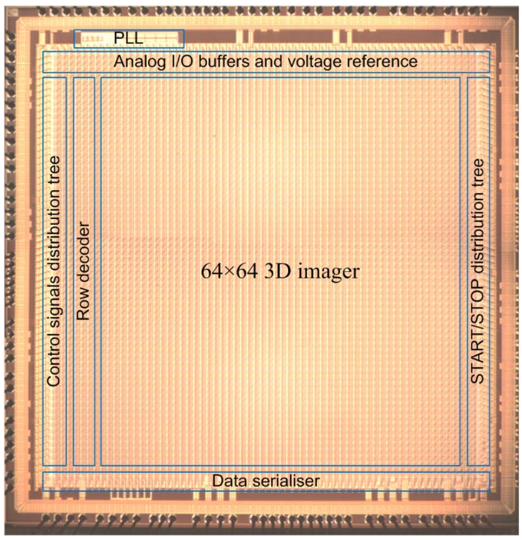

Fig. 2. Chip microphotograph

The organization of the rest of the paper is as follows. Next section briefly describes the architecture of the sensor and the

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experimental setup. The third section is dedicated to the sensor characterization. The forth section is concentrated on the time-gated capabilities of the imager. The efficiency of this technique is experimentally proved as well. The last section is dedicated to conclusions.

II. 3D IMAGER BUILDING BLOCKS

The microphotograph of the chip is presented in Fig. 2. The central component of the chip is the array of 64×64 SPAD cells containing the diode itself, an active quenching/recharge circuit, a TDC, a memory block and the output buffers. Peripheral circuits are needed to supply stable voltage references, provide accurate control and even distribution of time-critical signals, and the data bus for delivering the 11b pixel code representing either the measured ToF or the corresponding photon count.

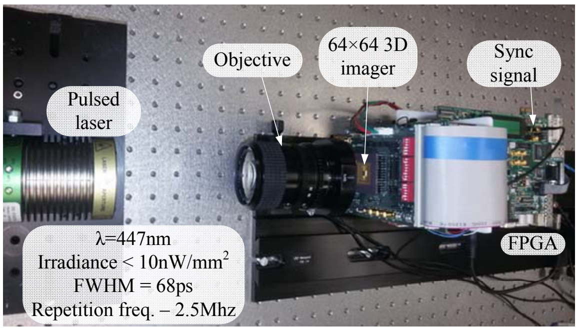

Fig. 3. Topview of the experimental setup

The details of the chip architecture have been already described in [5]. The pixel area is 64×64μm^2. The in-pixel TDC area is about 1740μm^2. The best time resolution measured for the TDCs array is 145ps. The characterization has been made by means of an 8ps incremental resolution **T**ime-**I**nterval-**G**enerator [6]. The average power consumption per TDC is about 9μW. It has been evaluated for 10ns resolved time interval and 500k conversions per second.

This paper is focused on the timing characterization with particular emphasis on the time-gating capability of the sensor. The experimental setup is depicted in Fig. 3. All the experiments are performed in agreement with single photon detection conditions. The synchronization signal of the laser module PDL 800-D is converted to 3.3V CMOS standard. It is used as global STOP signal for the TDCs array. The SPAD detectors are enabled by a time gate of less than 400ns. The first event triggered by light or noise activates the corresponding local TDC which estimates the time interval length (or ToF). The digital code of the time stamps is stored in each in-pixel memory. The frames are readout line by line and stored. The final image containing the actual ToF estimated by each pixel is computed by building time interval histograms over a certain number of frames (see Fig. 8).

III. PERFORMANCE EVALUATION OF THE IMAGER

A. Time resolution

The ToF histogram collected over 50k frames is plotted in Fig. 4. The number of frames is related to the accuracy of the ToF estimation which improves with its square-root. The LSB of the TDC is 160ps. The selected time gate for this experiment is about 50ns. According to Fig. 4 the number of spurious pulses that trigger the in-pixel TDC is negligible.

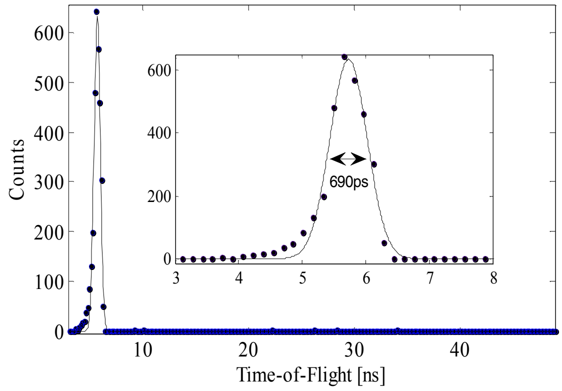

Fig. 4. Time-of-Flight histogram measured by the in-pixel TDC

If the contribution of the noise is assumed to be statistically independent, then the total jitter of the pixel-detector ensemble composed by the SPAD and TDC is:

$$\sigma_{TOT} = \sqrt{\sigma_{TDC}^2 + \sigma_{SPAD}^2 + \sigma_{SYNC}^2}$$

where the σ_{TDC}, σ_{SPAD} and σ_{SYNC} are the jitter of the TDC, SPAD detector and synchronization signal respectively. The jitter of the SPAD has been measured by PICOHARP 300 with 8ps time resolution [7]. The FWHM of the collected histogram is about 200ps. According to Fig. 4, the total FWHM jitter is 690ps. The jitter of the synchronization signal is about 20ps. Therefore the resulting FWHM jitter of the TDC is approximately 660ps, what means ±2.1LSB. The laser repetition period cannot be set less than 327ns which is the maximum time range of the TDC. Therefore the appropriate value that needs to be selected for the laser module is 2.5MHz.

B. Dark count rate

Spurious avalanche currents are caused by phenomena different from impinging photons. There are counts caused by thermal agitation, which adds up to a certain **D**ark **C**ount **R**ate (DCR). Another phenomenon is afterpulsing, in which carriers trapped in the silicon surface imperfections ignite new avalanches [8]. Both of them are considered noise in SPAD detectors. The measurement of the DCR is done by configuring the sensor in the integration mode [5], i. e. when each pixel counts the number of avalanche events during a certain period of time. The only fair evaluation of the DCR has to be done at the same excess voltage required to achieve the best figures of PDE and time resolution.

Fig. 5 shows the DCR distributed across the sensor array at 1V excess voltage (V_e) and room temperature. As it is already known, some pixels in this technology feature an abnormal behavior by showing a much higher DCR than the rest. In our case, these pixels represent more or less 1% of the sensor pixels (see Fig. 6). The number of pixels with a DCR lower than 23kHz covers 70% of the array. In order to successfully resolve the time even in this case, time-gated strategy has been applied. This technique is discussed in the next section.

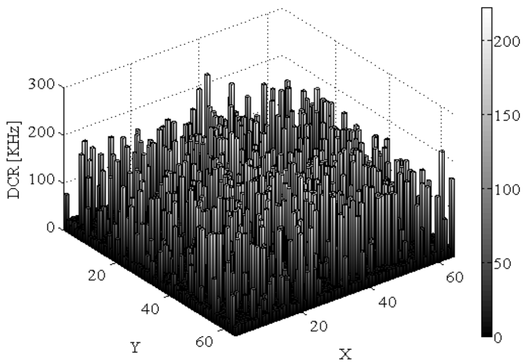

Fig. 5. DCR at 1V excess voltage

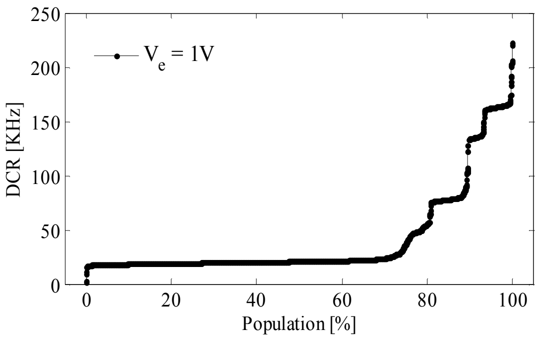

Fig. 6. DCR profile across the sensor

C. *Photon detection efficiency*

The **P**hoton **D**etection **E**fficiency (PDE) can be evaluated from the total count rate subtracting the dark count rate, divided by the expected arrival rate of incoming photons. The PDE of one pixel is shown in Fig. 7.

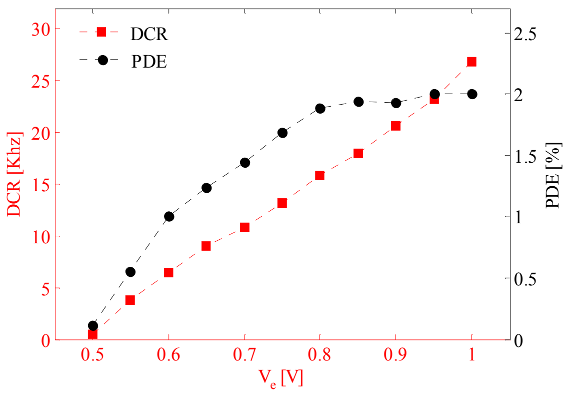

Fig. 7. PDE and DCR vs. V_e

A lower DCR is obtained by decreasing the excess voltage which lowers the PDE and affects the time resolution as well. Therefore a fair comparison requires plotting both DCR and PDE at the same time, bias and temperature conditions. The excess voltage is chosen such that the jitter and the PDE of the SPAD are the best. The value of the DCR corresponding to this V_e needs to be handled during ToF measurements. This evaluation is provided in the next section.

IV. TIME-GATED IMAGING

The only way to handle the large DCR at this point is to time-gate the ToF measurement. Right after a pixel is activated by turning on the SPAD detector, the in-pixel TDC is triggered by the first avalanche pulse which could be spurious or caused by the impinging light. Usually many frames are collected to build an accurate statistic of the light arrival time for each pixel of the array. In our experimental setup, 3D reconstruction works at low video rates, e. g. 1fps, because of the limitations imposed by the instrumentation speed. If synchronous acquisition without additional time out between consecutive frames were possible, e. g. by means of a FPGA, the video rate of the 3D reconstruction can reach 1kfps.

Fig. 8 shows the dependence of the number of pixels activated at least once only by light on the number of frames that have been acquired.

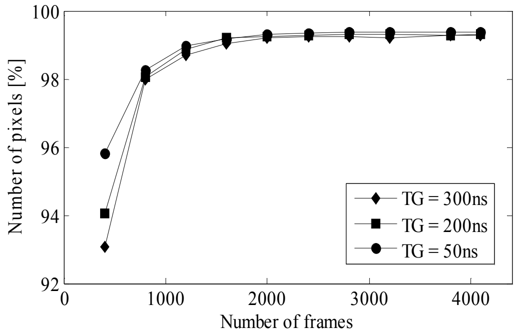

Fig. 8. Dependence of the number of pixels activated by light on the collected number of frames

This means that at least 2k frames are required to activate more than 99% of the sensor. Moreover it can be used at the maximum full dynamic range of 327ns even if 20% of the array has the DCR higher than 80kHz (see Fig. 6). For small number of collected frames, the size of the time gate should be smaller to have more pixels activated by light, and not by thermal agitation or other sources of noise.

Even if the number of frames is considerably high (50k frames) and the time gate is set to 50ns, still there are pixels mostly triggered by noise. Notice that the average value of the histogram still estimates the ToF with an error of 20ps (see Fig. 9). The actual resolved time interval is 5.66ns. It has been measured by PICOHARP 300 with 8ps time resolution [7].

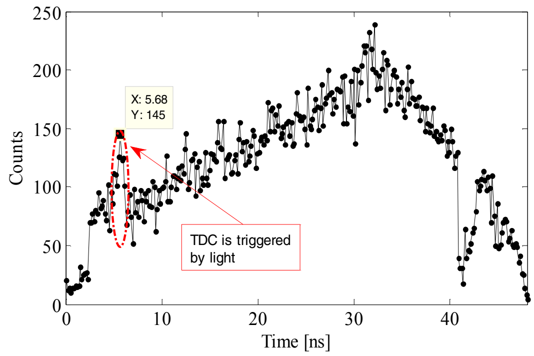

Fig. 9. Time interval histogram of a noisy pixel

When the DCR is high what happens is that the in-pixel TDC is triggered before the light pulse impinges the SPAD. Therefore the detection of the light is masked by the spurious event. This situation is illustrated in Fig. 10. In this case the pixel is not able to evaluate the ToF. One possibility is to reduce the time gate almost at the size of the ToF that needs to be measured. However, this kind of pixels represents less than 1% of the imager.

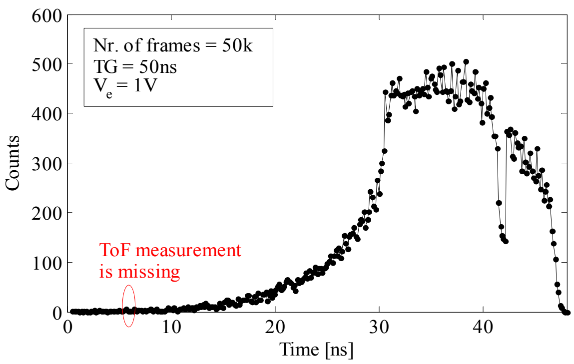

Fig. 10. Time interval histogram of a pixel triggered only by noise

Let us consider that the light is uniformly distributed across the sensor array. The laser is pointing the chip as it is described in Fig. 3. The laser diode has been set to an irradiance of $8nW/mm^2$. The repetition rate is 2.5MHz. In this case all the pixels have to measure the same distance. The emerging ToF surface is shown in Fig. 11. The maximum deviation across the array is ±1LSB (see Fig. 12). These figures are very promising, proving that the sensor can be successfully used for 3D image reconstruction.

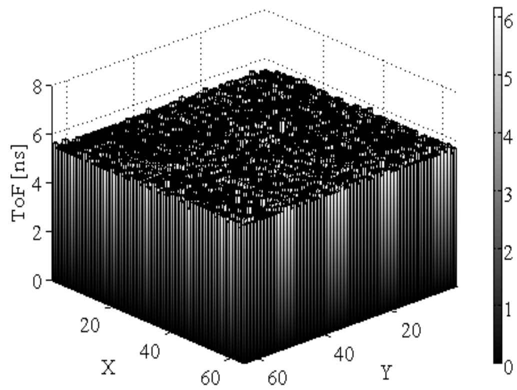

Fig. 11. ToF uniformity

V. Conclusions

A 64×64 SPAD-based 3D imager was fabricated and characterized in 0.18µm UMC standard CMOS technology. The proper functionality of the sensor has been proved by measurements. The key point of the design which makes the ToF estimation possible even with a large amount of noise is the incorporation of time-gated active quenching/ recharge SPAD. This is the first ToF sensor build in a standard process despite the low PDE (2% at 447nm) and large average DCR (42kHz) compared to the state of the art [2].

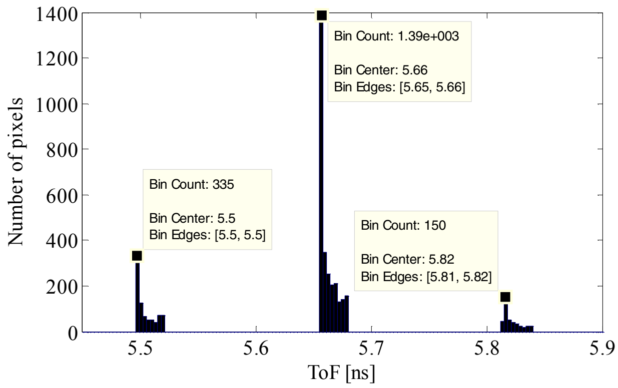

Fig. 12. ToF distribution across the array

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