Towards Probabilistic Analog Behavioral Modeling

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***Abstract*—Analog behavioral models are widely used to reduce the complexity in hierarchical analog circuit design and verification. In the presence of process variations and atomic-level fluctuations, however, these models have to be extended to take variability into account. In this paper, we present a probabilistic solution that treats the behavioral model coefficients as multi-dimensional random variables and supports non-Gaussian as well as correlated parameters. A voltage divider and a bandgap voltage reference demonstrate the capabilities of our modeling approach in terms of accuracy and efficiency.**

I. Introduction

Complexity issues in analog circuit design can be tackled by hierarchical approaches with top-down design and bottom-up verification [1], [2]. However, the simulation-based verification is only efficient when higher-level models replace the circuit-level representations of sub-components. Analog behavioral models are particular approaches for this task [3].

Circuit variability arises from process variations and atomic-level fluctuations [4], [5]. The simulation-based joint analysis of these effects is the subject of the FP7 research project SUPERTHEME. In this paper, we discuss how variability information available in a process design kit (PDK) can be transferred to variation-aware analog behavioral models of analog circuit components to increase the verification efficiency or to create analog intellectual properties (IPs). To our knowledge, variation-aware analog behavioral models have not been widely used yet. Following previous research results [6], [7], we treat the coefficients of a behavioral model as a multi-dimensional random variable (RV). Supporting arbitrary correlations and distribution shapes, in particular non-Gaussian parameters, we describe this RV combining rank correlation coefficients and generalized lambda distributions (GLDs).

In the remainder of this article, Sec. II briefly introduces analog behavioral models and multi-dimensional RVs, and Sec. III presents our modeling approach. In Sec. IV, we demonstrate the accuracy and efficiency of our modeling approach using a voltage divider and a bandgap voltage reference as application scenarios. Including some directions for future research, Sec. V concludes this article.

II. Theoretical Background

A. Analog Behavioral Modeling

A circuit simulator builds a circuit matrix applying Kirchhoff's laws and device model equations. Solving this matrix determines the circuit response to predefined input signals. The potentially large number of active and passive devices in analog circuits can cause a considerable computational effort. Analog behavioral models of circuit sub-components, which are usually written in Verilog-A [8], are an approach to potentially significantly reduce this effort [3]. Instead of matrices from circuit-level representation, they abstract the component behavior by equations that connect pin voltages and currents and can be handled by standard circuit simulators. For example, in Sec. IV-B, (6) and (7) well describe the behavior of the bandgap voltage reference circuit in Fig. 8.

To meet the requirements of recent semiconductor technologies, analog behavioral models have to take variability into account, i.e. they need to capture the variability information available in PDKs. These non-idealities have been considered in variation-aware performance models, such as in [9], or in single-device Verilog-A model considering physical variations [10], but, to our knowledge, not in analog behavioral models.

B. Multi-Dimensional Random Variables

The values of RVs occur according to a probability distribution [11]. A one-dimensional RV A is described by its probability density function (PDF) $\varphi_{\mathrm{A}}(\mathrm{x})$, its cumulative distribution function (CDF) $\phi_{\mathrm{A}}(\mathrm{x}) = \int_{-\infty}^{\mathrm{x}} \varphi_{\mathrm{A}}(\mathrm{x})\,\mathrm{dx}$, or its quantile function $\phi_{\mathrm{A}}^{-1}(.)$. A k-dimensional RV $\mathbf{A}$ consists of random components $\mathrm{A_i}$. It can, for instance, be characterized by [12] (i) its rank correlation matrix $\mathbf{R}$ and (ii) the quantile functions $\phi_{\mathrm{A_i}}^{-1}(.)$ of its random components $\mathrm{A_i}$.

In case of such a description, random samples from the RV $\mathbf{A}$ can be generated with a 4-step approach [12]: (i) element-wise transformation of the matrix $\mathbf{R}$ into a matrix $\mathbf{C}$ with $\mathrm{c_{ij}} = 2 \cdot \sin(\pi/6 \cdot \mathrm{r_{ij}})$; (ii) random sample generation from a Gaussian RV $\mathbf{Z}$ with mean vector $\boldsymbol{\mu} = \mathbf{0}$ and covariance matrix $\mathbf{C}$; (iii) component-wise transformation of Gaussian into uniform components, $\mathrm{u_i} = \Phi(\mathrm{z_i})$ with the standard Gaussian CDF $\Phi(.)$; and (iv) component-wise mapping to the marginal distributions applying their quantile functions, $\mathrm{x_i} = \phi_{\mathrm{Ai}}^{-1}(\mathrm{u_i})$.

In this paper, we apply a probabilistic behavioral modeling approach based on these principles and demonstrate its implementation into a commercial circuit simulator.

III. Probabilistic Behavioral Modeling Approach

We assume to have an analog behavioral model for a particular circuitry with k coefficients $\mathrm{A_i}$. For each sample in a Monte Carlo (MC) study, these coefficients can be determined so that sample data for the model coefficients, i.e. sample data for the RV $\mathbf{A}$, is available. To derive a probabilistic model,

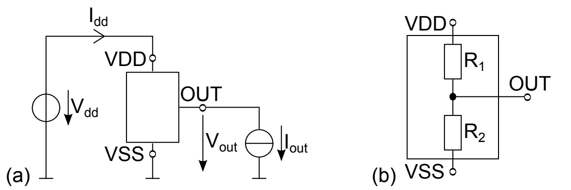

Fig. 1. Voltage divider; (a) test bench; (b) circuit-level schematic

```
`include "constants.vams"
`include "disciplines.vams"
module voltage_divider(VDD,VSS,OUT);
 // pins
 inout VDD, VSS, OUT;
 electrical VDD, VSS, OUT;
 // default model params: R1=1K; R2=2K;
 parameter a1=1.5, a2=1.5m, a3=3.0K;
 // inits
 real v_dd, i_out;
 // model equations
 analog begin
  v_dd=V(VDD,VSS); i_out=I(VSS,OUT);
  V(OUT,VSS) <+ v_dd/a1 - i_out/a2;
  I(VDD,VSS) <+ v_dd/a3 + i_out/a1;
 end
endmodule
```

Fig. 2. Verilog-A analog behavioral voltage divider model

```
Ix (1 2 3) voltage_divider [a1=<val1> a2=<val2> a3=<val3>]
```

Fig. 3. Instantiation of behavioral voltage divider model for simulations

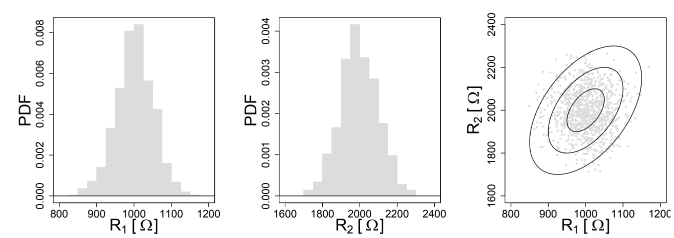

Fig. 4. Joint distribution of resistors R_1 and R_2

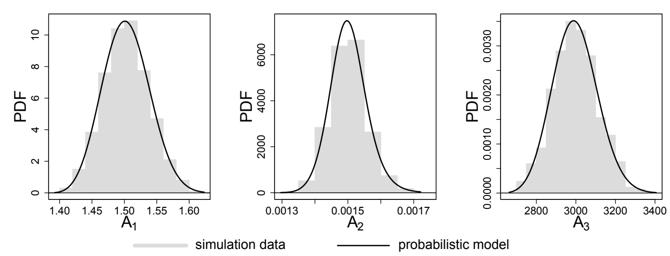

Fig. 5. PDFs of model parameters A_1, A_2, and A_3

we need to determine the rank correlation matrix of this RV and its marginal distributions based on the empirical data.

The $(k \times k)$ rank correlation matrix $\mathbf{R}$ is directly from derived by Spearman's rank correlation coefficients [11]

$$r_{ij} = r_{ji} = 1 - \frac{6 \cdot \sum_{k=1}^{N} d_{ij,k}^2}{N^3 - N} \quad \text{for} \quad i \neq j;\ 1 \leq i,j \leq m. \quad (1)$$

In (1), $d_{ij,k}$ is the rank difference of the k^{th} observations of A_i and A_j, i.e. the difference in their positions in the ordered samples. Note that $r_{ii} = 1$.

Additionally, we approximate the marginal distributions by GLDs defined by the quantile functions [13]

$$A_i = \phi_{A_i}^{-1}(u) = \lambda_{Ai,1} + \frac{\frac{u^{\lambda_{Ai,3}}-1}{\lambda_{Ai,3}} - \frac{(1-u)^{\lambda_{Ai,4}}-1}{\lambda_{Ai,4}}}{\lambda_{Ai,2}} \qquad (2)$$

with $0 \leq u \leq 1$. The four distribution parameters for location ($\lambda_{1,Ai}$), scale ($\lambda_{2,Ai}$), and shape ($\lambda_{3,Ai}$, $\lambda_{4,Ai}$), allow to approximate a variety of distribution shapes, including Gaussian and non-Gaussian distributions.

Applying these basics, we transfer previous research results for transistor compact models and standard cell models [6], [7] to variation-aware analog behavioral models. We perform all calculations in the statistics software *R* [14] and apply a dedicated package for GLD processing [15].

IV. Application Scenarios

We apply the probabilistic analog behavioral modeling approach to two scenarios: a voltage divider and a bandgap voltage reference. While the first scenario is intended to outline the basic procedure, the second scenario demonstrates its capabilities in terms of accuracy and efficiency.

A. Voltage Divider

For a simple voltage divider composed of the resistors R_1 and R_2 with the test bench and circuit-level schematic in Fig. 1, Kirchhoff's laws can be applied to obtain the equations

$$V_{out} = \frac{V_{dd}}{1+\frac{R_1}{R_2}} - \frac{I_{ref}}{\frac{1}{R_1}+\frac{1}{R_2}} = \frac{V_{dd}}{A_1} - \frac{I_{ref}}{A_2} \quad \text{and} \qquad (3)$$

$$I_{dd} = \frac{V_{dd}}{R_1+R_2} + \frac{I_{ref}}{1+\frac{R_1}{R_2}} = \frac{V_{dd}}{A_3} + \frac{I_{ref}}{A_1} \qquad (4)$$

relating the output voltage V_{out} and the current consumption I_{dd} to the supply voltage V_{dd} and the output current I_{ref}. The model coefficients $A_1 = 1 + R_1/R_2$, $A_2 = 1/R_1 + 1/R_2$, and $A_3 = R_1 + R_2$ can be directly calculated in this scenario. Alternatively, they can be determined during characterization from output voltages V_{out} and current consumptions I_{dd} at different supply voltages V_{dd} and output currents I_{ref}. Fig. 2 provides a Verilog-A [8] implementation of (3) and (4); Fig. 3 provides the model instantiation in Spectre [16] syntax.

Due to process variations and atomic-level fluctuations, we assume that the resistors R_1 and R_2 to vary following correlated Gaussian distributions with the mean values $\mu_{R1} = 1\,k\Omega$ and $\mu_{R2} = 2\,k\Omega$, the standard deviations $\sigma_{R1} = 50\,\Omega$ and $\sigma_{R2} = 100\,\Omega$, as well as their product-moment correlation coefficient $\rho_{R1,R2} = 0.5$. Their histograms and scatter plot, the inputs to circuit-level MC simulations, are depicted in Fig. 4. For each MC sample for characterization, the model coefficients A_i can be determined. Their empirical histograms from 1000 samples are illustrated in Fig. 5.

The coefficients A_1, A_2, and A_3 can be modeled as a three-dimensional RV $\mathbf{A}$ applying the approach in Sec. III. From the characterization data, the GLD parameters $\lambda_{A1,1} = 0.67$, $\lambda_{A1,2} = 58$, $\lambda_{A1,3} = 0.076$, $\lambda_{A1,4} = 0.092$;

```
////// user-defined functions
// approximation of standard Gaussian CDF
real pnorm ( real z ) {  // from [15]
 return 0.5 + 0.5*sgn(z)*sqrt(1.0-exp(-0.626657*z*z))
}
// quantile function of GLD
real qgl ( real u, real l1, real l2,
           real l3, real l4 ) {
 return l1 + ( (pow(u,l3)-1)/l3 - (pow(1-u,l4)-1)/l4 ) / l2
}
////// parameter inits
parameters real z1=0 z2=0 z3=0
////// statistics section
statistics {
 process {
  vary z1 dist=gauss std=1 percent=no
  vary z2 dist=gauss std=1 percent=no
  vary z3 dist=gauss std=1 percent=no
 }
 correlate param=[z1 z2] cc=-0.285 // values from conversion
 correlate param=[z1 z3] cc=-0.324 // of R in Eq. (5) as
 correlate param=[z2 z3] cc=-0.803 // in Sec. II.B
}
////// conversion to model params
parameters u1=pnorm(z1)
parameters u2=pnorm(z2)
parameters u3=pnorm(z3)
parameters a1=qgl(u1, 1.5,    38,    0.21, 0.15)
parameters a2=qgl(u2, 1.5e-3, 2.8e4, 0.13, 0.026)
parameters a3=qgl(u3, 3e3,    0.013, 0.19, 0.12)
```

Fig. 6. Statistics section for voltage divider behavioral model; approximation of standard Gaussian CDF (function *pnorm*) from [17]

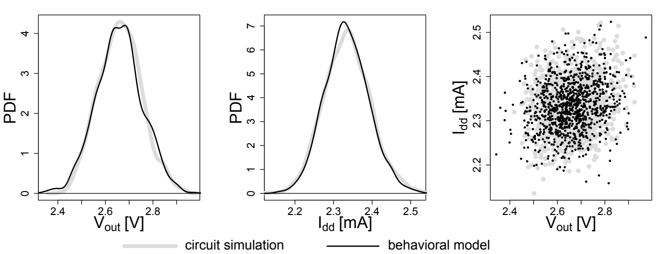

Fig. 7. Joint voltage divider performance parameter distributions (V_{out} and I_{dd}) from circuit-level simulations and behavioral model evaluations

$\lambda_{A2,1} = 670$, $\lambda_{A2,2} = 0.027$, $\lambda_{A2,3} = 0.083$, $\lambda_{A2,4} = 0.12$; and $\lambda_{A3,1} = 3.3\mathrm{E}{-4}$, $\lambda_{A3,2} = 5.1\mathrm{E}4$, $\lambda_{A3,3} = 0.31$, $\lambda_{A3,4} = 0.028$ as well as the rank correlation matrix

$$\mathbf{R} = \begin{pmatrix} 1 & -0.27 & -0.32 \\ -0.27 & 1 & -0.79 \\ -0.32 & -0.79 & 1 \end{pmatrix} \quad (5)$$

can be derived. In Fig. 5, the GLD approximations well represent the sample data. For example in a statistics section in Spectre syntax as in Fig. 6, the model statistics can be implemented to obtain a variation-aware analog behavioral voltage divider model. This model can be instantiated in a netlist according to Fig. 3 replacing <vali> with a_i.

For model validation, we compare MC evaluations of the behavioral model and circuit-level MC simulations at $V_{dd} = 5\,\mathrm{V}$ and $V_{out} = 1\,\mathrm{mA}$ with 500 samples each. As illustrated in Fig. 7, the PDFs and the scatter plots of the voltage divider output voltage V_{out} and current consumption I_{dd} do not differ. Hence, the variation-aware behavioral model is electrically equal to the circuit-level representation, which verifies our modeling approach. Since the circuit consists of two linear elements only and the behavioral model consists of two equations, behavioral modeling cannot be expected to improve the computational efficiency in this scenario.

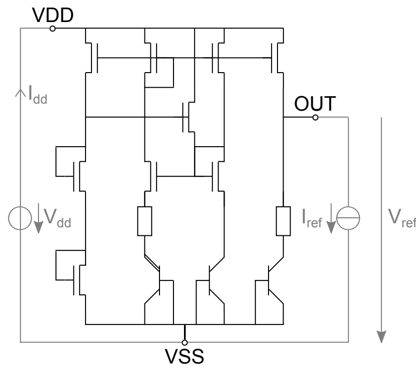

Fig. 8. Circuit-level schematic of the bandgap voltage reference

B. Bandgap Voltage Reference

Fig. 8 depicts a possible circuit implementation of a bandgap voltage reference circuit. Due to its moderate complexity, an appropriate behavioral model may indeed speed up the circuit verification.

In a $0.35\,\mu\mathrm{m}$ industrial technology, the equations

$$V^*_{ref} = A_1 + A_2 V^*_{dd} + A_3 T^* + A_4 \left(T^*\right)^2 + A_5 I^*_{ref} + A_6 V^*_{dd} T^* \quad (6)$$

$$I^*_{dd} \;= A_7 + A_8 V^*_{dd} + A_9 T^* + A_{10} \left(T^*\right)^2 \quad (7)$$

relate the reference voltage V_{ref} and the current consumption I_{dd} to the supply voltage V_{dd}, the temperature T and the output current I_{ref}. Using relative parameters $x^* = (x - x_0)/x_0$ and ten coefficients A_i, (6) and (7) well trade off accuracy and complexity at supply voltages $V_{dd} \in [3.0, 3.6]\,\mathrm{V}$, temperatures $T \in [-40, 160]\,^\circ\mathrm{C}$, and output currents $I_{ref} \in [1\,\mathrm{nA}, 1\,\mu\mathrm{A}]$. The reference values V_{ref0} and I_{dd0} are obtained at $V_{dd0} = 3.3\,\mathrm{V}$, $T_0 = 27\,^\circ\mathrm{C}$, and $I_{ref0} = 100\,\mathrm{nA}$. The coefficients A_i in (6) and (7) are extracted from circuit-level simulations that observe reference voltage V_{ref} and current consumption I_{dd} while sweeping supply voltage V_{dd}, temperature T, and output current I_{ref}. Implemented in Verilog-A, (6) and (7) realize an analog behavioral bandgap model.

With variability information from a PDK, the model extraction can be repeated for each sample of a circuit-level MC simulation. We evaluate 1000 samples to determine sample data of the coefficients A_i. Shapiro-Wilk tests [11], [14] with $5\,\%$ confidence levels figure out that only the coefficients A_1, A_3, and A_4 are Gaussian while the others are not, justifying the support of non-Gaussian distributions in our approach. To model the coefficients A_i as a ten-dimensional RV $\mathbf{A}$, we compute the (10×10) rank correlation matrix $\mathbf{R}$ and map the marginal distributions to GLDs. The PDFs and scatter plots of selected coefficients in Fig. 9 demonstrate that the model well captures the characterization data. It can be implemented following the principles for the voltage divider in Fig. 6 to yield a variation-aware analog behavioral bandgap model.

To validate our model, we run 1000-sample MC evaluations of the circuit in Fig. 8 and the variation-aware analog

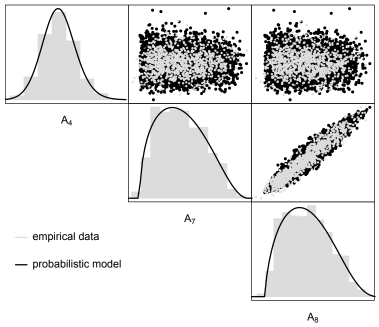

Fig. 9. Selected parameters of probabilistic behavioral bandgap model

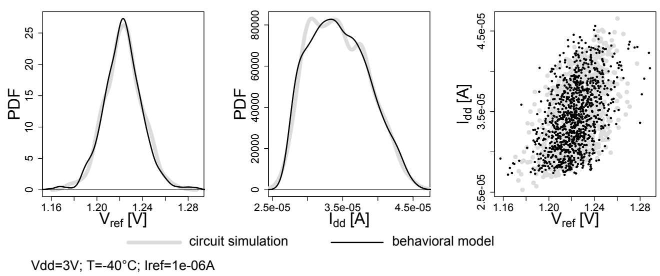

Fig. 10. Example results of behavioral model evaluation for the bandgap

behavioral bandgap model. At various combinations of supply voltages $\mathrm{V_{dd}}$, temperatures T, and output currents $\mathrm{I_{ref}}$, we observe the distributions of the reference voltage $\mathrm{V_{ref}}$ and the supply current $\mathrm{I_{dd}}$ for both representations, see Fig. 10 for an example. We compare these distributions with Kolmogorov-Smirnov tests [11], [14] with $5\,\%$ confidence levels and cannot observe significant differences. Hence, both circuit representations are electrically equal. The major benefit of the behavioral bandgap model, however, is its efficiency. While the 1000-sample circuit simulation for model validation takes $374\,\mathrm{s}$, the behavioral model evaluation finishes in $94\,\mathrm{s}$, corresponding to a $4\mathrm{X}$ speed up without loss of accuracy.

It has to be noted that the model extraction based on circuit-level simulations sweeping supply voltage $\mathrm{V_{dd}}$, temperature T, and output current $\mathrm{I_{ref}}$ takes about $15\,\mathrm{s}$ per sample point, creating a significant characterization effort for the 1000-sample characterization used in this paper.

V. Summary

Analog behavioral models allow handling the complexity in analog circuit design and verification. However, to meet the requirements of deeply scaled technologies, they need to be enhanced to capture variability.

For this purpose, we propose and demonstrate a variation-aware approach. The coefficients of an analog behavioral model are treated as a multi-dimensional random variable (RV), which is described combining rank correlation coefficients and generalized lambda distributions (GLDs) to capture arbitrary correlations and various distribution shapes. We further present how to implemented and access such a model using Verilog-A and the Spectre circuit simulator. We confirm the model accuracy in application scenarios and achieve a $4\,\mathrm{X}$ gain in efficiency evaluating a variation-aware behavioral bandgap model compared with circuit-level simulations.

However, extracting the coefficients based on MC simulations and subsequent modeling may require an immense computational effort. Fine-tuned behavioral models with fewer coefficients and smaller sample sizes may lead to short-term improvements. Further research may include advanced model extraction methods, correlation handling across multiple levels of hierarchy and between different behavioral model instances, or the integration of variation-aware behavioral models into analog IP design flows, such as [2]. Nevertheless, we believe that the proposed approach provides a step towards variability-aware behavioral models of analog circuits.

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