Device Modelling of Bendable MOS Transistors

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***Abstract*—This paper presents the directions for computer aided design, modelling and simulation of bendable MOSFET transistors towards futuristic bendable ICs. In order to compensate the bending stress a generalised geometry variation is discussed. Based on drain-current and threshold-voltage parameters varying under the bending stress, a Verilog-A compact model is proposed and describes I-V characteristics of a MOSFET in a standard 0.18-μm CMOS technology. This model has been compiled into Cadence environment to predict value and orientation of the bending stress. The proposed model validates against macro-model simulation results, and agrees for both the electron and hole conduction. It has been found that there is significant performance advantage in process-induced uniaxial stressed n-MOSFET, exhibiting a smaller drain-current variation and threshold voltage shift by monitoring the bending stress and changing the supply voltage.**

***Index Terms*—Bendable Electronics, MOS Transistor, Compact Device Modelling.**

I. Introduction

During the last decades the microelectronics industry have witnessed aggressive scaling of CMOS transistors from micrometer to the nanometer ranges, in order to improve performance, power consumption and cost [1], [2]. Scaling has been accompanied by various techniques to boost the device's performance [3]–[5]. Among them, strain engineering [6], [7] stands significant from other techniques, by providing a large enhancement of the carriers mobility [8]. If the nanoscale integrated circuits (ICs) are additionally intended to be manufactured on ultra-thin Si-chips for bendable electronics [9], then external global stress get introduced during or due to bending and twisting of the chip. Stress applied to Si crystal changes its resistivity [10], the electronic transport properties, thus changing the MOSFETs drain current. Stress affects the transistor's performance and consequently varies the output signals of the analog and digital circuit building blocks. Moreover, in CMOS-compatible sensors such as Hall, pressure, temperature, chemical/biological, or other sensors, stress introduces offsets that affect the sensitivity and detection ability of static and low frequency environment signals [11].

In order to fabricate ICs that function within specifications, both planar as well as during mechanical deformation, the effects of stress must be considered in the design process. Modelling of bendable devices will play a critical role in design of bendable ICs and help produce cost-effective and reliable flexible electronics, which have different simulation scenarios in both SPICE (Simulation Program with Integrated Circuit Emphasis) and FEM (Finite Element Method), as shown in Fig. 1. The conventional complementary-metal-oxide-semiconductor (CMOS) transistor compact models for

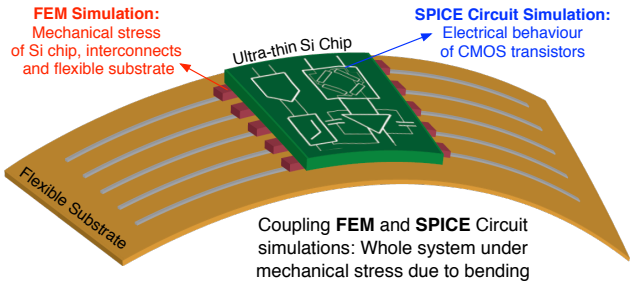

Fig. 1: Simulation scenarios of bendable ultra-thin Silicon chips.

SPICE simulations can predict the response of devices produced via various standard technologies. The local-induced stress-effects [6], [12] have been intensively studied and included in device compact models [13], [14]. On the other hand, the effects of external-induced stress are an ongoing investigation and the exist compact models are inadequate for electronics over flexible and bendable substrates [15]. This paper addresses this limitation of conventional circuits simulation tools by providing a new compact model that include the bending (both static and dynamic) related effects on device behaviour. Effects of deformation such as static and dynamic bending of the bendable substrates with electronics over them will be accounted for. The new model will allow early prediction (i.e. during the design phase itself) of the bending related effects in the electrical behaviour of devices and empower us to design circuits capable of operating reliably during arbitrary deformations. By using such models, any change of the electrical parameters of transistors induced by deformation can be predicted in the early phase of the schematic design in SPICE simulators such as Cadence environment.

The paper is organized as follows: Section II contains theoretical aspects of bending effects on transistor parameters and variation-compensation techniques. Compact device modelling of MOS transistors by using a stress-dependent MOSFET macro-model and Verilog-A are presented in Section III. The simulation results using compact models are discussed in Section IV. Finally, the conclusions are given in Section V.

II. Bendable Device Modelling

This section discusses the modelling and simulation scenarios for bendable CMOS devices and circuits. The flow involves different abstract levels, as shown in Fig. 2. The labels A, B, C etc. identify blocks in various levels of simulation.

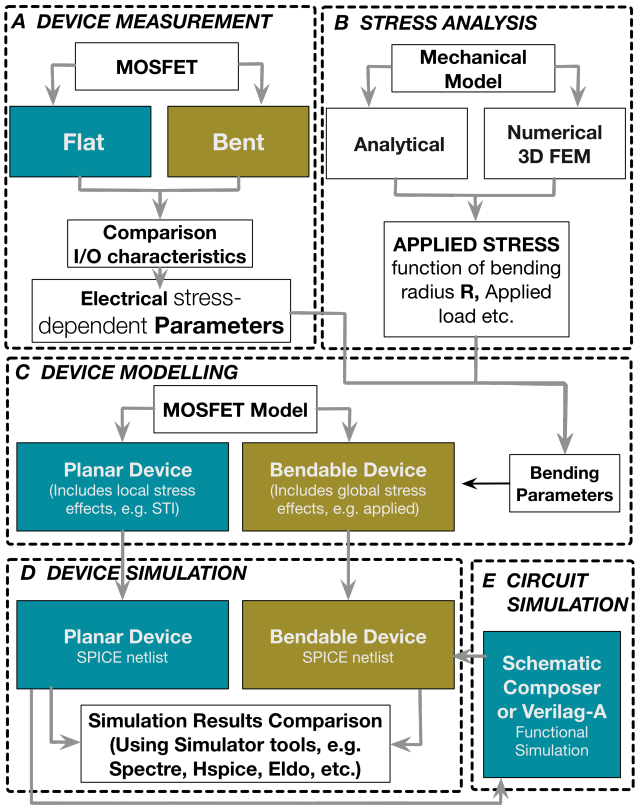

Fig. 2: A CAD-based simulation flow to study electrical device characteristics of bendable CMOS integrated circuit.

Prior to the SPICE model, device measurement and comparison I/O characteristics of both flat and bend devices (A) will be needed. In order to identify the MOSFET parameters that are sensitive to the applied stress such as carriers mobility and threshold voltage parameters. The model includes the short channel effects such as well proximity, impact ionisation, STI stress effects, etc. The mechanical stress analysis is performed in parallel (B), in order to determine the applied stress magnitude and distribution as a function of the applied load, bending radius R. Analytical and numerical FEM models are used for this purpose. FEM simulation are used to find the strain on interconnects and their relative movement with each other to find the change in parasitic resistances and capacitance with various standard bending/flexing or movements there by affecting the interconnect delay. Their variation with stress is expressed as a function of their sensitivities to stress. These are called as stress aware device SPICE models. The stress-induced changes in MOSFET parameters are computed at the transistor level, and then propagated to the gate and circuit level in order to predict circuit-level delay, leakage current and active power consumption for strained inverters, current mirror circuits and ADCs.

Once the planar devices are measured (A) those mechanical models (B) could be used in the next abstract model of functional modelling/simulation (C). In the level of functional simulation (C) will use the original model and SPICE models to simulate the planar devices and circuits. This simulation uses SPICE netlists (D) such as planar BSIM standard and/or locally stress aware device models such as models considering effects of strained silicon in a local scale affecting the mobility. The SPICE netlists of the planar and bendable MOSFET are provided to the simulator tool as input together with the voltage conditions. The devices are simulated in both linear and saturation regimes in order to compare their electrical parameters in each case. These models are well established and already available and used in commercial/non-commercial EDA tools such as Virtuoso Spectre, Edlo, PSpice, HSPICE, ADS etc. This will depend on the technology corresponding to the SPICE file.

From planar functional simulation, physical stress effect modelling (D) followed by physical simulation are done. In this simulation, effect of bending of interconnects could be brought in with 3D FEM of interconnect simulation (B). In this level, the output from the planar or local stress aware model of individual devices or components will be used just to model the overall parasitic effect due to bendable interconnects. The bending will cause additional strain in the wires which will affect the conductivity of the wires and the respective parasitic resistances. This level (D) covers the aspect of contacts and the lumped devices (considering planar or local stress aware model). Here a Verilog-A/system-C code could be used to synthesise the circuit; then a layout planning or optimisation stage followed by interconnects/block-power-handling optimisation stage. This level will help to come up with proper compensation circuits for different devices/blocks for optimal operation with global bending.

The final level (E) involves behavioural composer tools such as schematic capture or Verilog-A or system-C could be used to realise the schematics/desired functionality followed by planar functional simulation. The Verilog-A describes compact models to find a stress-aware schematic with electronic compensation capabilities and layout design optimisation. This block cover analogue circuits, digital or mixed signal circuits.

III. Bendable MOS Compact Model

Several modelling teams deal with the compact modelling of bulk MOSFET and advanced technologies such as double-gate (DG) MOSFET [16], graphene FET transistors [17], MoS_2 FET [18], and CNTFET (Carbon NanoTube FET) [19], for use in design of analog and mixed circuits. Its major goal is to bring simple solutions, numerically efficient and close to the physics of the device. These compact modelling extensively studied the capabilities of Verilog-A and VHDL-AMS for developing compact models. However, few models work on the effect of stress in MOSFETs such as [20] and [21].

First a Verilog-A compact model is derived and describes I-V characterisations of a MOSFET in a standard 0.18-μm CMOS technology. This model has been compiled into Cadence. The proposed model is validated against macro-model simulation results, and an agreement has been achieved for both the electron and hole conduction simultaneously.

An overview of the simulation flow that is used to link stress effects to circuit performance has been presented in Fig. 2. These step sequences enable design and fabrication of the ultra-thin Si chips to achieve the target performance objectives under mechanical stress.

A. Generalised Geometry Variation Under Bending Stress

Several parameters are affected under bending stress and varying the transistor behaviour and performances. Therefore, it is important to properly understand bending effects on channel mobility, threshold voltage, and other electrical parameters such as saturation velocity, parasitic resistance, gate leakage, gate stack, and reliability of MOS devices.

Understanding the magnitude of the mobility variation and threshold-voltage shifting under uniaxial stress is important when determining the performance gain of bended-Si. Since performance benchmarking needs to be done to obtain highest efficiency at worst case, an adjustment to compensate for the stress-induced mobility variation and threshold-voltage shift is required. This adjustment can be accomplished by determining the difference of the stress versus crystal orientations. On the other hand, since the supply voltage of transistors are constant, therefore still the effects of geometry variation under bending stress is main challenging issues since the threshold voltage is changing proportional with stress. As it can be shown as in saturation region:

$$I_{Dstress} \propto \mu C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2$$
$$\cong (\Delta G \ .\mu_0 C_{ox0}) \left(\frac{W_0/\Delta G}{L_0/\Delta G}\right) \left[\frac{V_{GS} - V_{th}}{\Delta G}\right]^2 \propto \frac{I_{D_0}}{\Delta G} \quad (1)$$

where ΔG is geometry variation factor of the transistor and I_D is drain-current under bending stress. Furthermore, the MOSFET geometry factor variation under bending stress directly affect the substrate doping, and reversely change oxide thickness (t_{ox}) and consequently gate capacitance (C_{gate}). This can cause variance the power consumption as a factor of $\pm\Delta G^{-2}$:

$$P_{peak}{=}I_{Dstress}.V_{DDstress}{=}\left(\frac{I_{D0}}{\Delta G}\right)\left(\frac{V_{DD0}}{\Delta G}\right){=}\frac{P_{peak0}}{\Delta G^2} \quad (2)$$

In order to adjust above mentioned issues a generalised geometry variation under bending stress approach is presented, which can control the voltage supply (V_{DD}) in compare to dimension changing under stress. This can help to compensate the current drain and threshold voltage as:

$$I_{Dstress}{\propto}(\Delta G \ .\mu_0 C_{ox0})\left(\frac{W_0/\Delta G}{L_0/\Delta G}\right)\left[\frac{V_{GS}{-}V_{th}}{\Delta U}\right]^2{\propto}\frac{\Delta G \ .I_{D_0}}{\Delta U^2} \quad (3)$$

where ΔU is voltage supply coefficient. If it provided by $\Delta U^2 = \Delta G$ by monitoring the amount change of dimension change, this turns out to $I_D = I_{D_0}$.

B. Verilog-A Model

A compact model precisely predicts the performance of the simulated circuits under stress and eases the bendable large-scale integrated circuit. With the parameters extracted from a standard 0.18-μm CMOS technology, the compact model is implemented in Verilog-A language to enable circuit simulation as in standard silicon ASIC design process [20].

Based on the state-of-the-art theoretical concepts and experimental results in literatures of the piezoresistive effect and the observed behaviour of the tested transistors, the drain-current duo to mobility variation and threshold-voltage parameters in the BSIM4 model are modified:

$$I_{D_{stress}} = I_{D_0} \times (1 - \Pi_{I_D} \cdot \sigma_{I_D}) \quad (4)$$

$$V_{th_{stress}} = V_{th_0} \times (1 - \Pi_{V_{th}} \cdot \sigma_{V_{th}}) \quad (5)$$

where $I_{D_{stress}}$ and $V_{th_{stress}}$ are new effective drain-current and threshold-voltage parameters including bending stress. I_{D_0} and V_{th_0} are original drain-current and threshold-voltage of the transistor without stress, respectively. Piezoresistive coefficients proportional to the drain-current and threshold-voltage are shown in Π_{I_D} and $\Pi_{V_{th}}$. The σ_{I_D} and $\sigma_{V_{th}}$ are known as proportional bending stress to drain-current and threshold-voltage, respectively.

Two instance parameters are defined in the compact model in order to perform simulations: bending radius (R) and stress orientation (Θ). The σ_{I_D} and $\sigma_{V_{th}}$ are contributions of R define as:

$$\sigma_{I_D} = E \cdot \frac{h}{2R} \cdot \Delta G_{I_{D0}}(1 + \frac{\Delta G_{I_D}}{G_{I_D}}) \quad (6)$$

$$\sigma_{V_{th}} = E \cdot \frac{h}{2R} \cdot (\Delta G_{V_{th0}} + \frac{\Delta G_{V_{th}}}{G_{V_{th}}}) \quad (7)$$

where h is the thickness of wafer and equals to 625 μm, and the Young's modulus for silicon has been considered as $E \cong 169$ GPa. The geometry variation factor of drain-current and threshold-voltage are shown as $\Delta G_{I_{D0}}$ and $\Delta G_{V_{th0}}$, which with $\frac{\Delta G_{I_D}}{G_{I_D}}$ and $\frac{\Delta G_{V_{th}}}{G_{V_{th}}}$ have been considered as the geometry dependency of transistors under stress.

The Π_{I_D} and $\Pi_{V_{th}}$ are contributions of the stress orientation versus the wafer crystal orientation given as:

$$\Pi_{I_D} = 1 - 2 \times \pi_{I_D} \cdot \sin(\Theta) \quad (8)$$

$$\Pi_{V_{th}} = 1 - 2 \times \pi_{V_{th}} \cdot \sin(\Theta) \quad (9)$$

where Θ is stress orientation in 0° and 90° versus wafer crystal direction. The π_{I_D} and $\pi_{V_{th}}$ are proportional coefficients of piezoresistivity which varying by drain-current and threshold-voltage, respectively.

IV. Simulation Results

As part of the compact model validation, a behaviour of the n-MOSFET under different bending stress are simulated. The schematic in Fig. 3 shows the simulation results. Fig. 3(a) and (b) depicts the modelled I-V characteristics. With parameters extracted from FETs, the Verilog-A model enables circuit simulation as in standard silicon ASIC design process an a negligible variation observed in the simulated threshold voltage (V_{th}), as shown in Fig. 3(c). Fig. 3(d) depicts the drain-current (I_D) variation which it increased by 5.2% under

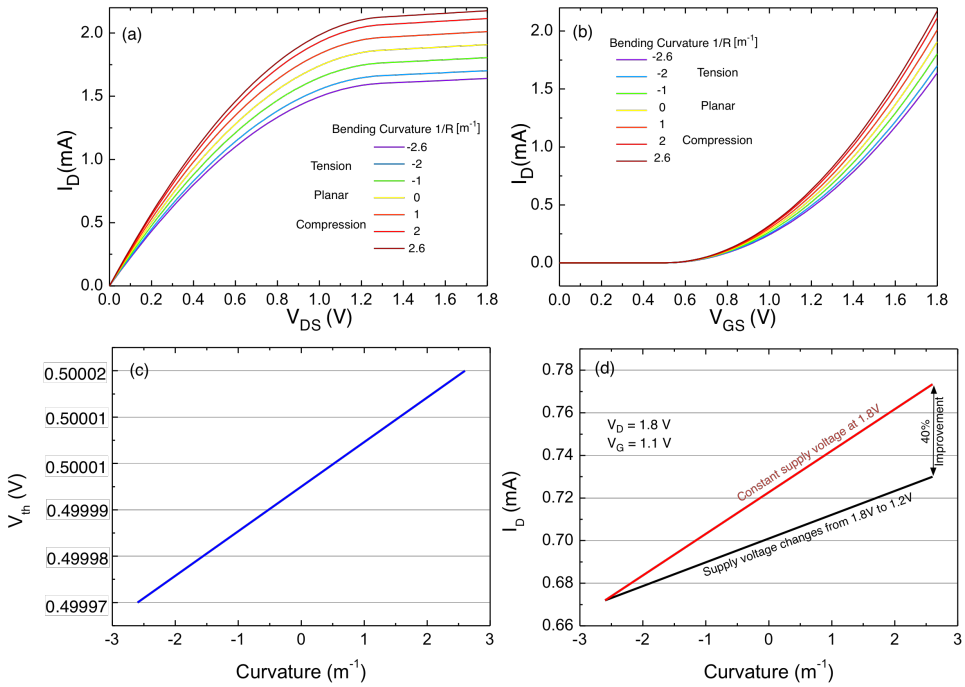

Fig. 3: I-V curves of a bendable n-MOSFET from Verilog-A model.

bending curvature of -2.6 to 2.6 m^{-1}. However, it can be noted that if the supply voltage reduces when the bending increases, the drain-current variation can be improved by 40%.

V. Conclusion

Compact modelling is the best solution to leverage between the accuracy and design complexity. This paper described a platform to estimate the performance of conventional CMOS circuits under bending stress. It will serve to guide future experimental work by identifying which device features must be optimised as technology progresses. The simulation results show that compensation of drain-current and threshold-voltage bending stress effects is a viable approach of the design bendable circuits by using such compact models.

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