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Crosstalk Noise Effects of On-Chip Inductive Links on Power Delivery Networks

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Abstract—Inductive links have been proposed as an inter-tier interconnect solution for three-dimensional (3-D) integrated systems. Combined with signal multiplexing, inductive links achieve high communication bandwidth comparable to that of through silicon vias. However, being a wireless medium, electromagnetic coupling between the inductive link and nearby on-chip interconnects can cause voltage fluctuations affecting interconnect performance. The interference of interconnects on the operation of inductive links has been empirically investigated. Nevertheless, the reverse problem has yet to be explored. Consequently, this paper investigates the effect of electromagnetic coupling on global interconnects of the power delivery network in the vicinity of on-chip inductors. Analysis shows that operation at 6 GHz leads to an induced noise of 39.5 mV per link, which increases further if the interconnect length spans several inductors. As this noise adds to the existing power supply noise, this paper proposes amendments to the placement of the power/ground lines to maintain the power supply noise below a specified limit.

I. INTRODUCTION

Heterogeneous three dimensional integration is an emerging technology that provides a platform for multifunctional, high performance, and low power electronics [1], by vertically stacking ICs of disparate technologies. Through silicon vias (TSVs) and inductive links provide low latency and low power interconnections [2] for inter-tier communication, exhibiting comparable performance, when signal multiplexing is employed for inductive links [3].

TSVs, however, can be an expensive means due to manufacturing complexity and possibly low yield [4]. Alternatively, inductive links comply with standard (2-D) CMOS processes. Furthermore, inductive links provide unique advantages to heterogeneous integration, such as die detachability [5], and although the transceiver is designed in different nominal voltage supplies there is no need to add level shifters [6].

High performance inductive links have been developed recently [7], [8]. In addition to design methods, crosstalk between inductive links has been experimentally investigated [5], [9], while more recently the interference of interconnects on inductive links has been explored [10]. Nevertheless, the effect of inductive links on global interconnects has yet to be investigated.

This work focuses on the noise caused by electromagnetic coupling between the inductive link interface and the power

delivery network (PDN). This crosstalk noise is added to the other components of noise experienced by the power delivery network. Power/ground (P/G) wires suffer from static IR -drop noise due to the wire resistance and transient, high frequency voltage drops, $L \frac{di}{dt}$ due to device switching [11]. In 3-D systems with inductive links, voltage fluctuations are induced on the P/G wires adjacent to the inductive link array, deteriorating system robustness.

Standard design methods and CAD tools for PDN provision for the static and dynamic noise sources. However, traditional PDN design does not cope with the additional noise, originating from the inter-chip inductors in contactless 3-D systems. Consequently, the combined effect of noise from PDNs is addressed in this paper, including the induced noise by multiple inductors and the resistive IR -drop noise. Interconnect structures are simulated, considering the spatial alignment of power and ground loops to the inductive link. An expression that determines the impact of an inductive link array onto a power/ground grid is also provided. Analysis indicates that crosstalk coupling between inductors and P/G wires can lead to harmful levels of power supply noise. Measures to avoid this situation are proposed.

The remainder of this paper is organised as follows. In Section II, a structure consisting of an inductive link and a loop of either a power or ground wire is analysed. Moreover, the behaviour of the induced noise is presented. A practical scenario where an array of inductive links couples to a portion of the power network is investigated in Section III, where the location of P/G lines is adapted to satisfy noise constraints. Some conclusions are drawn in the final section.

II. INDUCTIVE LINK - PDN CROSSTALK ANALYSIS

The coupling between inductive links and a global P/G wire is presented in this section. The noise behaviour over the spectrum of operating frequencies for an inductive link is described. Moreover, the variation of the induced noise with the spatial position of the P/G loop is investigated.

The simulated structure based on a flip-chip and face-to-back 3-D integration approach comprising an inductive link and an interconnection loop is illustrated in Fig. 1. The cross-section of the structure is depicted in Fig. 1(a), showing the distance X between the inductors of the link and the pitch of the power lines s_{PDN} . The top view of this structure is seen in Fig. 1(b). The length of the interconnect is denoted as

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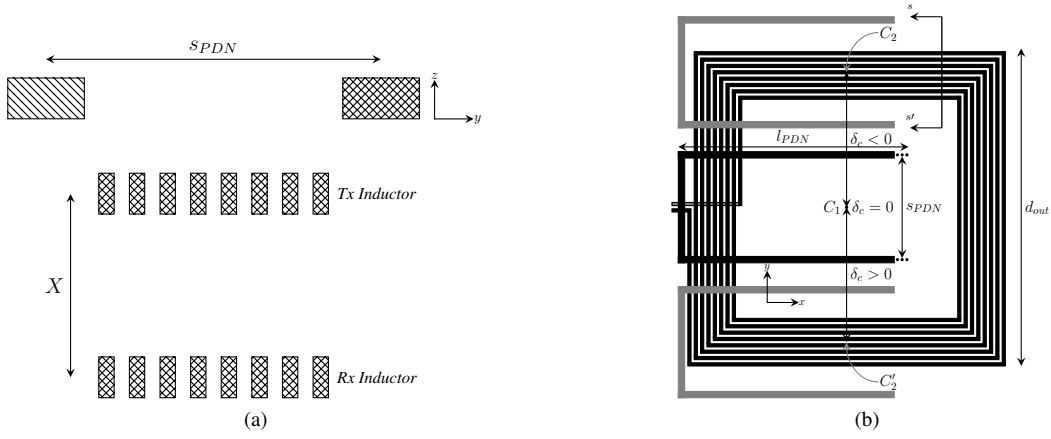


Fig. 1: Inductive link with adjacent P/G loop, (a) cross-section of the structure along $s - s'$ in Fig 1(b) and (b) top view of the structure with the loop placed in different locations.

l_{PDN} . Distance δ_c denotes the spatial separation between the geometric centre of the inductor, C_1 and the geometric centre of the interconnect loop.

The loop in Fig. 1(b) is assumed to be a pair of power lines within a pseudo-pair grid with Double Signal Double Ground (DSDG) [11]. Although a power loop is investigated in this paper the same analysis is also applicable to a ground loop. To assess the impact of the electromagnetic coupling between the inductive link and the power loop, a set of simulations is performed, considering both the frequency dependence and the spatial alignment of the loop with respect to the centre of the inductive link. Simulations are performed with Ansys Electronics Desktop (HFSS) [12].

Voltage fluctuation V_{noise} induced by the inductor to the power loop is extracted by the S-parameters of the simulated structure. As the transmission coefficient S_{ij} describes the transmitted voltage ratio between the respective structures [13], V_{noise} is given by

$$V_{noise} = (S_{31} + S_{21}S_{32})V_{dd}, \quad (1)$$

where S_{31} is the transmission coefficient from the transmitter inductor to the PDN wire. S_{21} describes the transmission coefficient from the transmitter inductor to the receiver inductor and S_{32} the transmission coefficient from the receiver inductor to the PDN wire, modelling the impact of both inductors. Note that both inductors induce some voltage on the power wire, yet the level of noise from the receiver is significantly lower.

To quantify this noise, the structure is simulated based on a 65 nm technology [14]. A width and spacing of $0.45 \mu m$ are used for the windings of the inductive link, while a width of $4.5 \mu m$ is used for the power loop. The structure is assumed to occupy the three topmost interconnect layers, with a thickness of $1.2 \mu m$ each and the inductor is laid out on the uppermost metal layer. The inductive link model is based on [6], where an inductor with an outer diameter of $d_{out} = 79 \mu m$ and $n = 8$ turns is implemented. Due to the symmetry of the structure, each inductor can transmit or receive data, and therefore, there is no need to add another wire beneath the inductor in

the lower tier (see Fig. 1(a)). This way the electromagnetic simulation is simplified, without sacrificing accuracy.

The amplitude of noise according to the operating frequency of the link is illustrated in Fig. 2. The solid line denotes the induced noise V_{noise} on the transmitter tier, while the dashed line is the coupling k_{13} between the transmitter inductor and the power loop. The impact from the receiver is represented with the dashdotted line.

The curves in Fig. 2 illustrate that as the operating frequency increases, the induced noise also increases. This effect is a consequence of the coupling between the transmitter inductor and the power loop. As the frequency approaches the self-resonance, the coupling between the structures increases leading to a higher level of noise. However, with increasing frequency, the input voltage wave is gradually reflected back to the source, leading to decreased transmission power. As a consequence, V_{noise} saturates above 6 GHz, the frequency this inductive link has been designed for.

Moreover, noise amplitude varies considerably with the relative location of the interconnect with respect to the centre of the inductors due to the different amount of magnetic flux flowing through the power wire. Parameter δ_c is used to notate the relative location between the power loop and the inductors where δ_c is swept within the range $[-d_{out}, d_{out}]$. Three positions with respect to the inductor, C_1 , C_2 , and C'_2 are shown in Fig. 1(b), where $\delta_{c,C_1} = 0 \mu m$, $\delta_{c,C_2} = -35 \mu m$,

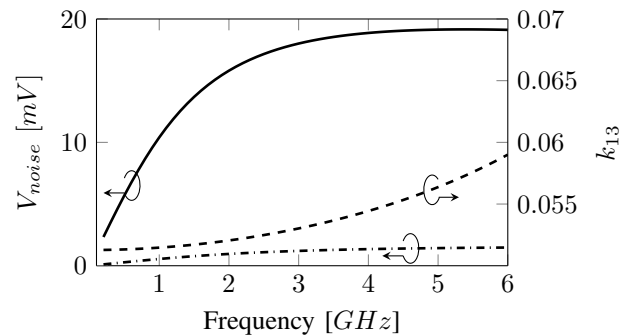


Fig. 2: Noise induced by the inductive pair and coupling coefficient between the inductor and the power wire.

and $\delta_{c,C'_2} = 35 \mu m$, respectively. For $\delta_c \geq |d_{out}|$, the amplitude of noise becomes negligible as shown in Fig. 3 by the crosshatched area. Results indicate a maximum induced noise of $V_{noise,max} = 39.5 mV$ where the power loop is close to the windings of the inductor. Nevertheless, a considerable dip on the induced noise is observed for $\delta_c = \pm 35 \mu m$, decreasing to $V_{noise,min} = 4.6 mV$.

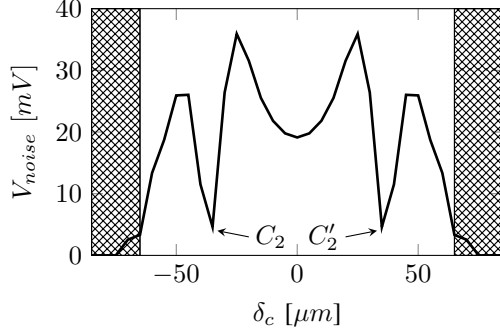


Fig. 3: Noise induced by the inductive pair, for increasing δ_c .

This outcome is due to the opposite direction of the magnetic flux between the two wires of the power loop, where the power loop is placed at either C_2 or C'_2 , as shown in Fig. 1(b). This behaviour indicates that there is no need to shift the power loop far away from the inductive link to avoid crosstalk. Instead, considering the opposite direction of coupling between the wires of the loop and the turns of the inductor leads to low crosstalk without considerably altering the design of the PDN, which can require expensive design iterations.

Although this structure is sufficient to demonstrate the harmful effects that an inductive link can have on P/G lines, a 3-D system that employs wireless inter-tier communication will utilise an array of inductors as in [7], [8]. Consequently, more than one inductor can couple with the long P/G wires, further aggravating the crosstalk noise. In this case the number of N inductors placed along the length of the power loop should be simulated to model the induced noise. However, this approach significantly increases the simulation time particularly as noise for varying frequencies and δ_c must be determined. To address this problem, the noise from a single inductor is determined where this inductor is placed successively at the location of N inductors. The accumulated noise from N inductors along the length of the loop can be described as

$$V_{noise,acc} = 2V_{noise,l} + (N - 2)V_{noise,m} \quad (2)$$

where $V_{noise,l}$ is the noise generated from the inductors placed at the edges of the loop and $V_{noise,m}$ is the noise produced by the remaining $N - 2$ inductors coupled to the loop.

To verify the accuracy and gains of this approach using (2), four ($N = 4$) inductors are assumed to couple to a power loop along the x -axis. The distance of subsequent inductors is given by $pitch = d_{out} + 30 \mu m$, with the added spacing used to reduce crosstalk between the inductors during simultaneous operation. The noise due to a single inductor

placed at specific locations along the x -axis is listed in column 1 of Table I. In columns 2 and 3, this noise is compared with the noise resulting by each of the four inductors where multiple inductors are simulated. The low error of $\sim 2\%$ and the reduced simulation time reported in the last row of Table I shows that superposing the noise due to a single inductor from successive locations along the power loop is a computationally efficient approach.

TABLE I: Noise Induced by Four Inductive Links

| x -distance, 6 GHz | V_{noise} [mV] | | Error [%] |
|----------------------|-------------------------|----------|-----------|
| | Single | Multiple | |
| $x = 0$ | 17.7 | 17.4 | 1.6 |
| $x = pitch$ | 15.1 | 15.1 | 0 |
| $x = 2 \times pitch$ | 15.0 | 15.0 | 0 |
| $x = 3 \times pitch$ | 18.0 | 17.9 | 0.5 |
| Simulation Time | 4×1 min 37 sec | 16 mins | — |

III. NOISE EFFECTS OF INDUCTIVE LINK ARRAYS

The induced voltage due to the presence of inductive links on the neighbouring lines of the power grid appears as another component of power supply noise for contactless 3-D systems. Relocating the P/G wire in a great distance from the inductors is a straightforward approach to avoid coupling. However, an increase in the IR -drop is inevitable. The tradeoff between these two different noise components (i.e., the crosstalk noise and IR -drop) is considered in this section to determine suitable locations for the P/G lines so that the overall power supply noise is restricted within acceptable limits.

An array of 4×4 inductive links is assumed, with a spacing of $30 \mu m$ between each link to reduce crosstalk during simultaneous transmission. The area of the array is $436 \mu m \times 436 \mu m$. Each inductive link consists of the transceiver and multiplexing circuits, consuming a current of $I = 7.1 mA$ [7], which are modelled as uniformly distributed current sources across the area of each inductor. The array is supplied by a power grid that utilizes the global and intermediate metal layers of a $65 nm$ technology node. The design of the grid results in an IR -drop of $13.8 mV$, which satisfies a 10% V_{dd} power supply noise constraint assumed in this case study. The power loops on the topmost global layer are illustrated in Fig. 4 as solid lines. The power loops span the entire array connecting to $C4$ bumps placed symmetrically at the periphery of the array. A spacing of $s_{C4} = 150 \mu m$ and diameter of $d_{C4} = 75 \mu m$ is assumed for the bumps, satisfying the minimum size requirements for $C4$ pads placement [15]. The surrounding $C4$ bumps are assumed to supply the total current drawn by the array of inductors at nominal $V_{dd} = 1.1 V$.

The power loops are connected to each of the supply pads through a resistance, R_{dist} . This resistance is used to model the added IR -drop as the power lines are shifted away from the pads to reduce coupling with the inductive links. To include both the inductive link noise from (2) and the additional IR -drop due to relocation of the P/G wires, R_{dist} is also described as a function of δ_c , yielding a sheet resistance of $R_{dist,pm} = 23.7 m\Omega/\mu m$. For $\delta_c = -77 \mu m$ (or $-(d_{out}/2 + d_{C4}/2)$) the

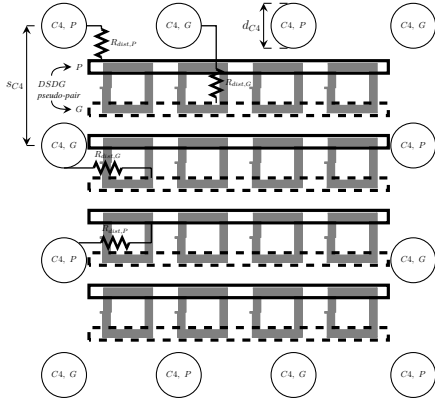


Fig. 4: Inductive link array and P/G loops connected to $C4$ supply pads (not to scale). Power and ground lines are depicted by solid and dashed lines, respectively.

power lines are aligned with the pads at the top of the array and there is no added resistance ($R_{dist} = 0$). As the wires are shifted away from the pads, R_{dist} increases, reaching a maximum of 3.8Ω for $\delta_c = d_{out}/2 + d_{C4}/2$.

The accumulated noise from a row of the inductive link array and the IR -drop is illustrated in Fig. 5. The dashed line denotes the noise of an inductor at the edge of the array while the dashdotted line exhibits the noise of an inductor at the middle of the line. The IR -drop is superimposed on both curves. The solid line is the overall noise for a row of the inductor array using Eq. (2) where $N = 4$.

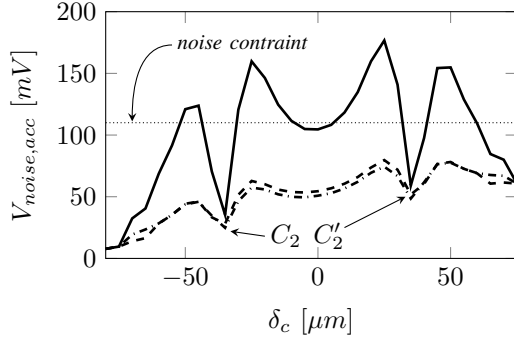


Fig. 5: Parasitic noise induced on the power wire, depending on the spatial alignment of the wire to the inductor.

Spatial alignment of the power grid over certain positions, such as C_2 and C'_2 depicted in Fig. 1(b), results in minimum noise caused by the inductor. The corresponding minimum noise positions for this case study are also shown in Fig. 5, for different δ_c . As mentioned in Section II, at these positions the opposite polarity of coupling to each wire of the loop greatly reduces the noise. The accumulated voltage noise of C'_2 , nevertheless, is slightly higher than C_2 , due to the greater IR -drop as the power wires are shifted away from the power pads to reduce the induced noise. A similar analysis applies for the ground grid (depicted with dashed lines in Fig. 4).

Considering the first row of inductive links as seen in Fig. 4, the power loop is placed at position C_2 , yielding a total noise level of $V_{noise,C_2} = 35.4 \text{ mV}$. Moreover, the ground loop can be placed at C'_2 , where the accumulated noise level is $V_{noise,C'_2} = 59.1 \text{ mV}$, increased due to the increased IR -drop.

The overall supply noise is no higher than 8.16%. Although the initial placement of power grid lines exhibits low IR -drop, the induced noise can reach $V_{noise,max} = 320 \text{ mV}$, assuming the worst case for both the power and ground loops, violating the allowed power supply noise constraint. Therefore, proper placement of the power grid can satisfy a low noise constraint, despite interference from the inductive link interface.

IV. CONCLUSION

The impact of an inductive link interface on power delivery networks is investigated. A fast and accurate method is presented, providing the induced noise of multiple inductors in a P/G loop. Furthermore, considering the trade-off between the noise induced by the inductive link and the IR -drop on the wire, locations less susceptible to crosstalk and IR -drop noise are determined. Analysis has shown that the best position for placing a PDN loop is on each side of the inductor windings, where the magnetic flux of each side cancels out, without prohibitively increasing IR -drop. Results show that with this analysis the target noise constraints can be met.

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