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A Single Switcher Combined Series Parallel Hybrid Envelope Tracking Amplifier for Wideband RF Power Amplifier Applications

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Abstract

In this paper, an improved architecture for RF power amplifier envelope tracking supply modulator is presented. It consists of a single switched mode supply regulator and one linear regulator. The switched mode supply regulator has two outputs, one of which is used in conjunction with the linear regulator to provide a wideband, high efficiency power supply to the RF amplifier, whereas the second output provides a band limited high efficiency supply to the linear regulator. The design offers improved power efficiency, reduced system complexity and area savings since the dual output switched mode regulator requires one inductor and a simple control loop. The design was implemented in 14nm CMOS process and validated with simulations. The supply modulator achieves a peak efficiency of 74% with a 6 dB PAPR 20MHz LTE signal at 29dBm output power.

Keywords

RF; power amplifier; supply modulator; envelope tracking; 4G LTE

I. Introduction

Due to ever increasing demand for mobile broadband services with higher data rates and limited spectral resources, 3G communication systems and beyond (WCDMA, LTE) use higher peak-to-average power ratio (PAPR) signaling [1]. For conventional fixed supply power amplifiers (PA), depicted in Fig. 1(a), high PAPR signals force the PA to operate at large power back-off levels in order to satisfy strict linearity requirements, leading to high power losses and low efficiency.

To address this issue, several PAs with dynamically changing supplies have been proposed [2–5]. One such system that has received great attention is the envelope tracking system (ET) depicted in Fig. 1(b). It improves efficiency by continuously adjusting the PA's supply voltage according to the baseband signal envelope, thereby biasing the PA consistently near saturation as represented in Fig. 2. The power spectral density of a 20 MHz LTE envelope signal is shown in Fig. 3. For such wideband signals, the high efficiency of a switch mode

power supply (SMPS) is needed to provide majority of the power near DC, while the high bandwidth, less efficient linear regulator would be ideal for providing the remaining power at far off frequencies.

Hybrid ET amplifier (Fig. 4) [4], which consists of a linear regulator in parallel with a switching stage shows the greatest potential for efficient PA supply modulation of 4G signals and beyond. The main source of inefficiency in this architecture is the power loss in the output stage of the linear regulator. This is because the instantaneous efficiency of the linear regulator is proportional to the ratio of peak output to supply voltage.

Given the high PAPR and PSD of LTE signals, the linear regulator operates in its low efficiency region with high probability. Recent work has attempted to improve efficiency of the hybrid ET amplifier by adding an additional SMPS to modulate the supply of the linear regulator [6]. Although this technique offers efficiency improvement, it is very costly in terms of added complexity, power consumption and area due to the extra inductor of the additional SMPS. A better approach would be to use a single SMPS to supply both the PA and linear regulator. This would allow for power and area savings because of inductor sharing.

This paper presents an improved hybrid ET amplifier for wide band signals. A single SMPS is used to regulate the supply of the RF PA working in parallel with a linear regulator. The same SMPS also regulates the supply of the linear regulator in order to minimize power losses and improve

II. SYSTEM ARCHITECTURE

The proposed architecture is shown in Fig. 5. It is composed of a linear regulator in parallel with a SMPS that regulates two outputs instead of one. The highly efficiency SMPS provides majority of the low-frequency power to the RF PA via (V_{out1}), which is controlled by the sensed current flow out of the linear regulator. The linear regulator provides the high-frequency current to the PA. Feedback around the linear regulator acts to minimize the current it provides. Additionally, low impedance of the linear regulator's output absorbs the switching ripple of V_{out1}. The second SMPS output (V_{out2}) provides an envelope dependent variable supply to the linear stage, thereby reducing losses in the linear regulator's output stage. V_{out2} is controlled by a band limited (2 MHz) version of the base band envelope injected into the SMPS's inductor from the main power rails, whereas M4 discharges the inductor to ground when M1 is off. M3 and M4 controlled by S2 and S2b distribute the inductors current to the two output loads in accordance to the required current as weighted by the error signals (ERR1 and ERR2). In order to track the LTE envelope signal, fast switching is required, hence the loop filter's cut off frequency is set to 30 MHz and switching frequency is 150 MHz.

III. Implementation

Circuit implementation of the single inductor dual output SMPS and modulated supply linear regulator are discussed below. Direct current sensing was used to minimize path delays and follows the design in [7].

A. Variable Supply Linear Regulator

Simplified schematic of the linear regulator is shown in Fig. 6. It is a three-stage, class-AB design with nested miller compensation based off design in [8]. Devices M0 – M10 form the input folded cascade stage, which provides high gain. M11 – M17 form the second transconductor stage, which transforms the output voltage of first stage into a current that is mirrored into the output stage using M18 and M19. The first and second stages uses stacked transistors to produce high gain and is supplied by the 3.3 V main rail. The Class-AB output stage (shaded in grey) is supplied by the SMPS (Vout2) terminal and is capable of operating in saturation with a supply voltage as low as VT+2VDSsat (where VT is the threshold voltage and VDSsat is the minimum drain-source voltage). Compensation capacitor Cc sets the gain bandwidth of the amplifier, whereas the parasitic capacitance of the output devices PM1 and PM2 compensate the output stage. The linear regulator's efficiency is given by (1)

$$\eta = \frac{V_{OUT}}{V_{IN}}\% \quad (1)$$

Therefore, the linear regulator's efficiency drops sharply at lower output voltages, or backoff power levels. In order to minimize the power losses, the output of the linear regulator needs to track its supply voltage closely, in fashion similar to supply modulation of the RF Envelope tracking PA.

B. Single Inductor Dual Output Regulator

The single inductor dual output SMPS is shown in Fig. 7. The inductor L is connected to the outputs (V_{out1}) and (V_{out2}) via MOS switches M3, M4. Vout1 delivers current to the RF PA, whereas Vout2 powers the output stage of the linear regulator. Storage capacitors C1 and C2 act as filters for the outputs and deliver power to the loads when the control loop directs the inductor current from one output to the other. Two feedback loops control the switching behavior of the SMPS and current sharing of the inductor between the two loads. Two pulse width modulation (PWM) signals (S1 and S2) are produced by error amplifiers AMP1 and AMP2, combined with comparators CMP1 and CMP2 and the triangular waveform generator. M1, controlled by S1, regulates the amount of power injected into the SMPS's inductor from the main power rails, whereas M4 discharges the inductor to ground when M1 is off. M3 and M4 controlled by S2 and S2b distribute the inductors current to the two output loads in accordance to the required current as weighted by the error signals (ERR1 and ERR2). In order to track the LTE envelope signal, fast switching is required, hence the loop filter's cut off frequency is set to 30MHz and switching frequency is 150MHz.

IV. Simulation

The proposed supply modulator was designed in 14nm HV process and validated through simulations. Fig. 8 demonstrates the transient tracking capability of the design for a 20 MHz LTE test envelope. All simulations used a 4.4 Ω resistive load corresponding to 29.5dBm RF output power. The simulated time domain Vout1 waveform tracks the envelope signal with high fidelity even during sharp deeps. Propagation delay is constant which allows for

accurate envelope reconstruction. The second SMPS output (Vout2) which supplies the linear regulator's output stage also follows the band limited envelope signal accurately.

Fig. 9 represents a typical transient response of a 29.5dBm, 2MHz SSB suppressed carrier envelope waveform. Table I summarizes the simulated performance of the supply modulator with a resistive load. Fig. 10 shows the simulated efficiency versus output power for modulator presented in this work and in [5, 6]. The new approach provides a 6% and 20% improvement at 28dBm and 18dBm output power respectively compared to [5]. Data provided by [6] is limited to high output power and does not include the power consumption of the external high precision switched mode supply. Layout of the proposed amplifier is provided in Fig. 11.

V. Conclusion

An improved hybrid, serial parallel PA supply modulator has been presented. It features a single inductor dual output switch mode regulator and a variable supply linear regulator. One output of the switch mode regulator, modulates the RF PA supply in parallel with the linear regulator. The other output of the switching regulator is used to modulate the supply to the output stage of the linear regulator, in order to reduce power losses in the linear regulator's output stage and improve overall efficiency. The design allows for considerable die and system level area savings since no additional high accuracy switching regulator and inductor are needed. The supply modulator was designed in 14nm HV process and validated with simulations. It offers accurate envelope tracking of a 20 MHz LTE envelope signal with peak output power of 30.5dBm.

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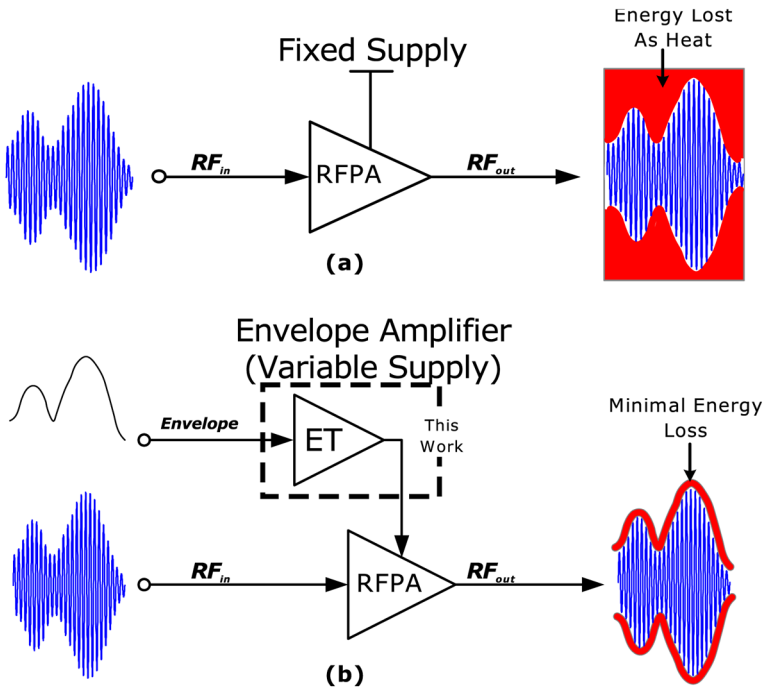

Fig. 1.

(a) Fixed power supply (b) envelope tracking supply modulation scheme in RF PAs.

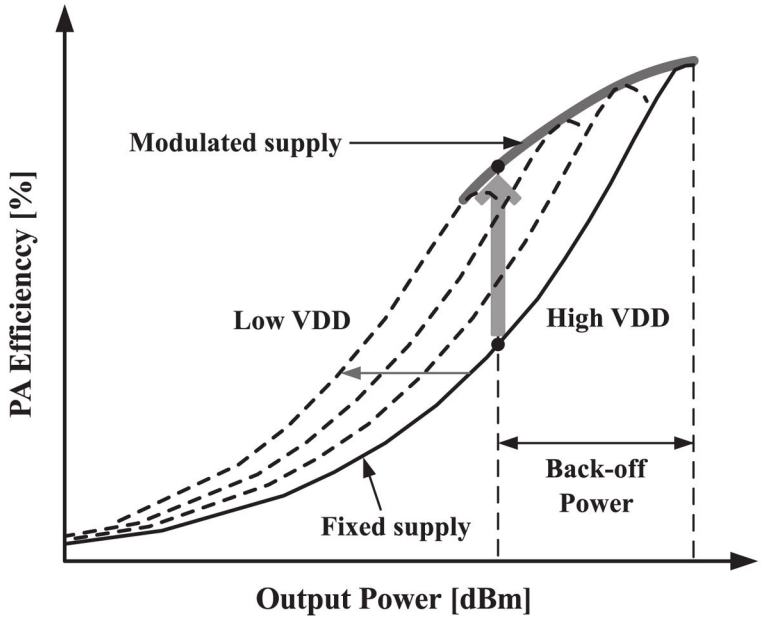

Fig. 2.

Efficiency as a function of output power for an envelope tracking system. VDD is continuously adjusted to achieve optimum efficiency at each output power.

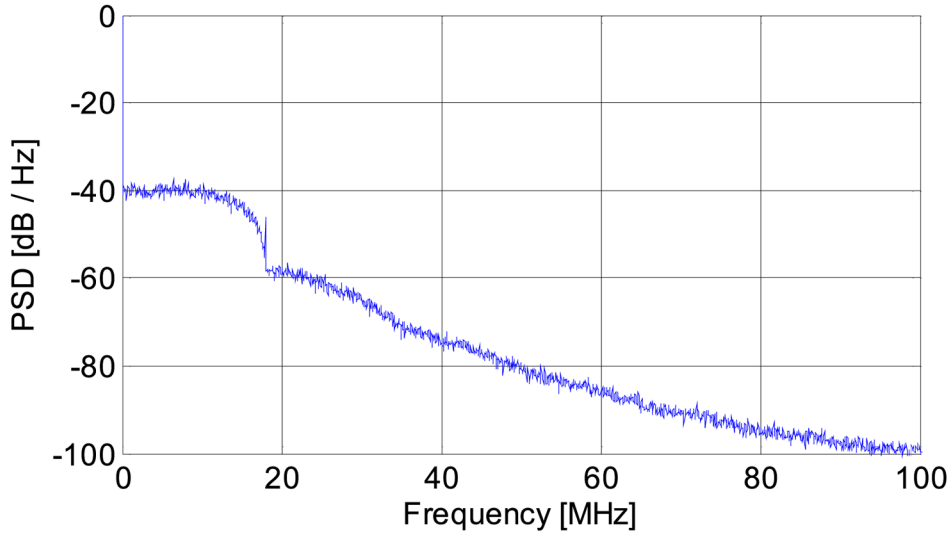

Fig. 3.
Power spectral density (PSD) of the envelope signal for 20 MHz LTE.

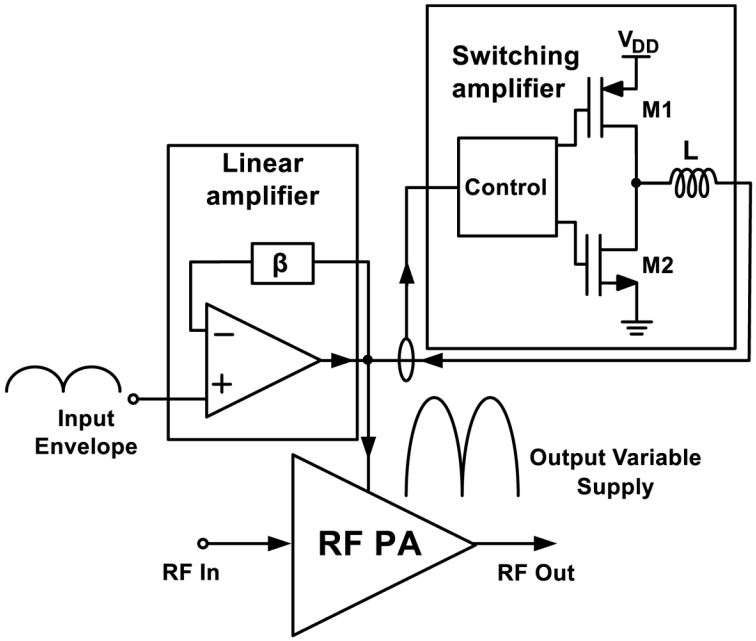

Fig. 4.
Hybrid parallel envelope tracking amplifier.

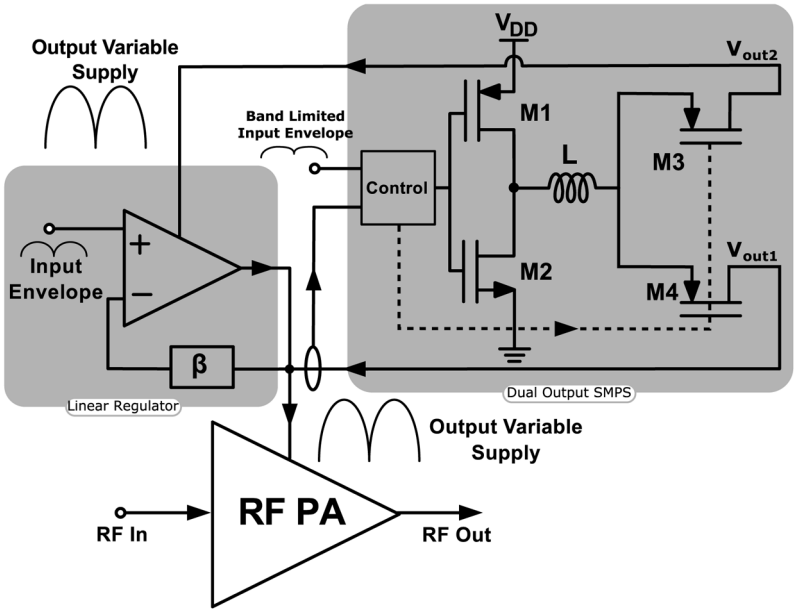

Fig. 5.
Proposed single switcher combined series parallel hybrid envelope tracking amplifier.

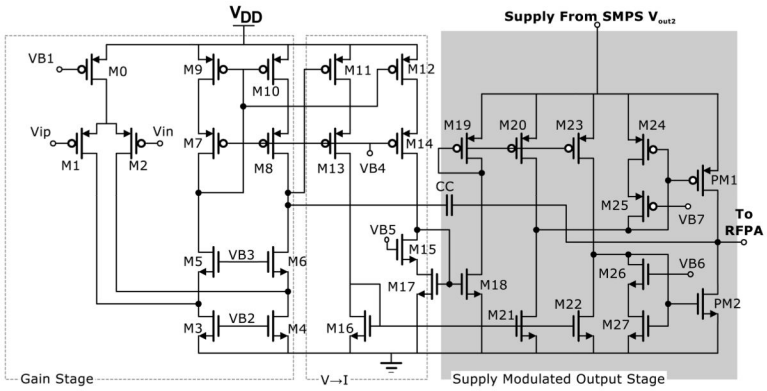

Fig. 6.

Simplified schematic of the linear regulator with adjustable output stage voltage supply.

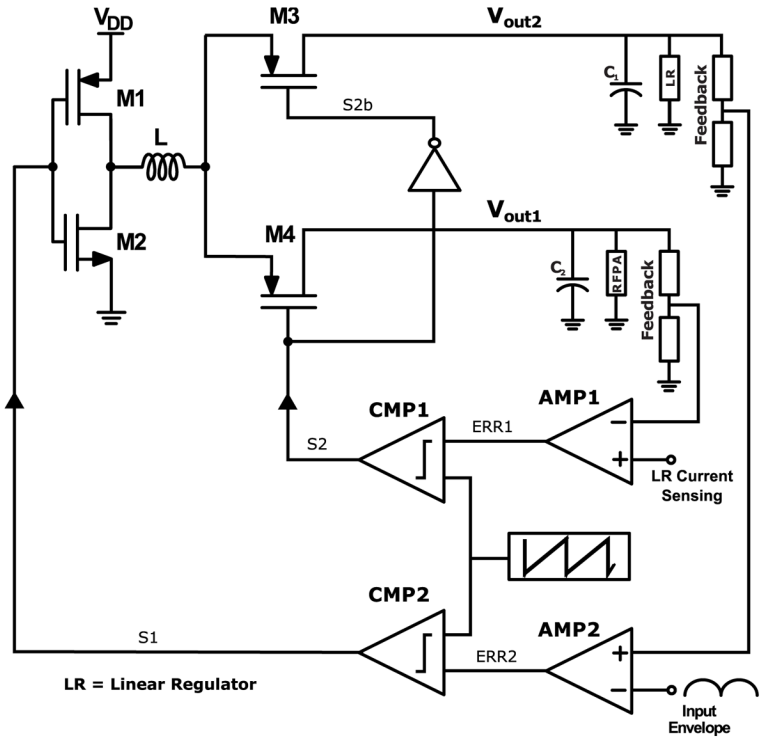

Fig. 7.

Single inductor dual output switched mode power supply.V_{out1} regulates the RFPA supply.V_{out2} regulates the linear regulator's output stage supply.

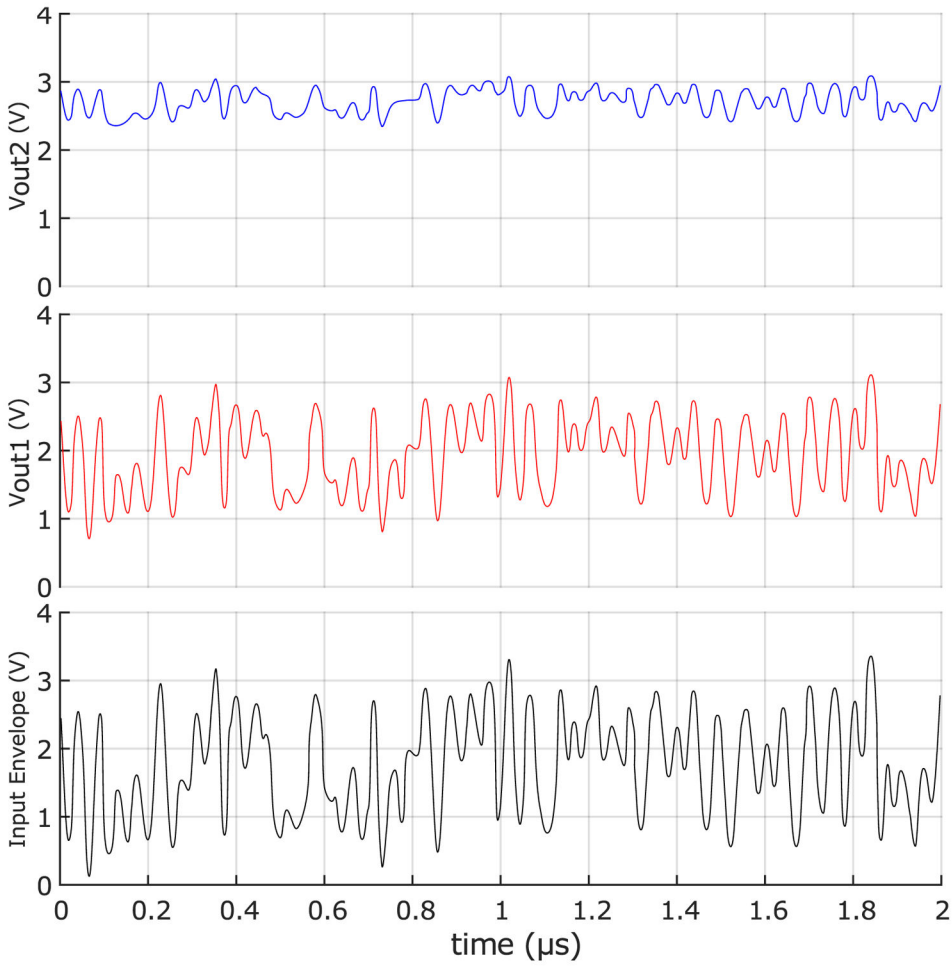

Fig. 8.
Transient tracking of a 20MHz LTE test envelope.

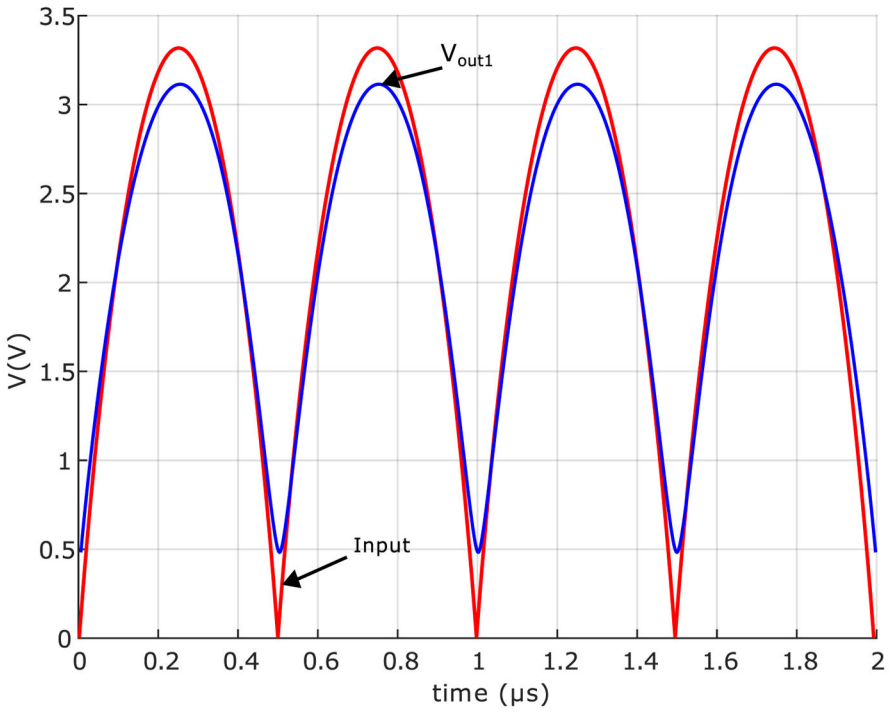

Fig. 9.
Transient response for a 2MHz fully rectified sine wave.

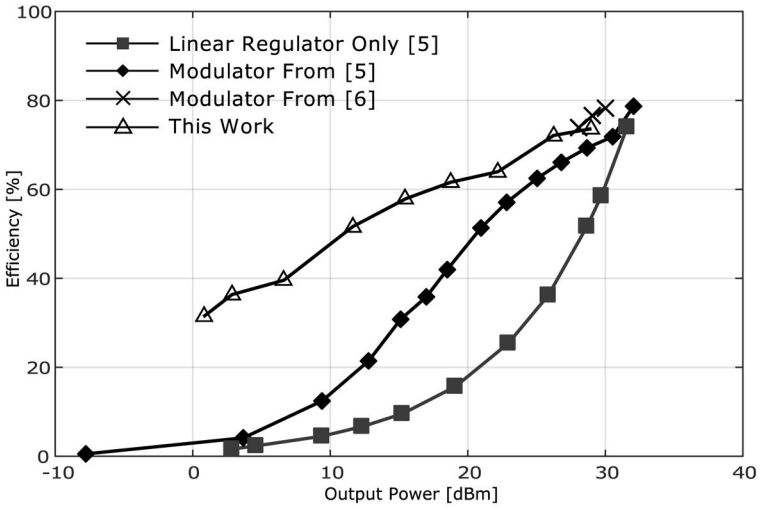

Fig 10.
Efficiency comparison at different load levels.

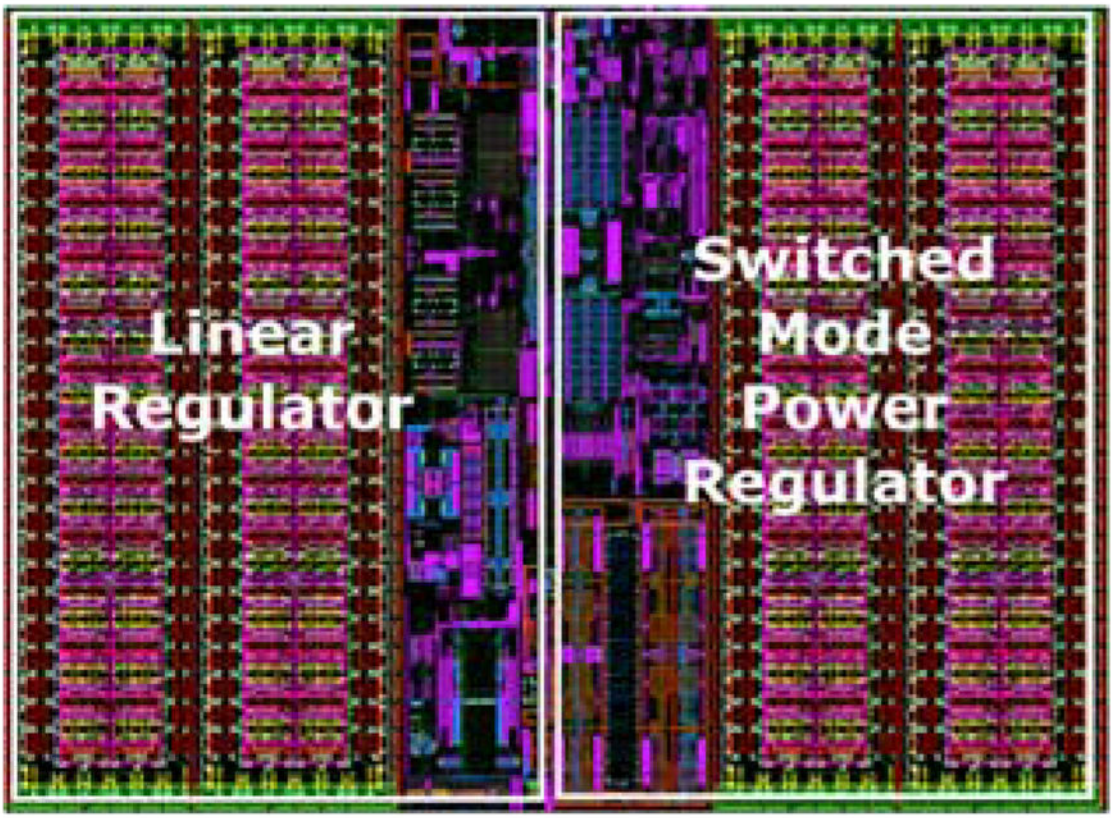

Fig. 11.
Layout of the proposed envelope tracking amplifier.

Table 1

Performance Summary

Process	14nm HV CMOS
Layout Area (μm)	250 × 230
Supply Voltage (V)	3.3 I/O, 1.05 Digital
Max. Switching Frequency (MHz)	150
Max. Efficiency (%)	74%
Regulated Output (V)	0.5 – 3.1
Max Load Current (A)	1.0
Max Output Power (dBm)	30.5