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An Enhanced Light-Load Efficiency Step Down Regulator with Fine Step Frequency Scaling

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Abstract

This paper presents a switching DC-DC Buck converter with enhanced light-load efficiency for use in noise-sensitive applications. Low noise, spur free operation is achieved by using a sigma-delta-modulator (ΣΔ) based controller, while light load efficiency is realized through the introduction of fine step frequency scaling (FSFS) which continuously adjusts the switching frequency of the converter with load conditions. Regulation efficiency is further improved by adoption of mode hopping (continuous conduction mode (CCM)/discontinuous conduction mode (DCM)) and utilization of a fully digital implementation. Furthermore, the presented converter maintains low output voltage ripple across its entire load range by reconfiguring the ΣΔ modulator's quantization step and introducing dither to the loop filter. The proposed modulator was implemented in 14nm bulk CMOS process and validated with post layout simulations. It attains a peak efficiency of 95% at heavy load conditions and 79% at light loads with a maximum voltage ripple of 15mV at light loads.

I. Introduction

Demand for on-chip power management systems has increased tremendously due to the exponential growth of portable consumer devices (cell phones, medical devices, tablets… etc). Step down DC-DC (buck) converters constitute the backbone of such systems, with the overwhelming majority of commercially available parts having analog implementation of the loop controller. An all-digital implementation of the control loop offers several advantages compared to analog control. These include low sensitivity to component mismatch and process variation, ease of reconfiguration and portability to advance digital processes.

Conventional pulse-width-modulation (PWM) loop control suffers from low light-load efficiency [1]. To address this drawback, pulse-frequency modulation (PFM) control, which reduces the switching frequency in proportion to load current has been used [1,2]. However, PFM control losses increase dramatically with load current and is therefore limited to operation at light loads. A technique often used to improve the efficiency over the entire loading range is to use both PWM and PFM control in a hybrid configuration [2,3]. Both PFM and PWM controllers inherently generate tonal spurs that couple to the load and other

blocks on the same substrate, degrading system performance. This is a particular problem for systems-on-chip (SoC) that house noise sensitive mixed-signal, RF and sensing subsystems on the same die [3,4]. This necessitates the use of off-chip high-Q filters which increase system cost and footprint or spread spectrum techniques the reduce efficiency [4,5]. Switching buck converters controlled by ΣΔ modulators make use of the noise shaping capability of the modulator's loop filter, and the variable output duty cycle to reduce both the harmonic tones in the output and the electromagnetic interference (EMI) produced by the converter itself.

Previously reported ΣΔ based buck converters have utilized the ΣΔ modulator to either increase the resolution of the PWM controller [6], or replace it all together [4,7]. However, with ΣΔ resolution enhanced PWM controllers, the tonal noise problem is not resolved as the PWM block still generates spurious spectral power [6]. Additionally, recent work on ΣΔ based controllers has relied on purely analog implementations (discrete time or continuous time) which are power hungry and not amenable to process portability or re-configurability [4]. Moreover, efficiency at light load conditions has not been adequately addressed since ΣΔ based controllers have the same efficiency characteristic as PWM controllers [7]. Another issue with the previously reported work is the requirement for higher values for passive components (L, C) in order to smooth out high voltage ripple at light loads [4].

This paper presents a DC-DC buck converter that uses a 2nd order ΣΔ modulator controller to achieve spurious-tone free regulation, and is therefore suited for noise sensitive applications. It also features circuits that continuously monitor and modify the regulator's switching frequency as well as operational mode (continuous conduction mode (CCM) for heavy loads and discontinuous conduction mode (DCM) for light loads) in order to maintain high efficiency across wide load conditions. Additionally, the ΣΔ controller quantization resolution is increased and dithering enabled at lower sampling frequencies (while regulating light loads) to reduce output ripple without the need for big passive components. In contrast to previous work, the proposed regulator's switching frequency is adjusted continuously in fine steps (FSFS) in order to ensure the most optimal efficiency vs. load performance profile. The entire regulator including the digitizers are implemented digitally.

Section II describes the proposed architecture whereas implementation is provided in section III. Transistor level simulations are presented in section IV, and finally conclusions in section V.

II. Proposed Architecture

A block diagram of the proposed buck converter is shown in Fig. 1. It can be divided into two main parts: power stage and digital loop controller. The power stage consists of switches S1 (PMOS) and S2 (NMOS), an off-chip passive low pass filter (L, C) which connects the switcher (S1 and S2) to the load, and the power stage drivers and dead time generator which drive the switcher. (Vin) is the unregulated power supply. The digital controller consists of digitizers ΣΔFDC1 and ΣΔFDC2, PID compensator, and ΣΔ modulator. Operational mode and frequency control are handled by the output current sensor and FSFS blocks.

Operation is as follows, the scaled output (V_{fb}) and reference (V_{ref}) voltages are digitized using ΣΔFDC1 and ΣΔFDC2 respectively, the digital difference (V_{err}) is processed by the proportional-integral-differential (PID) compensator. The output of the PID compensator is fed to the digital ΣΔ modulator which generates the duty cycle command that drives the power stage drivers. The current mirror based current sensor provides a read out of the load current by dropping a scaled down copy of the current on a sense resistor (not shown). The resulting voltage signal is digitized using ΣΔFDC3 and low pass filtered using a moving averager. The output digital code word is then used to configure the FSFS unit to divide the master clock down to the appropriate value and configure the controller to operate in either CCM/DCM mode. It also enables digital dithering in the ΣΔ modulator to reduce the output ripple in DCM mode.

III. Implementation

Implementation of the regulator's main blocks are discussed in the sections below. The PID follows the design methodology in [5].

A. Analog to Digital Converters

ΣΔ frequency Discriminators (ΣΔFDC) are used to implement ADCs 1, 2 and 3. These 1st order, digital, none feedback modulators, process an FM input signal to produce a single bit output stream [8]. Compared to conventional nyquist rate A/D architectures, ΣΔFDC have simpler circuits, and are more power efficient and inherently linear by virtue of using a single bit comparator. A schematic of the ΣΔFDC is shown in Fig. 2. The modulator consists of a voltage controlled oscillator (VCO), two D flip flops and one XOR gate. Decimation of ΣΔFDC1 and 2 outputs is implemented using CIC filter, whereas ΣΔFDC3 uses a counter based averager (N is the number of sampling clock cycles, 1024 for a 10 bit output code word). Resolution of the ΣΔFDC (n_{adc}) is given by:

$$n_{adc}=int\left[\log_2\left(\frac{V_{max,adc}}{V_{ref}}\cdot\frac{V_{fb}}{\Delta V_{fb}}\right)\right] \quad (1)$$

Where, V_{fb} is the scaled regulated output voltage, ΔV_{fb} is the error of the scaled output voltage, and $V_{max,adc}$ is the full scale voltage of the ADC (conversion in the range from 0 to $V_{max,adc}$). Operation is as follows: V_{fb}, $V_{ref,}$ and V_{sense} are inputs to current starved and matched VCOs of ΣΔFDC1, 2, and 3 respectively. The FM modulated outputs of the VCOs are processed by the 1st order ΣΔFDCs whose outputs are decimated by the output digital filters.

B. Digital Sigma Delta Modulator

Implementation of the 2nd order ΣΔ digital modulator is shown in Fig. 3. Fast response, spur free operation is achieved by eliminating a subsequent fast sampling rate and power inefficient DPWM stage [6]. A 2nd order modulator was chosen as a tradeoff between, noise shaping capability, power efficiency and stability. A feed forward (CIFF) topology with a non-delaying first stage integrator, and a delaying second stage integrator was used. This

design allows for simple regulator loop compensation because the signal transfer function of the modulator is unity, hence the only phase shift introduced by the modulator into the loop's transfer function is the delay term of the second integrator ($360 f_C T_S$) where T_S is the period of switching frequency f_s and f_C is the regulator's cutoff frequency. This is important since it permits the scaling of the regulator's loop frequency without the need to adjust the PID's frequency response. Additionally, this topology offers power savings by virtue of reduced internal node switching activity, since the loop filter in a CIFF topology processes the quantization error signal only. Recently reported regulators that use mode hopping (DCM mode at light loads) suffer from significant increase in output ripple at steady state (1300% as in [4]). Output ripple increases with the slower clock speeds required to reduce switching and gate-drive losses. To address this issue, multi-bit quantization is enabled at low f_s (2 bit feedback in the ΣΔ modulator). Additionally, the FSFS block (presented in the following section) provides a dither signal to the ΣΔ modulator to randomize its output at low clock speeds. Multi-bit quantization coupled with the dither signal, applied to the modulator's second stage LSB, effectively randomize the modulator's output when operating in DCM mode and low f_s thereby increasing the output switching activity level and reducing V_{out}'s ripple amplitude.

C. Fine Step Frequency Scaling and mode control (FSFS)

The FSFS block allows for continuous tracking of the regulator's most efficient switching frequency, especially in DCM mode were fine frequency stepping is needed for improved efficiency [4]. Diagram of the FSFS controller is shown in Fig. 4. It is composed of a 10-bit prescalar, a DCM/CCM mode selector and ΣΔ modulator configuration and dithering blocks. The programmable prescalar is a modified structure based of the design in [9] and is composed of cascaded divide-by-2/3 stages. It acts as counter of the number of (f_{clk}) cycles – as dictated by load sensing control <CTRL0:9> - and outputs a slower cycle (f_s) once the count is achieved. Output clock period is given by (2):

$$T_{out}=(2^k+2^{k-1}.CTRL_{k-1}+2^{k-2}.CTRL_{k-2}+\cdots+2.CTRL_1+CTRL_0)\times T_{in} \quad (2)$$

For our implementation, 9 divide-by-2/3 were used, providing a continuous integer division factor range of 2 to 1023.

Additional combinational logic is used to extend the functionality of the block to generate a random number sequence for dithering the ΣΔ modulator and to power-gate every divide-by-2/3 stage that is not enabled in order to improve efficiency. F_{clk} is a fixed 200MHz clock, whereas f_s is variable, therefore the FSFS controller continuously adjusts the regulator's switching frequency according to load conditions by adjusting the sampling frequency (f_s)of the ΣΔ modulator, and the feedback/reference digitizers.

IV. Simulation

The proposed regulator was implemented in 14nm bulk CMOS digital process (3.3V I/O, 1.05V digital) and validated with post layout simulations. The designed converter regulates an input supply range of 1.6V to 3.3V with output load current of 1mA to 1A and regulated

output supply line of 0.5V to 2.5V, making it suitable for portable applications. Fig. 5 shows the simulated power efficiency of the proposed converter for different modes of operation. Operation in static CCM mode with a fixed sampling frequency provides high efficiency at heavy load conditions compared to the low efficiency at light loads. This is due to the switching and gate drive losses dominating at light loads. These losses are effectively minimized by operating the regulator in DCM mode at light load conditions. Continuously adjusting the sampling frequency using fine step frequency scaling (FSFS) allows for considerable efficiency improvement at extreme light load conditions (sub 10mA), compared to operation in DCM mode with a preset sampling frequency [4]. This is particularly relevant to portable applications which operate most of the time in standby mode under light loading conditions.

Fig. 6 demonstrates an example of mode hopping and frequency transition operation. Although reduction of sampling frequency invariably leads to reduction in switching frequency and increased output ripple in conventional PWM/PFM controlled converters [6], the presented regulator mitigates this effect by increasing the ΣΔ modulator's quantization resolution and maximizing the output sequence length using dithering to increase switching activity. Key performance metrics are provided in Table 1. Layout of the proposed converter is provided in Fig. 7.

V. Conclusion

A fully digital DC-DC Buck converter intended for portable applications was presented. It features a ΣΔ modulator based loop controller for spur free operation and introduces fine step frequency scaling (FSFS) for light load efficiency enhancement. Mode hopping (CCM/DCM) is also implemented to further improve efficiency. Output voltage ripple is minimized in DCM mode without the need for large passives by increasing the ΣΔ modulator's internal quantization resolution and dithering its second stage integrator. The proposed converter was implemented in 14nm bulk CMOS process and validated with post layout simulations. It attains a peak efficiency of 95% at heavy load conditions and 79% at light loads with a maximum voltage ripple of 15mV at light loads.

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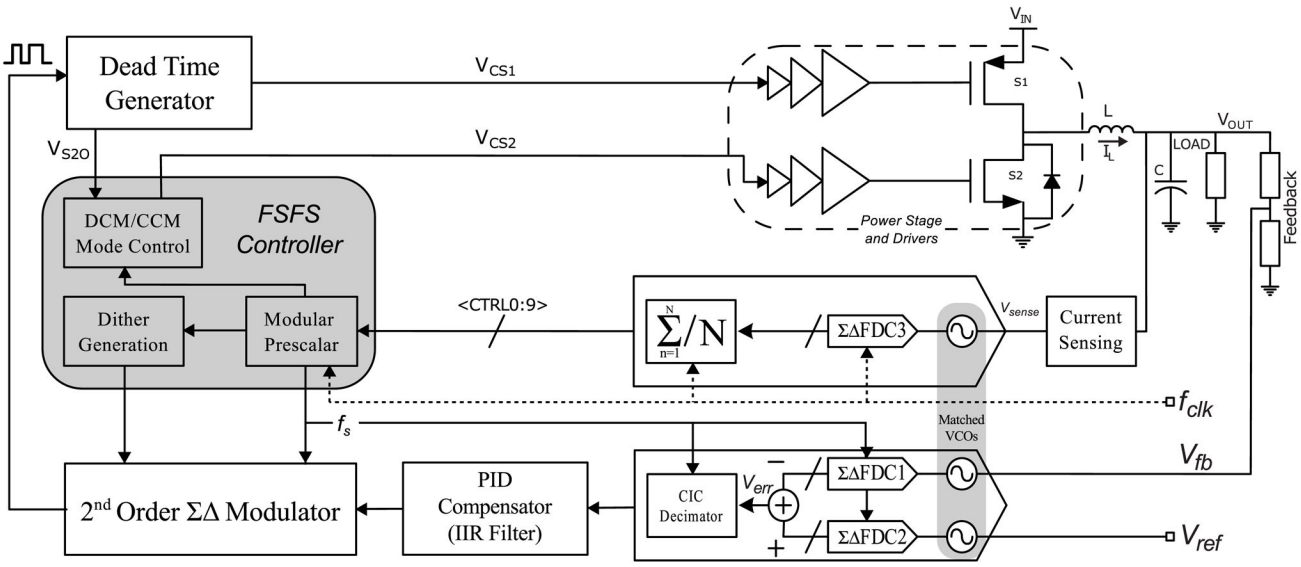

Fig. 1.
Proposed fully digital architecture of the DC - DC regulator.

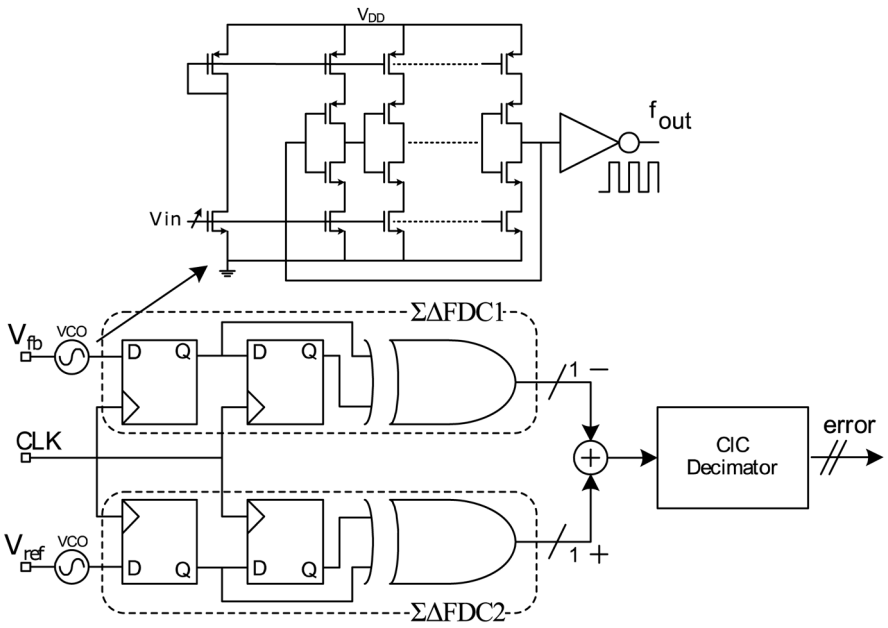

Fig. 2.

Gate level implementation of V_{fb} and V_{ref} digitizers. Current-starved VCOs are used as voltage-to-frequency converters.

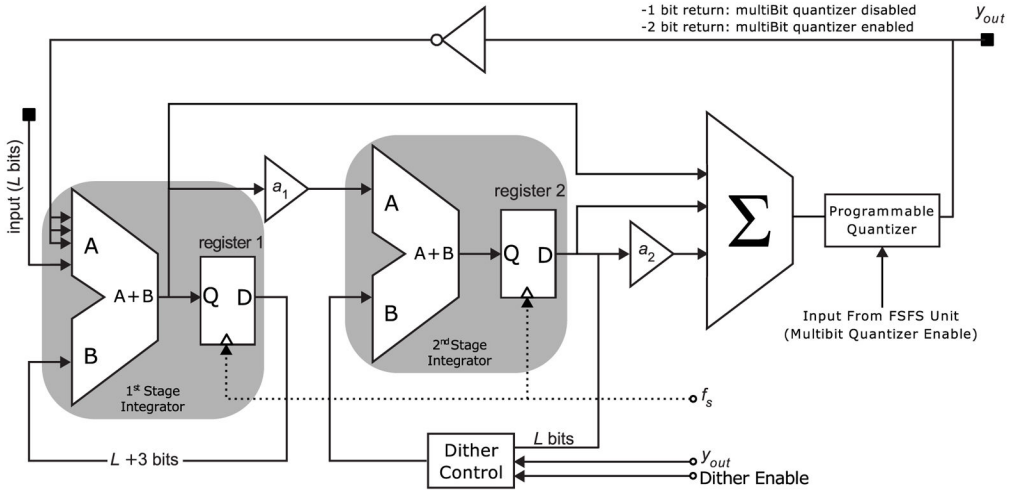

Fig. 3.
Proposed 2nd order digital ΣΔ modulator architecture.

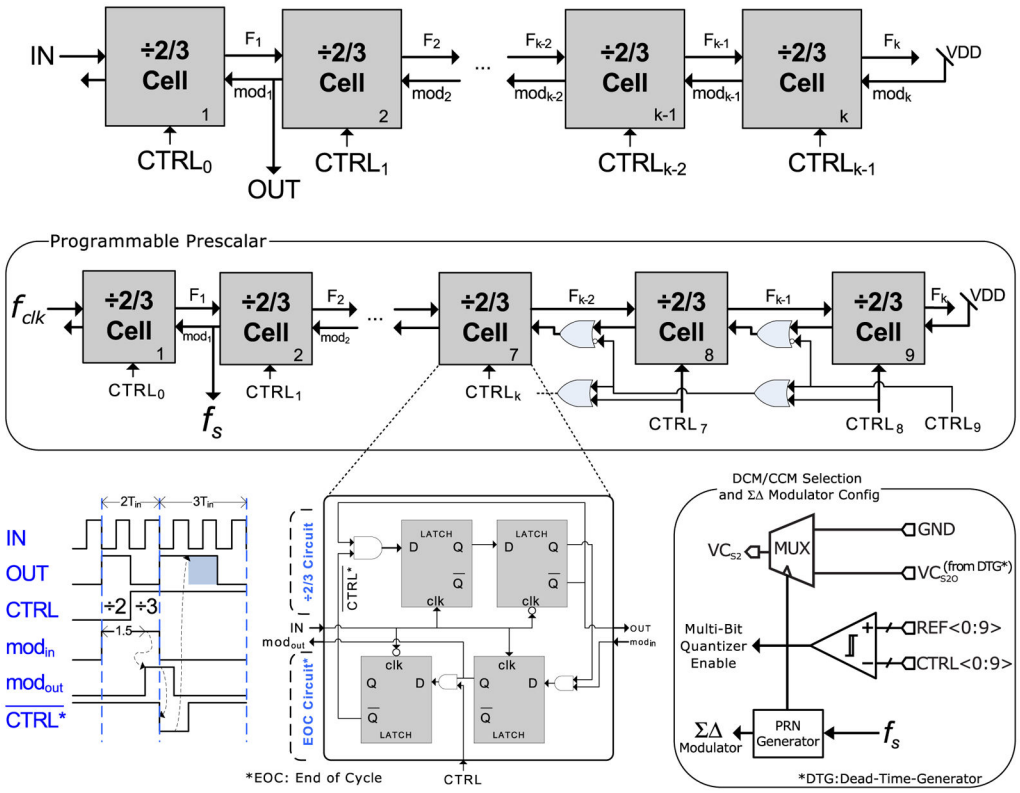

Fig. 4.
Implementation of the FSFS unit.

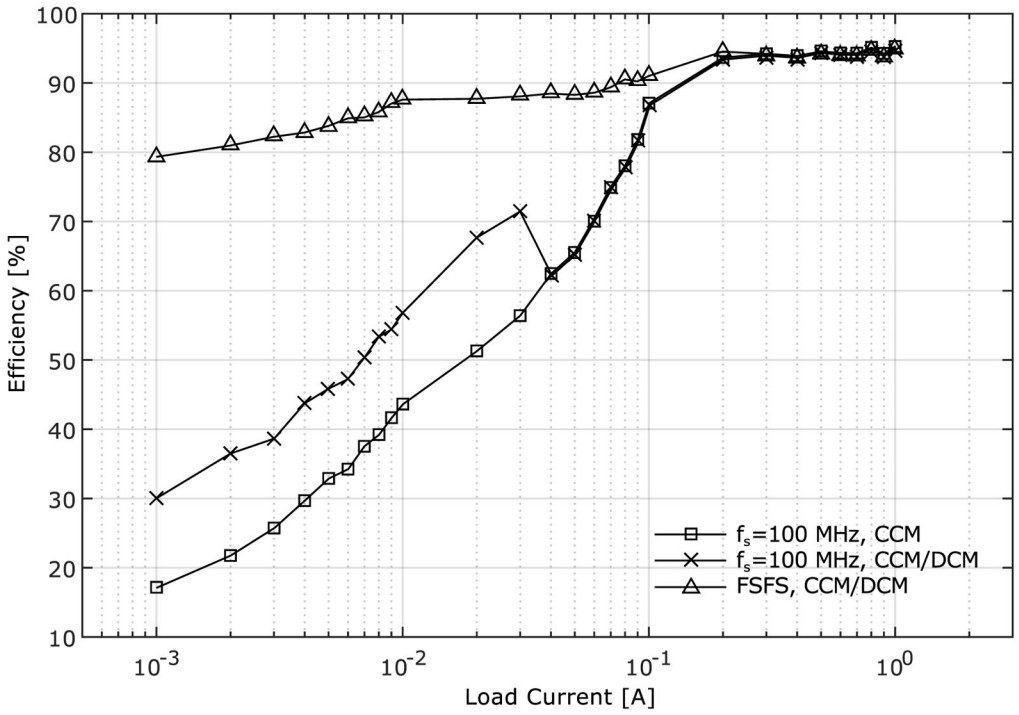

Fig. 5.

Simulated efficiency of the proposed buck converter in different operational modes. V_{IN} = 3.3V, V_{OUT} = 1.05V.

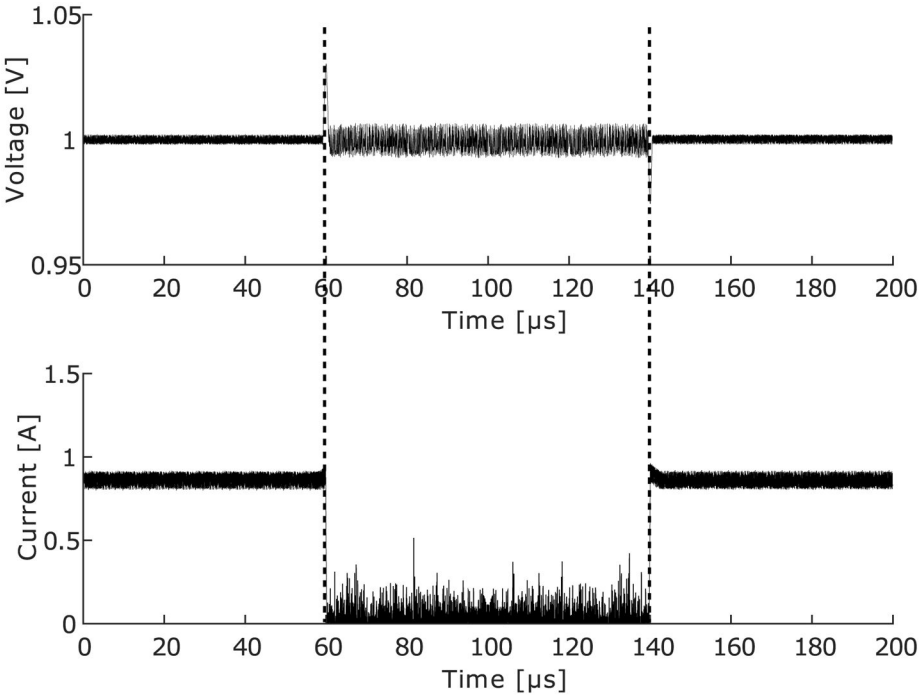

Fig. 6.

Mode and frequency transition transient simulation. I_{Load} transitions from 850mA (CCM at f_s = 16.4MHz) to 50mA (DCM at f_s = 2.5MHz). V_{IN} = 2.8V, V_{out} = 1.0V.

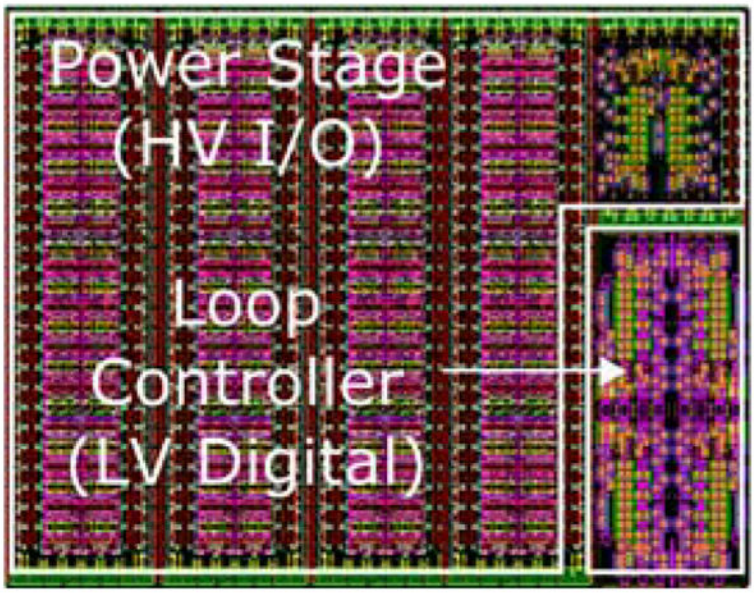

Fig. 7.
Layout of the proposed digital buck converter.

Table 1

Key Performance Summary

Process	14nm CMOS
Layout Area (μm)	150 x 130
Supply Voltage (V)	3.3 I/O, 1.05 Digital
ΣΔ Sampling Frequency (MHz)	0.5 – 100
Max. Efficiency (%)	95
Regulated Output (V)	0.5 to 2.5
Load Current (mA)	1 to 1000
Output Ripple (mV)	5 at 1A, fs = 100 MHz. 15 at 100mA, fs = 4 MHz
Output Noise (dBm)	−70 at 20mA, −90 at 800mA