Privacy Leakages in Approximate Adders

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Abstract-Approximate computing has recently emerged as a promising method to meet the low power requirements of digital designs. The erroneous outputs produced in approximate computing can be partially a function of each chip's process variation. We show that, in such schemes, the erroneous outputs produced on each chip instance can reveal the identity of the chip that performed the computation, possibly jeopardizing user privacy. In this work, we perform simulation experiments on 32-bit Ripple Carry Adders, Carry Lookahead Adders, and Han-Carlson Adders running at over-scaled operating points. Our results show that identification is possible, we contrast the identifiability of each type of adder, and we quantify how success of identification varies with the extent of over-scaling and noise. Our results are the first to show that approximate digital computations may compromise privacy. Designers of future approximate computing systems should be aware of the possible privacy leakages and decide whether mitigation is warranted in their application.

I. INTRODUCTION

In recent years, the growing need for energy efficient designs and the emergence of error-tolerant application domains has prompted significant research interest in the area of approximate computing. The basic concept of approximate computing is simple: For many applications such as DSP, data mining and multimedia (audio, video, graphics), a perfect result is usually not necessary. In other words, these classes of applications can tolerate some amount of error. The relaxation of accuracy introduces an amount of design space freedom that can be exploited to reduce power consumption or increase performance. With predictions of increasing adoption of approximate computing systems in the coming years, designers of approximate computing systems should start considering the associated privacy risks and whether they warrant mitigation.

In this work, we consider how approximate computing can compromise privacy of a device or of a device-bearer. We assume that an adversary can apply chosen operands to the processor and observe computed, and possibly identifying erronous results.

Contributions: The specific contributions we make in the paper are as follows:

- We show, for the first time, that results from overscaled approximate computations can reveal the identity of the chip that performed the computation.
- We compare and contrast the identifying ability of the outputs of three popular styles of 32-bit adders.

The remainder of this paper is organized as follows: Section II provides related work on approximate computing to give context to our contribution. Section III explains how approximate computational results can reveal device identity. Section IV addresses methodology. Section V presents simulation results showing how privacy leakage varies with design and clock frequency. Section VI concludes the paper.

II. BACKGROUND AND RELATED WORK

Approximate circuits exploit the potential error resilience of some classes of applications. This error resilience can have different reasons: a) the data is coming from the real world and therefore, is noisy by nature, b) the algorithm used is self-healing and can attenuate an amount of error, or c) the user of these applications is able to tolerate an amount of error in the result [18]. One method of approximate computing is to use deterministic functional approximation, in which a particular Boolean function is replaced by a simpler one that produces similar results at lower complexity [7, 8]. Because functional approximations compute identical results across all chips, they pose no risk to privacy.

The computational circuits that are of interest in this work are circuits that use non-deterministic approximations, or what are sometimes denoted timing-based approximations [19]. In these approaches, a design is voltage overscaled or frequency overscaled to an operating point where timing constraints may be violated by some circuit paths. At overscaled operating points, the output of a circuit depends not only on inputs, but also on process variation.

Many of the efforts toward approximate computing have focused on adders as ubiquitous basic components of digital systems (e.g. [5, 7, 8, 10, 13], among others). More specifically, there has been a lot of research that targets ripple carry adders (RCAs) as an approximate adder of choice because RCAs have a few long paths in the carry chain that are rarely sensitized [10], and this enables a gradual degradation of quality of results when overscaled. For example, the authors in [13] have targeted RCAs to reduce the error rate within a fixed energy budget and the authors in [5] proposed a biased voltage scaling for probabilistic RCAs that scales the operating voltage according to the significance of bits. Because of the focus on adders in previous approximate computing research, we focus our study on adders as well.

Aside from computational blocks in general and adders specifically, there has also been significant interest in approximate memories. Previous works have proposed DRAM-based approximate memories [14] with unsafe refresh intervals to save energy, fast but inaccurate writes to multi-level non-volatile storage cells [16], and voltage overscaled SRAM [3]. Recently, one paper has showed that data stored in approximate DRAM can be used as a fingerprint to reveal device identity [15]. To the best of our knowledge, this one previous paper is the only work to explore privacy issues in approximate computing systems, and no previous works at all have studied privacy leakages on the computational (i.e. non-memory) side of approximate computing.

The use of process variations to identify devices is similar to the idea of a physical unclonable function (PUF) in security. PUFs are circuits designed to extract identifying fingerprints from process variations via timing variations [4] or power-up states of SRAM [6, 11].

III. IDENTIFICATION FROM OVERSCALING

Overscaling-based approximate computing relaxes clock period constraints and allows that the long combinational paths of a circuit may not fully propagate within the clock period. In this case, the register at the end of the path may capture intermediate (wrong) results on the clock edge. Because of process variation, the critical paths of different chips will have different delays. For example, recent works report 12% frequency variation at 1.1V in 45nm technology [17] and 30% for sub-90nm technologies [2]. The variable path delays will cause different erroneous outputs in approximate computation.

Example: We now give a concrete example to show how gate delays can lead to different results at overscaled operating points. Fig. 1 shows an example 8-bit ripple carry adder that has two 8-bit input signals $\{a_7 \dots a_0\}$ and $\{b_7 \dots b_0\}$, and a 9-bit output signal $\{c_{out}s_7 \dots s_0\}$. If $\{a_7 \dots a_0\} = 8'b1111111$ and $\{b_7 \dots b_0\} = 8'b00000001$, a carry signal has to propagate all the way from FA0 to FA7 in order to generate the correct result. We now focus on what occurs after the carry has propagated through the first seven full adders and signal c_7 rises on the input to FA7. Letting the delay of gate *i* in FA7 (see Fig. 1) be denoted d_i , when the value of c_7 rises, the output s_7 will fall after time d_2 . The critical path to c_{out} goes through gates 3 and 5. Therefore, it takes $d_3 + d_5$ from the time c_7 changes for c_{out} to rise.

The value captured on c_{out} and s_7 will depend on the delays of the gate instances. In the presence of process variation, some gates might be faster or slower on one chip than another. If all gates are slow relative to the clock period, then the rising transition on c_7 may propagate to neither c_{out} nor s_7 before the clock edge, and the output will be $c_{out}s_7 = 01$. If gates 2,3, and 5 are all fast, then the correct value of $c_{out}s_7 = 10$ will be captured on the clock edge; this is depicted in Fig. 2a. If gate 2 is slow, and gates 3 and 5 are fast, then output s_7 will not have fallen before the capturing clock edge, and the captured value will be $c_{out}s_7 = 11$ (Fig. 2b). If gate 2 is fast and gate 3 or 5 is slow, then output s_7 will have fallen but c_{out} will not have risen, and the captured output value will be $c_{out}s_7 = 00$ (Fig. 2c). This example shows that variations in gate delays can lead to different erroneous outputs in approximate computing; this is the reason that overscaled approximate computing may lead to device identifiability.

Entropy of Input Vectors: Note that for the above example, we only considered a portion of a small circuit. For a large circuit, each individual gate has different delays and many different output results can be generated for some inputs. A good input vector for identification is able to distinguish different chips with different path delays caused by process variation. When applying random input vectors to a circuit the majority of vectors will not sensitize long paths and therefore will produce deterministic error-free outputs. To distinguish



Fig. 1: An 8-bit ripple carry adder with full-adder blocks.



Fig. 2: Timing diagram for FA7 of the ripple carry adder depicted in Fig. 1

the useful vectors from non-useful vectors, we use metric of conditional entropy. When an input vector a_j is applied across a large number of devices at a particular operating point, let the probability of observing output x_i be denoted $Pr(x_i|a_j)$. The entropy associated with the result to input a_j is given by equation 1. The input vectors with high entropy may be specific to the style of adder and operating point. Although entropy can be estimated from the outputs of adders when viewed as a black box, the entropy associated with different inputs to each adder type implicitly depends on the distribution of path lengths and the path diversity inside of the adder.

$$H(X|a_j) = -\sum_i Pr(x_i|a_j) \log_2 Pr(x_i|a_j)$$
(1)

If an input vector has high entropy on a particular style of adder, it will induce different results for many of the considered chips. However in practice, an input vector usually produces the same results for many chips. Furthermore, noise can diminish the usefulness of high-entropy inputs. Nonetheless, entropy is a useful metric that can provide insights about the identifying ability of each adder, as will be discussed in Sec. V-A.

IV. METHODOLOGY

We considere three different 32-bit adders for our evaluations: ripple carry adder (RCA), carry lookahead adder (CLA) and Han-Carlson adder (HCA) [9]. Because our experiments require simulating a large number of vectors on large populations of 32-bit adder circuit instances, using HSPICE simulation alone was found to be impractical in terms of simulation time. Instead, we use HSPICE simulation to extract gate delays and then use timed Verilog simulation with the extracted gate delays to simulate the overall 32-bit circuit. The gate models in HSPICE are 45nm CMOS Predictive Technology Model [1] (PTM) minimum-sized transistors at voltage of 1.0V. Monte-Carlo simulation is performed 100 times across process variations on V_{th} to provide a realistic distribution of pin-to-pin gate delays for each gate type. When creating an instance of the overall adder circuit, we randomly select gate delay instances from the pre-characterized distributions of each gate type. The timed Verilog models of the adders are simulated using Icarus Verilog (iVerilog).

Changing voltage and changing clock period are two different ways of affecting the same amount of overscaling. In our experiments, we control overscaling by changing the clock period while keeping a set of gate delays extracted at one voltage. We choose this approach because it allows us to dial in a target error rate by performing a binary search on the clock period until hitting the desired error rate. We make comparisons across the different styles of 32-bit adders by choosing a clock period for each adder style that realizes equivalent rates of erroneous output. For our 32-bit adders, the clock periods that yield 1%, 2% and 5% erroneous outputs are shown in Tab. I. Note that going from 5% error to 1% error in an RCA requires increasing the clock period by 127 ps, whereas both CLA and HCA require only a 20 ps increase for the same change in error. This occurs because the RCA has many infrequently sensitized long carry chain paths, whereas HCA is a tree adder with many near-critical paths.

To represent non-idealities in our timing model and to evaluate the robustness of identification, we introduce random noise to our simulations. Each time noise is added to a gate, it is drawn from a normal distribution with 0 mean and standard deviation equal to 10% of the nominal delay. Noise is uncorrelated across gates, and across vectors, meaning that for each new vector applied to a circuit, the noise offsets are replaced by new values.

TABLE I: Clock period used for each adder type to achieve desired error rate.

	RCA	CLA	HCA
1% error	653 ps	345 ps	355 ps
2% error	624 ps	340 ps	349 ps
5% error	526 ps	325 ps	335 ps

V. EVALUATION

We perform a set of experiments to study the extent to which instances of each adder type can be identified by their outputs. We use these experiments to compare the identifiability of the different adder styles, and the impact of noise.

A. Measuring the Entropy of Vectors

The first step toward practical chip identification is to pick high entropy vectors. We set the clock period for each adder style to achieve a 1% error rate and simulate 200,000 random input vectors on 50 instances of RCAs, CLAs and HCAs. We calculate the entropy of each applied vector according to Eq. 1. The average entropy for RCA, CLA and HCA are 0.01227, 0.01187 and 0.03260, respectively. In the RCA, 97.78% of all input vectors induce the same result on all 50 chips, while in the HCA, the same number is only 90.73%. This is because in an RCA, a much higher percentage of vectors cause errors on no chips, or in other words sensitize no paths with delay comparable to or exceeding the clock period. On the other hand, an HCA, which is a tree adder, tends to have a variety of paths with similar nominal delays, and a much lower percentage of vectors are error-free across all chips at the chosen clock period. Another view of this result is as follows: when considering for each adder type the set of random vectors that caused an error on one or more of the 50 instances, we find that each such vector causes errors in about 71% of RCA chips, versus only 24% for CLA and 10% for HCA adders. If each adder type is operated at the same error rate, the error-causing input vectors will be less unique on the RCA. Note however, that non-unique input vectors does not mean that the output vectors are less unique to each chip; instead, it only means that the inputs that *induce* the erroneous outputs are less unique to each chip.

B. Identification Results

Next we explore identification of chip instances using their outputs. For this experiment, we simulate 40,000 vectors on 50 instances of each adder type operating at their respective clock periods for 1% error (Tab. I). To measure similarity or lack of similarity between the outputs produced, we use a metric of Matching Distance. The matching distance for any two adders of the same type is the number of outputs that differ when the same (40,000) input vectors are applied. The histograms of between-class and within-class matching distances are shown in Fig. 3. The within-class bars correspond to the matching distance of two trials of the same chip in the presence of noise (see Sec. IV), and the between-class bars correspond to pairings of two different chips. When between-class and within-class overlap less, then one can better tell whether two sets of outputs are from the same chip, and can therefore better identify a chip. A chip can always be identified using some matching distance as a decision threshold if the between-class and within-class distances are non-overlapping.

ROC Curve: A Receiver Operating Characteristic (ROC) curve is used to measure the performance of chip identification. Each point of an ROC curve corresponds to a single decision threshold and depicts the trade-off between true positives and false positives at that decision threshold. In an ideal case where between-class and within-class distances are separable, the ROC curve will be a step function [12], as this would indicate that there exists some decision threshold that can correctly identify all true positives (within-class pairings) without accepting any false positives (between-class pairings). Fig. 4 shows the ROC curve for the three adder styles; the RCA is easily the most identifiable of the three adder styles in this case.

C. Impact of Error Rate

There is usually a trade-off between the amount of errors in the outputs and the power/performance improvement in the system. While accepting a higher error rate can be more attractive for efficiency, our results show that a higher error rate can increase identifiability of a circuit. In this experiment we set the clock period such that an average error rate of 1%, 2% and 5% are seen on the output results. The results of this experiment are shown in Fig. 5.

VI. CONCLUSION

This paper has considered, for the first time, the possible privacy implications of voltage-overscaled or frequency-overscaled approximate computations. We perform a large simulation study on three types of adders and show that the ability to provide inputs to a computation unit and observe corresponding outputs



(c) Matching distance of Han-Carlson adder

Fig. 3: Matching distance based on outputs produced for 40,000 random input vectors for each adder type.



Fig. 4: ROC curve of three adders when 40,000 vectors are simulated on 50 instances of each adder using a clock period for 1% error rate. The AUCs for RCA, CLA, and HCA are 0.99, 0.89 and 0.81 respectively.



Fig. 5: ROC curve of each adder type at different error rates

can reveal the identity of the approximate computing device that performed the computation. This is a possible privacy risk that designers of future approximate computing systems should consider when evaluating application scenarios.

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