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A Switched Capacitor DC-DC Buck Converter for a Wide Input Voltage Range

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Abstract*—In this paper, a power-efficient multiphase Recursive Switched Capacitor (RSC) converter is presented. Conventionally, RSC converters are used to obtain many different output voltages from a fixed input voltage. Here, the converter provides a fixed output voltage of $1\,\mathrm{V}$ at $1\,\mathrm{mA}$ from an input voltage ranging from $1.4\,\mathrm{V}$ to $4.5\,\mathrm{V}$. It has one programmable stage ($2:1$ or $3:2$) followed by four $2:1$ stages. Contrary to most conventional topologies, depending on the input voltage, not all the stages are always deployed. This allows to increase the power efficiency of the whole architecture. The flying capacitance of the non-activated stages is transferred to the activated ones. Hence, for any given input voltage, 100% of the on-chip capacitance is always used for the conversion. For a general $2:1$ topology, an analytical analysis of the power losses is carried out and the impact of the overdrive voltage of the switches on the power efficiency is quantified. A novel gate-driver technique for the switches involved in the conversion is proposed. It ensures an optimal overdrive voltage of the transistor, irrespective of its source and drain potentials. The 16-phase interleaved converter employs a charge recycling technique and uses a total on-chip capacitance of $3\,\mathrm{nF}$. The RSC converter is designed to be implemented in a standard $40\,\mathrm{nm}$ CMOS process which offers a capacitor density of approximately $2\,\mathrm{nF/mm^2}$. Circuit simulations over the whole input voltage range show a power efficiency never lower than 54% with a peak value of 92.7%.

Keywords—DC-DC converter, switched-capacitor, voltage regulator, wide input voltage range.

I. Introduction

Voltage regulators have become widely used in today's electronic systems. They are required to power up electronics working in different voltage domains, each of them with different power requirements and different specifications, e.g. amplitude and frequency of the ripple. Among voltage regulators, switched Capacitor (SC) DC-DC converters are becoming more and more popular. They take advantage of higher switching frequencies (up to GHz) and higher capacitor densities of nanometer IC technologies to obtain efficient conversion without using external components. In Fig. 1, the block diagram of a typical energy harvester and power management system is shown. The energy harvester receives the energy from an external source and converts it into electrical energy. The power delivered by the energy harvester strongly depends on the type of energy source and its environment and may be fluctuating. It is therefore necessary to continuously store the available energy. Nowadays, as storage elements, supercapacitors are preferred over batteries for their longer lifetime (measured by the numbers of charging and discharging cycles they can handle). Supercapacitors are also considered to be more environmentally friendly. However, as the capacitor gradually discharges during T_{on}, its voltage reduces, as shown in Fig. 1. Hence, the voltage regulator has to cope with a wide input voltage range.

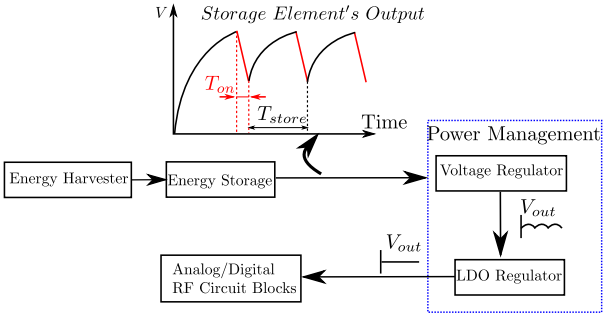

Fig. 1. Block diagram of a typical power management system.

With the migration towards more advanced IC technologies, the maximum overdrive voltage that a transistor can handle is becoming smaller and smaller. This poses a serious challenge in the design of switched capacitor circuits. In order to reduce the on-resistance of a switch, the designer can modify the aspect ratio of the transistor (i.e. the W/L ratio) or the overdrive voltage defined as $|V_{GS} - V_{th}|$. The aspect ratio of the switches can be increased at the expense of the parasitic capacitance that is charged and discharged during every switching period. In a standard $40\ nm$ CMOS process, the maximum rating voltage that a low-power transistor can handle is $1.1\,\mathrm{V}$, which is well below the maximum input voltage. While the exposure of the transistor to a high drain-to-source voltage can be overcome by cascading more devices, the maximum gate-to-source voltage requires a proper gate-driver circuit. If the overdrive voltage is too low, it seriously affects the power efficiency, while an excessively high gate-to-source voltage causes gate-oxide breakdown of the transistor. In this paper, rather than implementing gate-driver circuits that consume silicon area and power, a novel switch is presented.

This paper is organized as follows. In Section II, an analysis of the 2:1 SC converter is carried out. Following the state space model introduced in [1], the power efficiency is derived for a given stage of the RSC converter. In Section III, the topology of the implemented RSC converter is described. A novel switch that tackles the problems highlighted in Section II is presented. Results from circuit simulations are shown, along with a discussion and comparison with state of the art converters. Finally, in Section IV, conclusions are drawn.

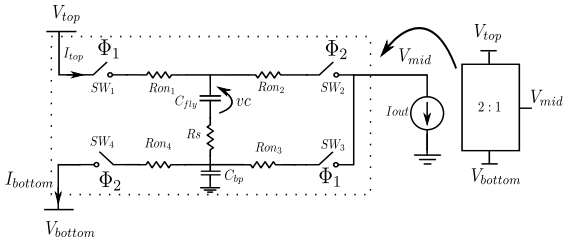

Fig. 2. Circuit representation of a 2 : 1 SC converter

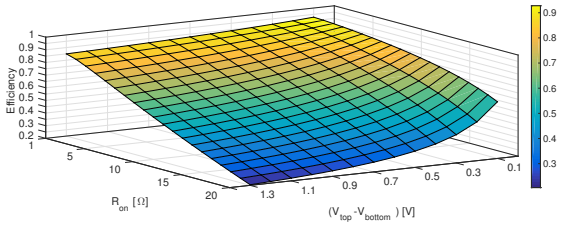

Fig. 3. Power efficiency for different on-resistances with $C_{bp} = 5\%C_{fly}$. $V_{top} = 2.2\,\mathrm{V}$, while V_{bottom} has been swapped from $2.1\,\mathrm{V}$ to $0.9\,\mathrm{V}$.

II. Converter analysis and power losses of a 2:1 SC topology

In this section, the state space model approach of a 2 : 1 SC converter, introduced in [1] is generalized. Taking into account the on-resistance of the switches and the parasitic capacitances, the expression of the power efficiency is derived for a generic 2 : 1 SC converter. MATLAB simulations are used to compute the derived equation for the power efficiency and point out the importance of a low on-resistance for all the switches involved in the conversion chain.

In Fig. 2, the equivalent circuit of a 2 : 1 SC converter is shown. It has a charge-transfer capacitor C_{fly} with its series resistance R_S and parasitic capacitance C_{bp}. A MOM (Metal-Oxide-Metal) capacitor is used, therefore its parasitic capacitance is mainly due to the coupling between the bottom plate and the substrate. Two non-overlapped clock phases Φ_1 and Φ_2 drive the four switches $SW_1 - SW_4$ having on-resistances $Ron_1 - Ron_4$, respectively. The output voltage V_{mid} is the average value of the two input voltages, V_{top} and V_{bottom}.

In [1], the power efficiency η is derived in terms of I_{out}, I_{top} and V_{top} and the authors assume that V_{bottom} always equals zero, hence $V_{mid} = V_{top}/2$. This assumption does not hold for RSC converters in which V_{bottom} is not always zero. During phase Φ_1 (Φ_2) , C_{fly} is charged (discharged) towards $V_{top} - V_{mid}$ ($V_{mid} - V_{bottom}$) through an RC circuit having a time constant of $(2Ron + Rs)C_{fly}$. For the converter shown in Fig. 2, the power efficiency can be expressed as

$$\eta = \frac{V_{mid} I_{out}}{V_{top} I_{top} + V_{bottom} I_{bottom}} \tag{1}$$

In steady state, the total charge transferred to the output per each switching period is [1]

$$Q_{tran} = 2C_{fly}\Delta vc = 2C_{fly}(V_{Cmax} - V_{Cmin}) \tag{2}$$

where V_{Cmax} and V_{Cmin} are the voltages across the capacitor at the end and at the beginning of the charging phase, respectively. They can be expressed as follows:

$$V_{Cmax} = \frac{V_{top} - V_{mid} + AV_{mid} - AV_{bottom}}{A + 1} \tag{3}$$

$$V_{Cmin} = \frac{V_{mid} - V_{bottom} + AV_{top} - AV_{mid}}{A + 1} \tag{4}$$

where $A = -1/e^{2fsw(2Ron+Rs)C_{fly}}$ and fsw is the switching frequency of the converter. It is worth mentioning that if $I_{out} = 0$ the net charge transferred to the load is zero and $V_{Cmax} = V_{Cmin} = (V_{top} + V_{bottom})/2$. Applying the state space model approach used in [1], I_{top}, I_{bottom} and I_{out} can be rewritten in terms of the charge transferred by each capacitor during the charging and discharging phase. The average currents over a switching period become:

$$I_{top} = q_C f_{SW} \tag{5}$$

$$I_{bottom} = (q_C - q_{Cbp}) f_{SW} \tag{6}$$

$$I_{out} = (2q_C - q_{Cbp}) f_{SW} \tag{7}$$

where q_C and q_{Cbp} are the total charges transferred by the flying capacitor and its parasitic capacitance, respectively.

Eq. (1) can now be rewritten in terms of q_C and q_{Cbp}, leading to

$$\eta = \frac{V_{mid}(2q_C - q_{Cbp})}{V_{top} q_C + V_{bottom}(q_C - q_{Cbp})} \tag{8}$$

The above equation is computed in MATLAB and the results are shown in Fig. 3. For all the simulations we used: $f_{SW} = 20\,\mathrm{MHz}$, $C_{fly} = 1\,\mathrm{nF}$. To control R_{on} the overdrive voltage has been varied from the maximum value allowed by the technology down to $V_{GS} = 0.6\,\mathrm{V}$, which provides $R_{on} = 20\,\Omega$. An aspect ratio of 250 for all the transistors has been assumed. In phase Φ_1, parasitic capacitance C_{bp} is charged to V_{mid} and then in phase Φ_2 it is discharged to V_{bottom}. Therefore, the closer V_{top} is to V_{bottom}, the lower is the impact of the parasitic capacitance on the power efficiency. From Fig. 3, we can see that the power efficiency decreases when the overdrive voltage reduces, i.e. the on-resistance increases. The voltages experienced by the many switches involved in the conversion can vary greatly, depending on the input voltage. It is therefore important to ensure a proper overdrive voltage for all the switches. Appropriate overdrive voltages require proper circuit techniques usually based on bootstrapping, which consume area, power and sometimes even require an external power supply [2].

III. Circuit design and simulation results

In this section, the circuit implementation of the RSC converter is discussed along with a novel implementation of the switches. Simulation results are discussed and compared with the performance of other converters that aim to achieve high power conversion efficiency for a wide input voltage range.

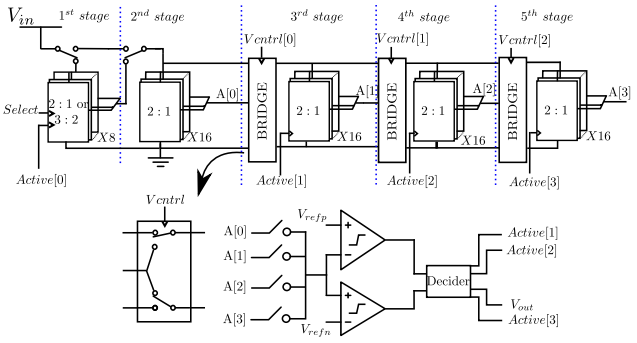

Fig. 4. Diagram of the RSC converter implemented and control.

A. System description

In Fig. 4, the block diagram of the converter along with the digital control is shown. The voltage conversion is performed in several stages until the desired voltage of $1\,\mathrm{V} \pm 5\%$ is reached. The voltage V_{in} comes from the storage element, and can be as high as $4.5\,\mathrm{V}$. Each stage consists of the $2:1$ converter shown in Fig. 2 except for the 1^{st} $stage$ which, based on the value of V_{in}, can perform a $3:2$, a $2:1$ conversion, or is being switched off. Its configuration is set by the $Select$ signal. The 1^{st} $stage$ is made of high voltage devices and is used to bring the voltage low enough so that the next stages can be made of more efficient low-power devices. For the $1st$ $stage$, depending on the value of V_{in}, one of the following scenarios occurs

- $3.2\,\mathrm{V} < V_{in} < 4.5\,\mathrm{V}$. The $2:1$ conversion is performed and the output of the first stage becomes the top voltage of the second stage;
- $2.2\,\mathrm{V} < V_{in} \leq 3.2\,\mathrm{V}$. The $3:2$ conversion is performed and the output of the first stage becomes the top voltage of the second stage;
- $V_{in} \leq 2.2\,\mathrm{V}$. V_{in} is directly connected to the top voltage of the second stage. The first stage is not involved in the conversion, while its flying capacitance is being used by the stages that follow.

The 2^{nd} $stage$ is always active and its top voltage ranges from $1.4\,\mathrm{V}$ to $2.2\,\mathrm{V}$. The block $BRIDGE$ is made of four switches and it connects two adjacent stages. The top voltage of each stage is connected either to the output or top voltage of the previous stage. The bottom voltage of each stage is connected either to the bottom or the output voltage of the previous stage. Signal V_{cntrl} is used to control the switches of the $BRIDGE$. Depending on the value of V_{in} not all the stages might be needed [4]. For instance, if the output voltage of any given stage already equals the desired voltage, all the subsequent stages are switched off by making the $Active$ signal low. In order to choose how many stages are needed for the conversion, a window-comparator is used. The comparator checks whether the output voltage of each $2:1$ stage is in the desired range. The *Decider*, based on the comparator's result, connects one of the output nodes of the $2:1$ stages, $A[0], ..., A[3]$, to the output node.

The total on-chip capacitance is $3\,\mathrm{nF}$ and occupies most of the silicon area. Therefore, in order to achieve the maximum power efficiency for the given silicon area, the charge transfer capacitor of the non-activated stages is transferred to the active ones, allowing a 100% use of the total capacitance. For this purpose, each stage has two additional switches, not shown in Fig. 4, which connect the top (bottom) plate of the capacitor of any given stage with the top (bottom) plate of the previous stage. These switches are kept off when the stage is used, while they are turned on, when the stage is not used, allowing to transfer that capacitor to the previous stage.

Each $2:1$ stage is divided into several smaller units. Each unit operates out of phase with respect to each other. In [3], it is shown how such a time-interleaving technique helps reducing the ripple of the output voltage. From circuit simulations of a $2:1$ stage, 16-interleaving units are found to be the best trade-off between control-circuit overhead and benefit coming from the interleaving. The 1^{st} $stage$ can perform a $3:2$ or $2:1$ conversion. Therefore it has additional switches, which makes its control more complicated. This is the reason why, for this stage, 8 units seem to provide a higher efficiency. Since the last stage is the only one to determine the frequency of the output ripple, all the internal stages involved in the conversion can operate at higher appropriate switching frequencies. In our design, each unit of the last stage operates with a switching frequency of $20\,\mathrm{MHz}/16 = 1.25\,\mathrm{MHz}$.

As discussed in Section II, the charge lost due to the parasitic capacitance affects the power efficiency, especially when V_{top} and V_{bottom} are far from each other. In this work, the charge recycling technique introduced in [1] has been implemented. The parasitic capacitance of each unit is charged and discharged at every switching event. At the end of the charging phase, C_{par} is charged to V_{mid}. The idea is to short two bottom-plate nodes of two units that are in antiphase with respect to each other. Therefore the charge is redistributed between the two parasitic capacitances and the supply V_{top} will have to deliver only half of the energy needed to charge the parasitic capacitance again.

B. Switch design

The voltages at the terminals of some of the switches of the RSC converter can vary by a large amount depending on the input voltage. Hence proper gate driving circuits are to be used. In [4], this problem is not experienced because the input voltage is fixed and equals the rating voltage of the devices, therefore the optimal overdrive voltage can always be ensured. In [2], an input voltage higher than the rating voltage is used. The authors propose a gate driver circuit that uses an adaptive bootstrapping technique to ensure an appropriate overdrive voltage to all the switches. The gate driver, however, uses an external supply. In [5], the necessary voltages are obtained by using capacitor-based boosting circuits and thick-gate transistors. However, a 5-stage 16-phase RSC converter has too many switches that need to be properly driven. Therefore, in this design, boosting circuits would lead to chip-area overhead and additional power consumption. All these solutions will however be compared in the next subsection.

In Fig. 5 (a), the schematic of the proposed switch is shown along with its $I-V$ characteristic, Fig. 5 (b). In point A the switch is off, while in point B the switch is on. When a current flows through transistor M_3, and hence

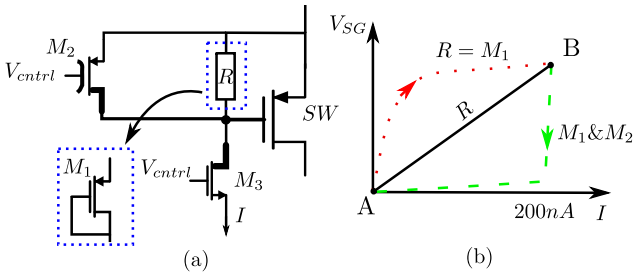

Fig. 5. (a) Schematic of the P-MOS switch implemented (b) with its equivalent resistance diagram in case a linear resistor, R (solid black line), or a diode-connected transistor, M_1 (dotted red line) is used. M_1 used in combination with M_2 allows for a fast turn-off of the main switch (green dashed line).

through resistance R, a voltage drop is generated between the source and the gate of switch SW. The overdrive voltage of SW only depends on the value of R and the current flowing through it. Hence, with a resistance of $5\,\mathrm{M\Omega}$ and a current of $200\,\mathrm{nA}$, a voltage drop of $1\,\mathrm{V}$ between the source and the gate of SW can be ensured irrespective of its source and drain potential. A diode-connected transistor is preferred over a resistor for its lower silicon area. When SW needs to be turned off, the time constant associated with the discharging process of the gate-to-source capacitance will be too high. For this purpose transistor M_2 is used. It is turned on when Switch SW needs to be turned off. Hence, the source and the gate of SW are shorted together and the gate-to-source capacitance is discharged with a substantially smaller time constant. Although transistor M_2 is a high voltage device, it does not affect the power efficiency because it is only used to discharge the gate-to-source capacitance of the main switch. Graphically, the switch is turned on moving from A to B along the red dotted line, and it is turned off moving from B to A on the green dashed line. By doing so, every time the switch changes state, either the current or the voltage is zero, additionally allowing to reduce the power wasted during the switching event.

Transistors M_1 and SW are both PMOS devices. In, e.g., the slow PMOS corner, the threshold voltages of both Switch SW and Transistor M_1 increase. As a result the overdrive voltage of the switch becomes larger, which compensates for its larger threshold voltage. Hence, the on-resistance of the switch stays pretty constant with respect to process variations. Circuit simulations of the four corner cases (SS, SF, FS, and FF) showed that the resistance of transistor M_1 can vary as much as 10% with respect to its nominal value, leading to a source-to-gate voltage of $1.1\,\mathrm{V}$, which does not exceed the maximum rating voltage of the switch.

C. Simulation results and comparison with the state of the art

The simulated power efficiency of the converter over the whole input voltage range is presented and compared with the state of the art in Fig. 6. In the proposed design, all the stages are connected in cascade, hence the overall power efficiency of the converter is proportional to the product of the power efficiency of each single stage involved in the conversion. The peak value of power efficiency of 92.7% is achieved when one stage is used. It is well above the value achieved by the state of the art, mainly due to the new switch topology and the recycling of the charge of the parasitic bottom plate

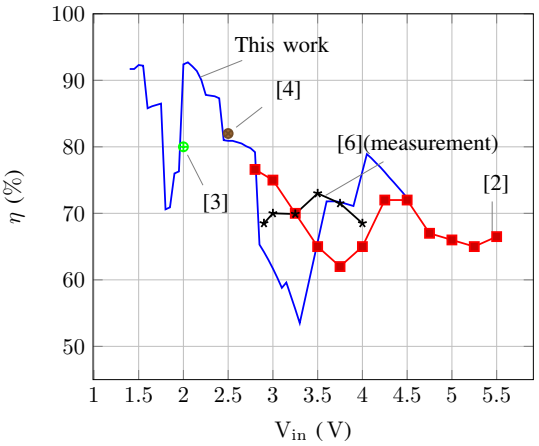

Fig. 6. Efficiency results of the RSC converter for various input voltages and $V_{out} = 1\,\mathrm{V}$. For [3] and [4] only the peak value has been considered.

capacitance. In [2], the input voltage ranges from $2.8\,\mathrm{V}$ to $8\,\mathrm{V}$ with a peak efficiency of 76.6%. It implements a bootstrapping technique which generates a floating rail to drive the gate of the switches. This solution requires an external voltage of $2V_{out}$, which depends on the output voltage, hence needs to be tuned every time the desired output voltage changes. In [3] and [4], the input voltage is fixed and thus does not pose serious challenges on the gate-driving circuits. In [6], additional circuitry made of thin-gate transistors is used to generate a voltage of $2V_{out}$. This limits the input voltage range to $2.8\,\mathrm{V}$ - $4\,\mathrm{V}$. The average power efficiency of the state of the art is limited by the great voltage variations experienced by some of the switches. In the proposed architecture, this problem is overcome with the design of a novel switch, and an average higher power efficiency over a wide, input voltage range is achieved.

IV. Conclusions

In this paper a 5-stage RSC converter has been presented. The output voltage is kept constant at $1\,\mathrm{V} \pm 5\%$ by reconfiguring the stages of the converter. It efficiently converts an input voltage from $1.4\,\mathrm{V}$ to $4.5\,\mathrm{V}$ into a fixed output voltage of $1\,\mathrm{V}$ with an efficiency between 54% and 92.7%. The effect of the overdrive voltage of the switches on the on-resistance has been quantified and a novel switch that always work with an optimal overdrive voltage has been implemented. The converter uses an interleaving technique and is capable of recycling the charge lost due to the parasitic bottom plate capacitance. Results from circuit simulations prove the correct operation while achieving a maximum efficiency of 92.7%.

Acknowledgements

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