

Design of a 4th-Order Feed-Forward-Compensated Operational Amplifier for Multi-GHz Sampling Frequency Continuous-Time Bandpass Sigma-Delta Modulators

Fikre Tsigabu Gebreyohannes, Marie-Minerve Louërat, Hassan Aboushady

▶ **To cite this version:**

Fikre Tsigabu Gebreyohannes, Marie-Minerve Louërat, Hassan Aboushady. Design of a 4th-Order Feed-Forward-Compensated Operational Amplifier for Multi-GHz Sampling Frequency Continuous-Time Bandpass Sigma-Delta Modulators. 2019 IEEE International Symposium on Circuits and Systems (ISCAS), May 2019, Sapporo, Japan. 10.1109/ISCAS.2019.8702147 . hal-02145589

HAL Id: hal-02145589

https://hal.sorbonne-universite.fr/hal-02145589

Submitted on 3 Jun 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Design of a 4th-Order Feed-Forward-Compensated Operational Amplifier for Multi-GHz Sampling Frequency Continuous-Time Bandpass Sigma-Delta Modulators

Fikre Tsigabu Gebreyohannes, Marie-Minerve Louerat, and Hassan Aboushady, *Member, IEEE,*
Sorbonne Université, CNRS, Laboratoire d'Informatique de Paris 6, LIP6, F-75005 Paris, France
e-mail: (fikre-tsigabu.gebreyohannes, marie-minerve.louerat, hassan.aboushady@lip6.fr)

***Abstract*—This work presents a 4th-order multi-stage, multi-path, feed-forward-compensated operational amplifier in 65 nm CMOS technology. It is designed to meet the requirements of a continuous-time bandpass ΣΔ modulator with multi-GHz sampling frequency. The designed amplifier is modular with each stage implemented based on a unit differential amplifier block and it meets its targets with smart placement of poles and zeros. The amplifier is simulated under the loading condition of a single-amplifier resonator which is in turn part of a 6th-order ΣΔ modulator. The unloaded amplifier reaches a unity-gain-frequency of 38.29 GHz and a DC gain of 58 dB. With a parallel load of 440 fF and 300 Ω, representing the maximum load, the op-amp, including common-mode and biasing circuits, consumes a total of 18.98 mA from a supply voltage of 1.2 V. It is unconditionally stable with a phase margin of 54° and has gains of 35 dB and 23 dB at 1 GHz and 2 GHz respectively.**

***Index Terms*—multi-stage amplifiers, Feed-forward compensation, sigma-delta modulators, bandpass, continuous-time**

I. Introduction

HIGH-speed bandpass ΣΔ modulators are employed in receiver front-ends for direct conversion of RF signals to digital. For narrow band standards, high purity reception is possible with large sampling frequency to bandwidth ratio. Nevertheless, multi-standard reception requires broadband operation and this limits the value of the oversampling factor. While configurations with multi-bit digital output can realize aggressive noise transfer functions, high resolution conversion with a 1-bit digital output must rely on increasing the order of the modulator. For the target application of this work, a feedback-form 6th-order continuous-time (CT) bandpass ΣΔ modulator was selected.

In a 1-bit implementation, the analog blocks account for the biggest share of the total power consumption and it is more pronounced for the chosen topology as resonators in the feedback-form ΣΔ architecture are designed for stringent requirements [1]. Compared to traditional active-RC resonator implementations, this work favors single-amplifier resonators to half the number of op-amps. A single-amplifier resonator topology is shown in Figure 1 [2]. Compared to other reported single-amplifier resonators, it features a small capacitor and resistor spread which helps in tuning and mismatch reduction [3]. With the values shown in Figure 1, the output network cancels a left-hand zero, but can also be modified to reduce kickback from next stage resonator [4]. The transfer function in (1) is obtained from current output to current input ratio. The quality factor and resonance frequency can be derived

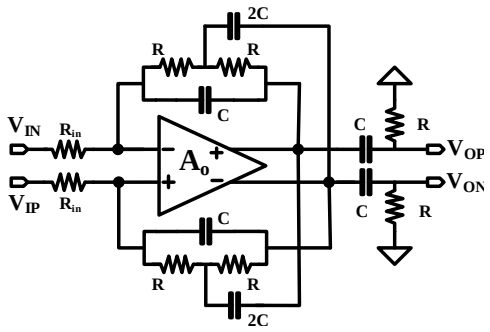


Figure 1: A single-amplifier resonator with small passive component spread

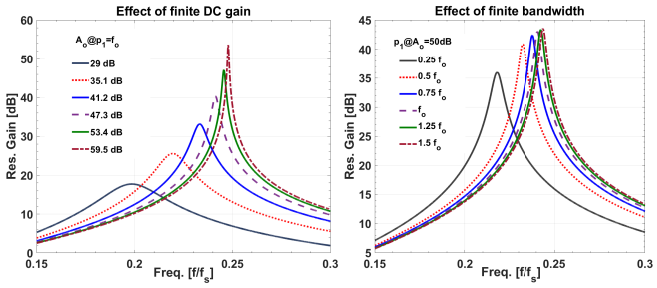


Figure 2: Effects of finite amplifier DC gain (A_o) and bandwidth (p_1) on quality factor and resonance frequency

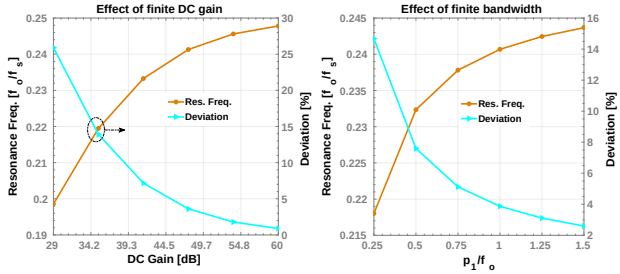


Figure 3: Percentage deviation of the resonance frequency due to effects of finite amplifier DC gain and bandwidth

$$H_{RES}(s) = \frac{s(2RCA_o p_1)}{s^3(2(RC)^2) + s^2(2p_1(RC)^2(A_o+1) + 4RC) + s(4RCp_1 + 1) + p_1(A_o+1)} \tag{2}$$

$$\left(\frac{Vout}{Vin}\right)_{FF} = \frac{A_{o1}A_{o2}A_{o3}A_{o4} + A_{of1}A_{o3}A_{o4}(1+\frac{s}{p_1}) + A_{of2}A_{o4}(1+\frac{s}{p_1})(1+\frac{s}{p_2}) + A_{of3}(1+\frac{s}{p_1})(1+\frac{s}{p_2})(1+\frac{s}{p_3})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})(1+\frac{s}{p_3})(1+\frac{s}{p_4})} \tag{3}$$

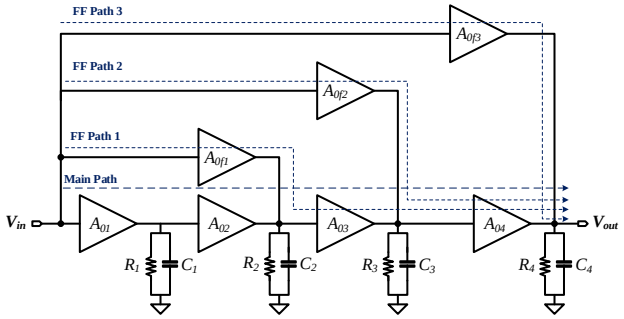


Figure 4: System-level diagram of the 4th-order FF-compensated op-amp

using the standard form second-order bandpass filter equation from (1) i.e. $\omega = 1/2\sqrt{RC}$, and $Q = (A(s)+1)/2\sqrt{2}$.

$$H_{RES}(s) = \frac{s\frac{A(s)}{RC(A(s)+1)}}{s^2 + s\frac{2}{RC(A(s)+1)} + \frac{1}{2(RC)^2}} \tag{1}$$

where A(s) is the amplifier transfer function and R & C are the component values in Figure 1.

As the quality factor of the resonator dictates the shape of the noise transfer function of the modulator, the amplifier specifications can be derived from it. A simplified approach is to assume the op-amp has a constant gain. In that case, gain of op-amp is: $2\sqrt{2}Q - 1$. A more practical method is to model the op-amp as a single-pole system with DC gain of A_o and a pole at p_1 as: $A(s) = A_o/(1+s/p_1)$. The resonator transfer function is then given as in (2).

The simulation results in Figure 2 are carried out with a single-pole amplifier transfer function for the resonator in Figure 1. It can be seen that for a pole at the resonance frequency, which is also the center frequency (f_o) of the bandpass ΣΔ modulator, the quality factor rises and the frequency deviation improves as DC gain increases. Similarly, for a high DC gain, for example 50 dB, the resonance frequency deviation is low and reduces as the pole moves beyond f_o. The frequency deviation for each simulation in Figure 2 are extracted and plotted in Figure 3. To derive specifications for the op-amp, the acceptable percentage error has to be selected. A 15% error can be taken as the maximum acceptable error as it is a value comparable to resistor and capacitor variations due to process corners [5]. In that case, from Figure 3, we can see that at $p_1 = f_o$, the deviation is reduced to less than 15% for A_o larger than 34 dB i.e. to target a ΣΔ modulator with sampling frequency (f_s) of 2 or 4 GHz, the DC gain should be at least 34 dB and the gain at p_1 (0.5 or 1 GHz) should be at least 31 dB. Similar estimation can be carried out using the plot for effect of finite bandwidth.

To reach such high gain at the center frequency of the modulator, supply voltage limits the utilization of conventional gain boosting techniques such as cascoding. Thus, high gain is reached by cascading moderate-gain amplifiers. To ensure stability, simple amplifier topologies with few internal nodes ought to be selected. Still for more than two stages, a mechanism of creating zeros is required; and the feed-forward (FF)-compensated amplifier fits the bill. Recent works in FF-compensated amplifier include the work in [1] which demonstrates a gain of 60 dB at 250 MHz with a 5th-order op-amp. However, it achieves it with a supply voltage of 2.5 V in its input and output stages. Reference [4] implements a four-stage two-path amplifier and incorporates Nested Miller-compensation to improve its phase margin (PM). It relies on a 1.25 V supply and achieves a DC gain of 80 dB. Nonetheless, it fails to produce large gain beyond 1 GHz and only reaches a unity-gain-frequency of 3 GHz. The 4th-order FF-compensated op-amp in [6] fulfills performance requirements of a multi-GHz sampling frequency ΣΔ modulator at the cost of large silicon area.

This work introduces a G_m/I_d-based design methodology tailored for multi-stage, multi-path feed-forward compensated op-amps. Smart placement of zeros and poles enables it to achieve a gain of 23 dB at 2 GHz, a PM of 54° and a minimum phase of -150°. Section II discusses the system-level design approaches that can be followed when designing a high order FF-compensated amplifier. Section III details the circuit level choices that have been made to narrow the design space. The main results are plotted and tabulated in Section IV. The paper is concluded in Section V.

II. System-Level Description

A simplified system-level diagram of the designed 4th-order FF-compensated op-amp is shown in Figure 4. The main path consists of a cascade of four amplification stages (with DC gain $A_{oi}, i \in 1,2,3,4$); the FF path has three amplification stages (with DC gain $A_{ofi}, i \in 1,2,3$); and there are four output poles ($p_i, i \in 1,2,3,4$). The last three poles are shared between the main and FF paths. The transfer function can be formulated as in (3) which consists of four poles and three zeros.

At system-level, it is possible to generate a set of gain and pole combination of each amplification stage that can result in a transfer function with a desired total gain and stability. However, it is difficult to translate the pole values to an actual circuit parameters. This is because the resistors and capacitors forming the loads of each of the stages shown in Figure 4 are parasitic components–except an additional capacitive load at the output of the op-amp. To ease design problems, a modular approach can be followed where each of the amplification

stages are scaled from a single block. For example, selecting the DC gains using the following expressions:

$$A_{of1} = kA_{o1}, A_{of2} = kA_{of1} \wedge {}^{A_{of1}}/_{A_{o2}} = {}^{A_{of2}}/_{A_{o3}} = {}^{A_{of3}}/_{A_{o4}} = k \quad (4)$$

would bring the three left-hand zeros to the unity-gain-frequency of the first amplification stage. Other scaling factor choices enable to separate the zeros and position them such that a workable initial design of the 4th-order op-amp can be obtained [6].

With such design procedure, the problems are twofold. Firstly, the exponential growth of the transistor widths, for a scaling factor of k, the third stage is scaled with a factor of k^2 compared to the first stage and the final stage at least k^3. Normally, the first amplification stage is designed for high DC gain and a noise contribution smaller than that of the input resistance. Hence, even in an unloaded setting, the large gate and drain parasitic capacitors of the resulting final stage disturb smooth translation of the system-level calculations to circuit. Secondly, the zeros in (3) are minimized enough when the scaling factor increases. In other words, for the previous assumption to hold, the gains of each amplification block has to be at least an order of magnitude higher. This leaves the amplifier parameters to be chosen from a narrow design space such that other important specifications, for instance, input noise and feedback DAC biasing and distortion, are sacrificed for it.

To maximize the high frequency performance, no lumped passive components are inserted at each stage output; the poles are left to be defined by the parasitic capacitors and resistors in each node. The main problem in designing high-order FF-compensated amplifiers is, then, the difficulty in manipulating the complex equations that define the zeros and poles of the transfer function. In order to overcome this hurdle, the designed amplifier is constructed, modularly, from a simple differential pair shown in Figure 5a. For a given load, the differential pair can be sized—using ${}^{g_m}/_{ID}$ methodology, for example—to deliver any reasonable DC gain and 3-dB frequency. Starting with a set of gain and pole combination generated from (3), four versions of the differential pair can be sized to meet pole and gain at each stage. Obviously, due to the loading effects, the combined amplifier does not behave as expected. Two methods can be followed to remedy this problem: one is to resize the first three amplification stages, essentially using iterative simulation within a narrow range, until the effects of the input parasitic capacitances of the corresponding succeeding stages are diminished; another is to regenerate the gain and pole combinations with loading effects of the respective stages taken into consideration [7].

III. Design of the Amplifier

In order to guide the generation of the gains and poles combinations, circuit-level assumptions are taken and they are discussed in the following paragraphs. Generally, higher small-signal gain is obtained at lower overdrive voltages and longer transistor lengths. Since the main signal path, in Figure 4, is designed for gain, the NMOS input pairs are chosen to carry it. The feed-forward path is designed for speed, it is carried using the PMOS input pairs. The common-mode input level of the differential pair is set in conjunction with the feedback DACs of the ΣΔ modulator. Since the unit differential pair is repeated in all three resonators of the ΣΔ modulator, the common-mode output magnitude is made to be equal to the common-mode levels of the main and feed-forward inputs magnitudes. Effects of mismatch are lowered by using common-centroid or interdigitated layout; thus, ac-signal carrying transistors of the amplifier have same length. An initial value of of $3L_{min}$ is selected to maximize DC gain.

At this stage, with V_{GS}, V_{DS}, V_{SB}, and L known, the DC gain can be fixed, using (5), independent of the current consumption of each stage [7].

$$A_{o_{i/fi}} = \frac{({}^{g_m}/_{i_d})_{N/P}}{({}^{g_{ds}}/_{i_d})_N + ({}^{g_{ds}}/_{i_d})_P} \quad (5)$$

where $({}^{g_m}/_{i_d})_{N/P}$ is the transconductance to current ratio of either the NMOS or PMOS pairs, and $({}^{g_{ds}}/_{i_d})_{N/P}$ is the drain-to-source conductance divided by the current of either the NMOS or PMOS pairs.

Sizing of the unit differential pair for a desired pole can be readily carried out under the assumption that it is a single-pole system where the unity-gain-frequency (f_u) is the product of the dc gain and the pole frequency. The unity-gain-frequency ($f_u \sim {}^{g_m}/_{C_i}$) and the pole frequency, p_i, is given as in (6) where C_i is the sum of the total parasitic capacitances at the output node ($C_{ddn} + C_{ddp} + C_{ggn}$ of the next stage).

$$p_i = \frac{(g_{ds})_N + (g_{ds})_P}{C_i} \quad (6)$$

$$g_m = 2p_i f_u C_i \quad (7)$$

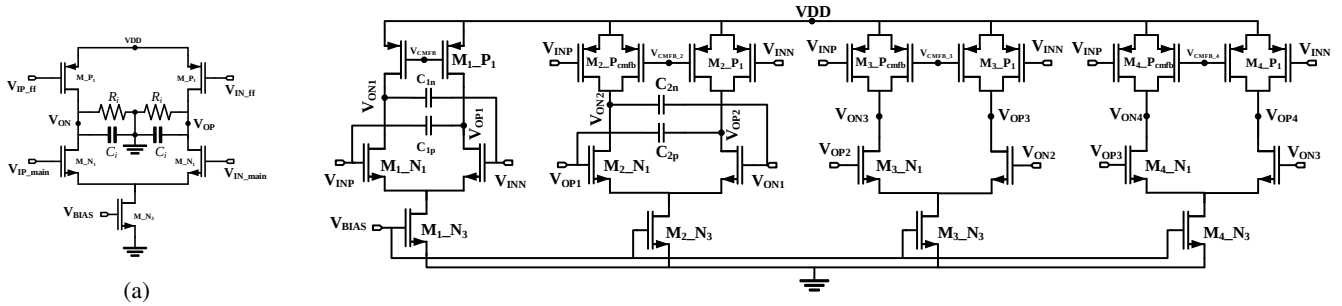
The transconductance of the NMOS pairs can, then, be calculated according to (7). The current and width are the remaining unknowns and they can be estimated using ${}^{g_m}/_{i_d}$ and current density, $j_{n/p}$, values as $i_d = {}^{g_m}/({}^{g_m}/_{i_d})$ and $W_n = {}^{i_d}/_{j_n}$. The ${}^{g_m}/_{i_d}$ and current density values can in turn be found from a lookup table generated for the specific technology using, for example, alogrithms described in [7]. Similar steps can be followed to calculate the transconductance of the PMOS pairs or the width can be directly determined from the current of the NMOS pairs and the current density of the PMOS pairs.

The final designed amplifier is drawn in Figure 5b. The first stage has no feed-forward input, so the PMOS pairs are biased by the common-mode feedback (CMFB) voltage. To minimize thermal noise in the input stage, a non-resistive common-mode sensing is adopted. The PMOS transistors in stages two to four are divided into two to accommodate the CMFB voltage.

Table I: Sizing of the transistors of the 4th-order amplifier

	1st-stage	2nd-stage	3rd-stage	4th-stage
P_1/P_{min}	50	18	36	144
P_{cmfb}/P_{min}	–	4	14	10
$N_1/N1_{min}$	27	9	18	32
$N_3/N3_{min}$	36	16	36	176
$P_{min} = N1_{min} = {}^{600nm}/_{180nm}$, $N3_{min} = {}^{2700nm}/_{320nm}$				$L_{P1} = L_{N1} = 80nm$ §
$I_d[mA]$	2.074	0.9129	2.044	12.944
I_{cmfb}	0.341	–	0.546	–

§ only for 4th-stage, others are set at 180 nm.



(a) (b)

Figure 5: a)The unit differential pair used in construction of the 4[th]-order FF-compensated amplifier, and b) The 4[th]-order FF-compensated op-amp. CMFB circuits not shown.

Table II: Comparison of the designed op-amp with similar works featured in bandpass ΣΔ modulators

REF.	Gain [dB]			f_u	VDD	P.	Tech.
	250MHz	1GHz	2GHz	[GHz]	[V]	[mW]	[nm]
[1]	60	19 ‡	8 ‡	6	1/2.5	100	65
[4]	30	15 ‡	6 ‡	3 ‡	1.25	2	65
[6]	50	28	11	7	1.2	10	65
This work	54	35	23	11	1.2	23	65

‡ estimated from plots

Common-mode correction based on RC networks is used in stages two and four, while stage three features a broadband CMFB amplifier [8]. A pair of cross-coupled capacitors in stages one and two help in improving the phase margin of the amplifier. Due to the high-current at each stage, thick transistors are chosen for the tail transistors. The sizes of each transistor are enumerated in Table I.

IV. Results and Comparison

The plot in Figure 6 depicts the simulated frequency response of the designed amplifier for the loading conditions it encounters in the resonator of Figure 1. It achieves a gain of 53.5 dB, 47.5 dB and 23 dB at 250 MHz, 1 GHz and 2 GHz frequencies respectively when loaded with a capacitor of 440 fF and a resistor of 300 Ω. The amplifier is stable with a phase margin of 54° and a minimum phase of -150°. The thermal noise performance of the amplifier is plotted in Figure 7. To make the results at different input resistances and sampling frequencies comparable, the quality factor of the resonator is maintained at $Q \sim 50$ while the feedback resistance is varied from 47 Ω to 158 Ω. The input noise at f_s of 4 GHz is marginally low owing to the fact that the feedback resistance is higher for the same Q. Despite the amplifier producing a relatively low input noise, 2.2 $nV/\sqrt{Hz}$, the signal-to-noise ratio (SNR) values deteriorate with increasing value of R_{in}.

To put the results in context, the work is compared with recently reported FF-compensated amplifiers of bandpass ΣΔ modulators in Table II. The amplifiers in [1], [4], [6] were designed to work in ΣΔ modulators at f_s = 0.8 GHz, 0.8 GHz and 1 GHz respectively. This work achieves the highest unity-gain-frequency at 11 GHz. It consumes 13 and 21 mW more than [4] and [6] respectively.

However, it improves the gain at 2 GHz by 12 dB compared to [6] and by 17 dB with respect to that of [4]. Compared to [1], this work improves the gain performance at both 1 GHz and 2 GHz by 15 dB.It also consumes less than 25% while relying only on a 1.2 V supply.

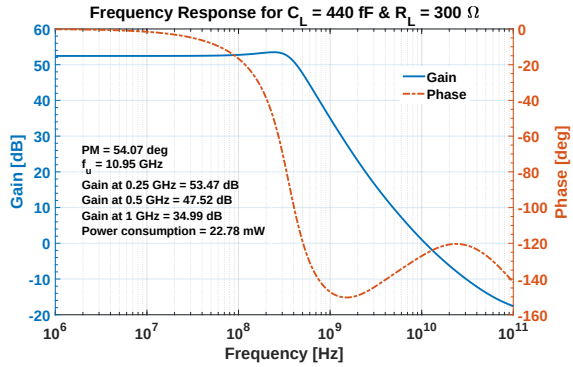


Figure 6: Gain and phase responses of the loaded amplifier

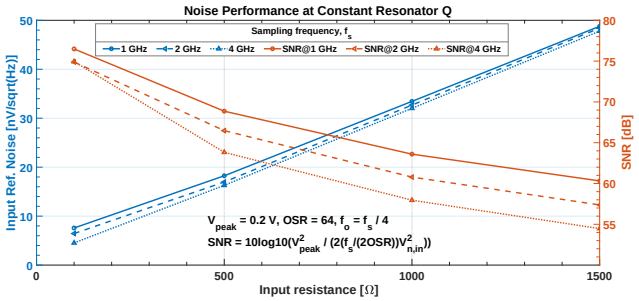


Figure 7: Input-referred thermal noise and the thermal-noise limited SNR for different R_{in}

V. Conclusion

Tunable, high-speed bandpass ΣΔ modulator ADCs are key blocks of a multi-standard highly-digital radio receiver. Continuous-time topologies with active-RC single-amplifier resonators are chosen for small area and low power consumption implementation. In this work, design of a 4[th]-order FF-compensated amplifier is presented with in-depth discussion of different design methods. The designed amplifier produces a low input referred thermal noise at 2.2 $nV/\sqrt{Hz}$. Compared to recently reported works, it achieves the highest unity-gain-frequency at 11 GHz and the largest gain at 1 GHz & 2 GHz. This performance enables it to meet multi-GHz sampling frequency bandpass CT ΣΔ modulator ADCs requirements.

References

[1] H. Shibata, R. Schreier, W. Yang, A. Shaikh, D. Paterson, T. C. Caldwell, D. Alldred, and P. W. Lai, "A DC-to-1 GHz Tunable RF Delta Sigma ADC Achieving DR = 74 dB and BW = 150 MHz at f0 = 450 MHz Using 550 mW," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2888–2897, Dec. 2012.

[2] R. Zanbaghi, P. K. Hanumolu, and T. S. Fiez, "An 80-dB DR, 7.2-MHz Bandwidth Single Opamp Biquad Based CT Delta Sigma Modulator Dissipating 13.7-mW," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 487–501, Feb. 2013.

[3] H. Chae and Flynn, Michael P., "A 69 dB SNDR, 25 MHz BW, 800 MS/s Continuous-Time Bandpass Modulator Using a Duty-Cycle-Controlled DAC for Low Power and Reconfigurability," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 649–659, Mar. 2016.

[4] H. Chae, J. Jeong, G. Manganaro, and M. P. Flynn, "A 12 mW Low Power Continuous-Time Bandpass delta sigma Modulator With 58 dB SNDR and 24 MHz Bandwidth at 200 MHz IF," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 405–415, Feb. 2014.

[5] A. Edward, Q. Liu, C. Briseno-Vidrios, M. Kinyua, E. G. Soenen, A. I. Karsilayan, and J. Silva-Martinez, "A 43-mW MASH 2-2 CT SigmaDelta Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 448–459, Feb. 2017.

[6] X. Yang and H.-S. Lee, "Design of a 4th-order multi-stage feedforward operational amplifier for continuous-time bandpass delta sigma modulators." in 2016 IEEE Int. Symp. on Circuits and Systems (ISCAS), May 2016, pp. 1058–1061.

[7] P. G. Jespers and B. Murmann, *Systematic design of analog CMOS circuits using pre-computed lookup tables*. Cambridge ; New York: Cambridge University Press, 2017.

[8] L. Luh, J. Choma, and J. Draper, "A continuous-time common-mode feedback circuit (CMFB) for high-impedance current mode application," vol. 3. Lisboa, Portugal: in 1998 IEEE International Conference on Electronics, Circuits and Systems. Surfing the Waves of Science and Technology (Cat. No.98EX196), Sep. 1998, pp. 347–350.