A CMOS Analog Front-End for Tunnelling Magnetoresistive Spintronic Sensing Systems

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Abstract—This paper presents a CMOS readout circuit for an integrated and highly-sensitive tunnel-magnetoresistive (TMR) sensor. Based on the characterization of the TMR sensor in the finite-element simulation, using COMSOL Multiphysics, the circuit including a Wheatstone bridge and an analogue front-end (AFE) circuit, were designed to achieve low-noise and low-power sensing. We present a transimpedance amplifier (TIA) that biases and amplifies a TMR sensor array using switched-capacitors external noise filtering and allows the integration of TMR sensors on CMOS without decreasing the measurement resolution. Designed using TSMC 0.18 µm 1V technology, the amplifier consumes 160 nA at 1.8 V supply to achieve a dc gain of 118 dB and a bandwidth of 3.8 MHz. The results confirm that the full system is able to detect the magnetic field in the pico-Tesla range with low circuit noise (2.297 pA/√Hz) and low power consumption (86 µW). A concurrent reduction in the power consumption and attenuation of noise in TMR sensors makes them suitable for long-term deployment in spintronic sensing systems.

Keywords—*CMOS front-end; Tunnel-magnetoresistance; Spintronic; ultralow noise.*

I. INTRODUCTION

Over the past decade, spintronic sensing has become an emerging methodology to emulate sensing and processing in wide applications from biosensing [1] to neuromorphic computing [2]. The early developments of magnetic biosensing were dominated by superconducting quantum interference devices, which require large equipment and operating costs and could not be operated at room temperature [3]. However, there has been substantial progress in developing spintronic devices to reduce system size and improve the detection range [4]. These devices open a new way to measure the weak magnetic field in pico-Tesla/√Hz levels locally at room temperature [5]–[7].

Through tunnel magnetoresistance (TMR) effect [8], [9], spintronic sensors can measure weak magnetic fields generated in the heart, and brain of humans by the electrical activity in various tissues [10]. In this respect, the TMR sensors has to be structured in form of the miniaturised wearable and implantable systems. Combining TMR sensors with CMOS technology offer miniaturise biomagnetic system enabling them to provide fully autonomous performance. For such integration, the CMOS analogue front-end (AFE) subsystem is a key unit that handles the readout the spintronic sensor output, amplification, power management, and noise cancellation [11], [12]. Low power circuitry design is essential to preserve long battery life and maximize the working hours, while the low input-referred noise guarantees accurate data acquisition. In addition, the
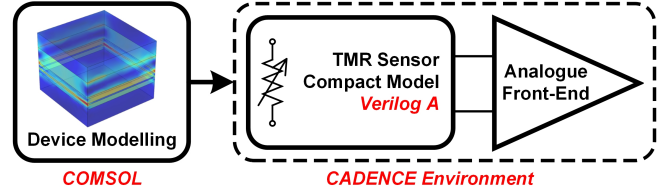

Fig. 1. Proposed idea for extracting spintronic sensor data from *COMSOL Multiphysics*® to *Cadence*© environment for the AFE design.

large dynamic range and small harmonic distortion are also important for weak magnetic signal recordings [13]. Furthermore, the AFE in CMOS technology will process the spintronic sensors outputs to secure a maximum signal to noise ratio [14].

The sensitivity and resolution of spintronic sensors can be improved by using a suitable readout circuitry while the associated environmental noises, e.g. the magnetic field of the Earth and 1/*f*, are attenuated. In this paper, we present a low-power low-noise AFE for a spintronic-CMOS sensing system. The overview of the proposed sensor system is shown in Fig. 1. A finite element method (FEM) model of a TMR device for extensive and accurate physical simulations was carried out with the software *COMSOL Multiphysics*®, to optimize its geometry and materials. Then the parameters of this model were exported into Cadence using *Verilog-A* language so that the model can be integrated into a standard CMOS-based AFE circuit, which can provide on-chip signal processing and noise/offset cancellation [15].

II. ARCHITECTURE OVERVIEW

The schematic diagram of proposed CMOS readout circuit integrated with TMR sensors is shown in Fig. 2. A couple of TMR elements are driven in the current mode and cascaded to a chopper-stabilized current integrator determine the output voltage and a switched-capacitor filter drives the output pads. Here, the Wheatstone bridge, a basic structure of the TMR sensor array, can increase the sensitivity of spintronic sensing and eliminate output offset from the temperature. From the theoretical calculation of voltage- and current-mode configurations, the sensitivity in the current-mode with an equal change of the resistors is twice larger than the voltage-mode [16]. Therefore, a bias current is adopted to drive such system where the final output current from the bridge will be sent to the amplifier, filter, and an analog-to-digital converter respectively. The following sub-Sections describe the circuital implementation of each block of the system.

A. Tunnelling-Magnetoresistive Sensor Design

Spintronic sensors based on the TMR effect have been widely utilized in detecting low magnetic fields owing to their small physical size, reduced cost, excellent linearity and high
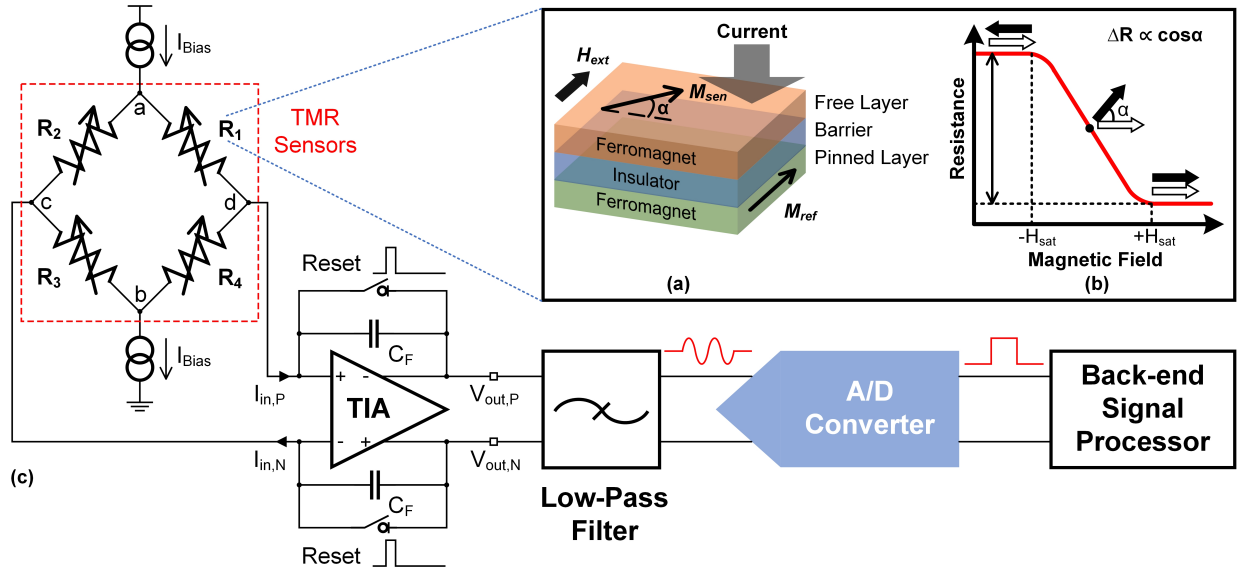
Fig. 2. System block diagram of (a) current perpendicular-to-plane configuration for TMR sensing, (b) R(H) linear behaviour and typical magnetization orientations correspondence; (c) a CMOS AFE with integrated TMR sensors.

sensitivity operated at room temperature [1]. This type of sensors is based on a nanoscale phenomenon in which, under the right conditions, electrons can tunnel through a very thin ordinary insulating material, which is called the TMR effect. Fig. 2(a) shows its basic structure consisting of free layer/barrier/pinned layers, and its transfer curve is demonstrated in Fig. 2(b). When a bias voltage is applied to the TMR sensor, electrical conducting properties is exhibited, and its electrical resistance has a linear relationship with the magnetic field strength over a certain field range. This occurs due to the dependence of the tunnelling probability on the relative orientation of the magnetization in the two ferromagnetic layers between the barrier. The largest and lowest resistances are obtained when the FM layers are operated in antiparallel and parallel orientations respectively.

To find the most effective structures and materials, a current-perpendicular-to-plane geometry of the TMR sensor has been modelled and evaluated by using *COMSOL*

(a)

(b)

Fig. 3. A Full Wheatstone bridge incorporating TMR sensors. Two types of sensors with opposite dR/dH are provided to achieve a full bridge output: (a) mesh created in COMSOL software; (b) magnify of the TMR sensors.

Multiphysics and *Verilog-A* with respect to a higher TMR ratio and better linearization range. The simulation details and specifications of the TMR sensor is described in our previous work [15]. Here, a new simulation structure of CoFeB/MgO/CoFeB based TMR sensors in a full bridge is shown in Fig. 3. The colour legend shows electric potential and magnetic flux density respectively. In this full bridge, there are two kinds of TMR sensors with different and symmetric orientations by setting the original directions of magnetizations of the pinned layer and free layer in 90 degree (R_1/R_3) and -90 degree (R_2/R_4) [15] respectively, which is demonstrated as red arrows. Subsequently, a TMR ratio of 233% with 6 µA bias current is obtained from the finite-element method (FEM) simulations and the TMR models were calculated as

$$R_{1,3} = R_o \times (1 - \alpha \times H_{ext}) \qquad (1)$$

$$R_{2,4} = R_o \times (1 + \alpha \times H_{ext}) \qquad (2)$$

where R_o is an initial resistance, α is a magnetic resistance coefficient, and H_{ext} is the external magnetic field. Therefore, the output current is expressed as follows:

$$I_{out} = I_{bias} \times \frac{\Delta R_I}{R} . \qquad (3)$$

Since the TMR sensor to be imported into *Cadence* environment with its AFE circuits, a magnetoresistor *Verilog-A* compact model was developed and implemented based on a physical point of view in the FEM simulation results [17]. Finally, the value of α was obtained from the linear response of the TMR sensor and the resistance is finally expressed as $R_{TMR} = 3100 \cdot (1 \pm 0.00121864 \cdot H)$ [15], where H_{ext} is ranging between [-5, +5] Oe.

Furthermore, the stability of the sensor output is essential and must be ensured over a large range of temperatures. Therefore, integrating the TMR sensors in a full Wheatstone bridge is highly demanded. Instead of a single TMR sensor, this method will cancel the temperature drift and provide a null-voltage output in the absence of an external magnetic field [18]. As shown in Fig. 2(c), when a current is driven through terminals a and b, the values of R_1 and R_3 are increased or decreased meanwhile R_2 and R_4 are changed in an
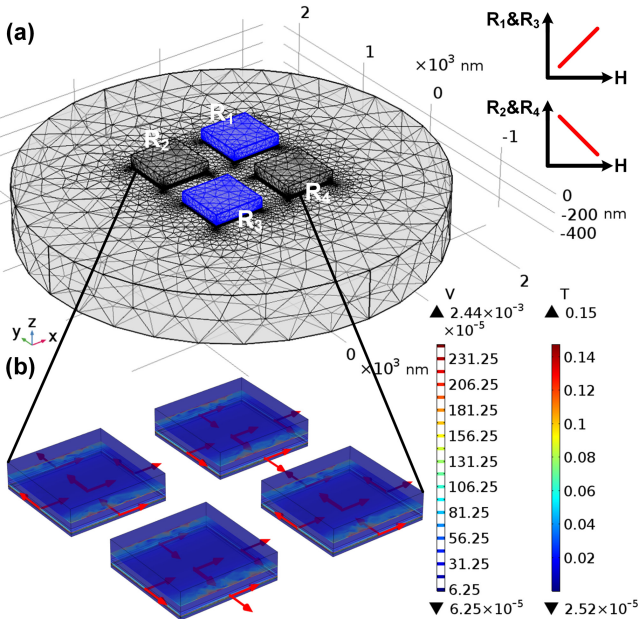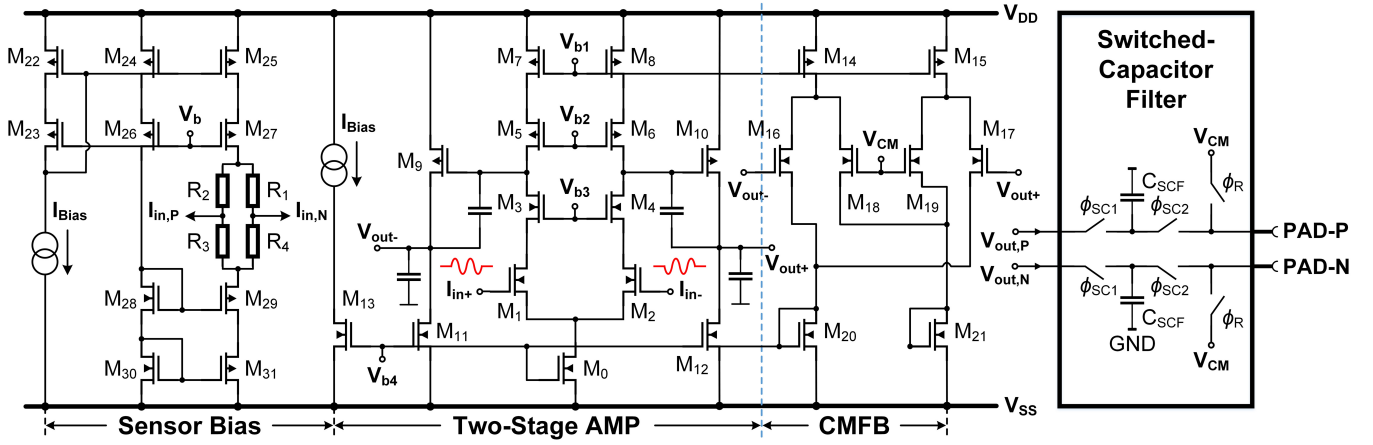
Fig. 4. Schematic diagram of the proposed TMR system.

opposite way. Finally, a full bridge behavior is achieved. Sensor input currents are set through terminals *a* and *b*, while the output currents are measured at terminals *c* and *d*.

B. Readout Circuit

The AFE comprises of a current to voltage converter, which is directly connected to the Wheatstone bridge outputs where the signal levels can be very low. In other words, the differential output currents of the TMR sensors are fed to the read-out circuit, which shall guarantee low noise and offset. The circuit design includes an operation amplifier, a bias circuit, a common-mode feedback and a low-pass filter.

1) Design of Operational Amplifier: The schematic diagram of the integrated TMR sensors is shown in Fig. 4. Our proposed operational amplifier (op-amp) featuring high DC gain and chopper stabilization realizes the current integration. Here, to eliminate the input offset and low-frequency noise, chopper switches is adopted based on a modulation-demodulation technique. The chopper switches modulate the input signal, amplify the modulated signals, and then demodulate the modulated and amplified signals. As a result, the signal is modulated, amplified and then demodulated back to the baseband. On the contrary, the input offset and *1/f* noise voltages of the amplifier are only amplified and modulated. Therefore, they can be removed by a low pass filter. In addition, the input chopper in a NMOS input differential pair is modulated up to the chopping frequency and then the second chopper transposes the signal at low impedance nodes and demodulates back the signal to cancel out the offset [19].

Here, a two-stage telescopic fully differential amplifier is implemented. The first stage is a telescopic cascode amplifier which enjoy large DC gain, single bias current, high speed, low power dissipation and low flicker noise, while the second stage is typically configured as a simple common source stage so as to allow maximum output swings. It is noted that the differential mode signal path consists of only n channel MOSFETs. That means only NMOS transistors conduct time-varying currents and the PMOS transistors conduct constant currents. This increases the speed of op-amp as the mobility of N channel MOSFET is higher than P channel.

2) Tranimpedence Amplifier: The amplifier is utilized to sense the current signals generated from the Wheatstone bridge and convert them into voltage readout with a maximum signal-to-noise ratio for subsequent signal processing. This current to voltage converter is called transimpedance amplifier (TIA), which typically has two kinds: fully differential *a)* resistive feedback and *b)*

capacitive feedback. In terms of the former, the resistor itself is the main noise source. This limits the maximum transresistance gain of the sensor interface. However, the capacitive feedback is like a integrator, which not only can convert the bridge output current into an analog voltage but also enjoy less input current noise. More concretely, the use of a low-noise op-amp enables the integration of the signal current with a very low residual offset and ensures superior voltage sensitivity, integrating the currents over the capacitor for a given period of time after a reset. This method grants a better noise performance, provides a transresistance gain proportional to the integration time, and achieves high common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). If the TIA is realized with a Miller compensated two-stage structure shown in Fig. 4, the transfer function can be derived approximately as [19]

$$H(s) \approx \frac{C_{in}}{C_F} \frac{1 - s \dfrac{C_F}{A_{V,st1} g_{m,st2}}}{\left(1 + \dfrac{1}{sR_P C_F}\right)\left(1 + s \dfrac{C_C C_{in}}{g_{m,st1} C_F}\right)} \qquad (4)$$

where $g_{m,st1}$ and $g_{m,st2}$ are the transconductances of the first stage and the second stage respectively, $A_{V,st1}$ is the voltage gain of the first stage, C_C is the Miller compensation capacitor, C_{in} is the input capacitance of the op-amp (each terminal), R_P is the MOS-BJT pseudo-resistor that occupies small area but can realize large resistance [20].

In addition, two reset switches are added to initialize the input and output nodes to the common-mode voltage quickly before the amplifier starts to operate or reset the amplifier when the output is saturated [21]. Another critical aspect in design of the TIA is the input-referred noise. According to [22], the input-referred noise current for the resistive feedback can be obtained as the output-referred noise voltage divided by the transresistance gain of the TIA:

$$\overline{i_n^2} = \frac{2kT}{R_F} + \left(\overline{V_{n-op}^2}\right)\frac{\left(1 + jwR_F C_{in}\right)^2}{4R_F^2}. \qquad (5)$$

Similarly, the input-referred noise current of the capacitive feedback TIA can be expressed as

$$\overline{i_n^2} = \overline{V_{n-op}^2}\left(\frac{C_F}{2T}\right) = \overline{V_{n-op}^2}\left(\frac{C_F}{2T} + \frac{C_{in}}{2T}\right)^2 \qquad (6)$$

where *k* is the Boltzmann constant, *T* is the temperature in Kelvin, R_F/C_F is the feedback resistance/capacitance.
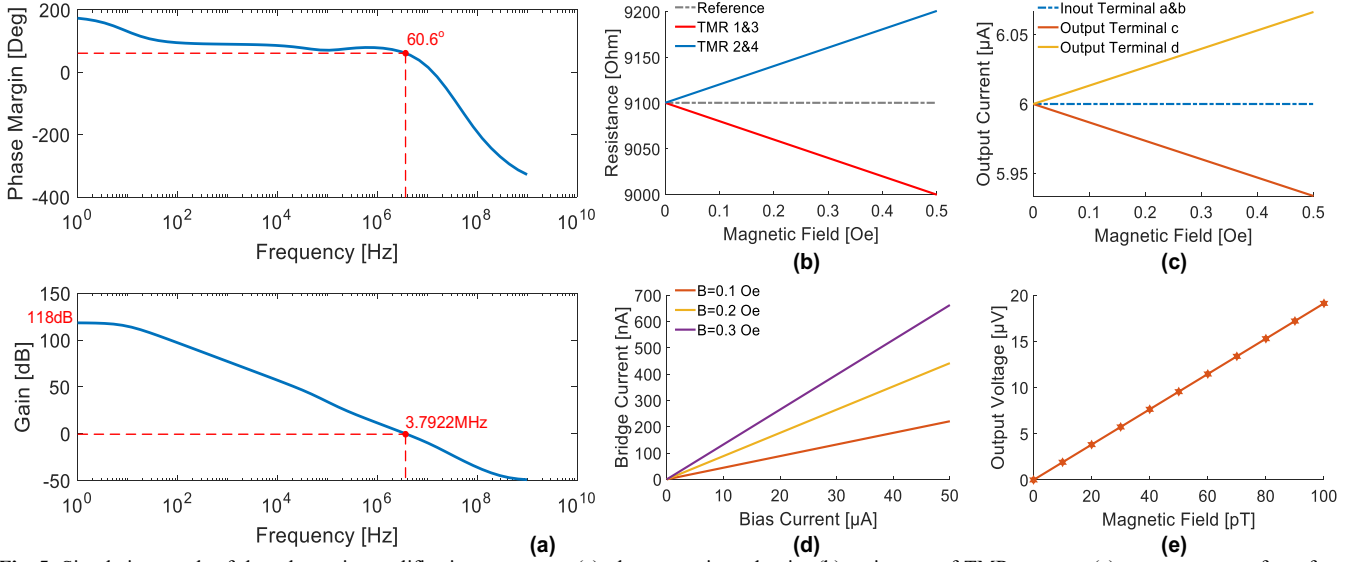
Fig. 5. Simulation result of the telescopic amplifier in two stages: (a) phase margin and gain; (b) resistance of TMR sensors; (c) output currents from four terminals; (d) output current before interface as a function of the biasing current at different magnetic fields; (e) differential output with a 50 μA bias current.

Therefore, to achieve low-power and low-noise sensing and recording system, the key point is to design a low input-referred noise TIA with low power consumption.

3) Common Mode Feedback Circuit: The differential operation has many advantages over single-ended signaling, such as improved immunity to noise, larger output swing, and reduced distortion. However, the high gain circuit needs common mode feedback (CMFB) to stabilize their DC voltages. In addition, a little mismatch between the bias current of pull-up network and that of pull-down network would force the output voltages to go to one of the power supply rails. Therefore, a CMFB circuit is adopted to sense the common-mode voltage, compare it with a proper reference, and return the comparison result to the bias network. As a result, it cancels the output common-mode current components and fixes the DC outputs to the desired level.

4) Switched-Capacitor Filter: Since the output voltages of the integrator are directly connected to the output pads, a quite large parasitic capacitance of the output pads together with the capacitive load of the testing probes will slow down the amplifier response and introduce the risk of instability. As shown in Fig. 4, a simple switched-capacitor filter is employed to overcome this problem. During the integration phase, the output nodes of the amplifier are isolated, and the output pads are kept at the common mode voltage, V_{CM}. At the end of the integration phase, the small switched capacitors CSCF exponentially charge the output pins.

III. SIMULATION RESULTS

The circuitry design simulations are performed in a standard CMOS 0.18 μm process. The low-power telescopic op-amp with a supply voltage of 1.8 V is employed to amplify the Wheatstone bridge output with four TMR sensors. As shown in Fig. 5(a), the DC gain of the op-amp is 118 dB and GBW is 3.8 MHz with a bias current of 50 μA, and the phase margin is 60.6 degree with load capacitors of 1 pF. The telescopic amplifier has enough gain while ensuring low-power and low-noise. The coupling between the two stages uses source followers to accommodate the voltage room necessary for the current chopping of the first stage. In addition, the input-referred noise current is decreasing with a lower feedback resistance and also a lower feedback capacitance. However, at a fixed low frequency, for example 100 Hz biomagnetic field, the capacitive feedback TIA with

reset switches displays a better noise performance of 2.297 pA/√Hz (25.39 pA/√Hz) at a frequency around 10 kHz (100 Hz), which makes it suitable for low-noise and high-resolution applications. The simulated performances of AFE are summarized in Table I. The resistances of the TMR sensors and output current from the Wheatstone bridge are shown in Fig. 5(b) and 5(c) respectively, while Fig. 5(d) shows the differential bridge currents with different bias current in the range of micro-Tesla. The final linear output voltage after the AFE with pico-Tesla level is demonstrated in Fig. 5(e), which has good linearity.

IV. CONCLUSION

In this paper, we present a low-noise and low-power AFE based on a capacitive feedback TIA, which meets the stringent requirements of the spintronic sensing system. The TIA employs differential telescopic pairs in the first stage to ensure ultra-high gain, and a common source in the second stage to provide maximum output swing. The system displays a better noise performance at a low frequency through the capacitive feedback. In addition, a CMFB circuit stabilize DC voltages for such high gain circuit, while a switched-capacitor filter drives the large pins capacitances. Designed in a standard 0.18 μm CMOS technology, post-layout simulation results show that the amplifier achieves good performances in terms of linearity, power, and noise and has the ability to record spintronic signals.

Table I: Main characteristics of the implemented TIA.

TIA Parameter	Post-Layout Simulated Value	
Voltage Supply	1.8	[V]
Power Dissipation	86	[μW]
GBW	3.8	[MHz]
Output Dynamic Range	Full	-
Open Loop DC Voltage Gain	118	[dB]
Input Equivalent Noise	2.297	[pA/√(Hz) @ 100 Hz]
Phase Margin	60.6	[degree]
CMRR	136.62	[dB]
PSRR	181.65	[dB]

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