A MONOLITHIC CMOS REALIZATION OF THE DOUBLE-QUADRATURE IMAGE-REJECT WEAVER RECEIVER

by

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Dedicated to Maggie
who never stopped believing in me

Table of Contents

List of Tables

List of Figures

Acknowledgements

0.1 Acknowledgements

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Abstract

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0.2 Abstract

This work presents a fully-integrated double-quadrature Weaver receiver for monitoring the NIST time and frequency reference radio station WWV across multiple channels in the 2.5-20 MHz range. The design takes advantage of the Weaver architecture's elimination of image rejection filters. The receiver uses a broadband low-noise amplifier (LNA) with an input-referred noise power spectral density (PSD) of < 2.25 nv/Hz$^{1/2}$ for high sensitivity. Instead of large filters, a double-quadrature down-conversion process is used to remove the image signal. Both local oscillators (LOs) are frequency- and phase-locked to each other via an on-chip frequency divider, and their I and Q components are generated by highly-precise digital phase splitters. The receiver was fabricated in the TSMC 180 nm CMOS process and consumes 24.9 mW. Measurements show in-band gain > 40 dB, noise figure (NF) < 2.9 dB, and maximum image rejection ratio (IRR) of 29 dB without calibration.

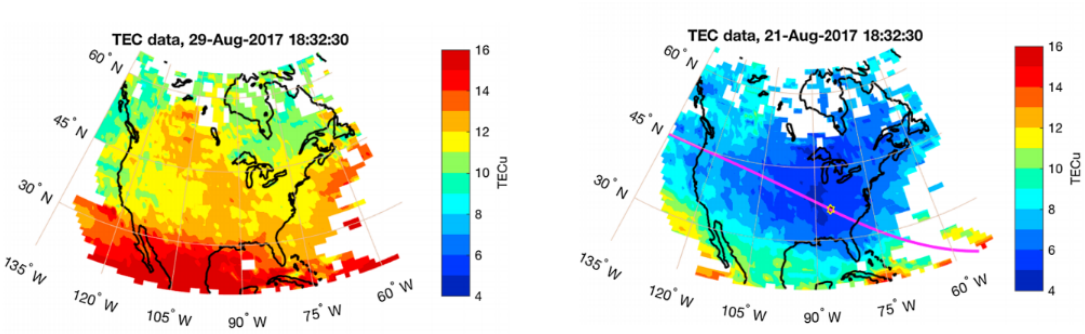
1 Introduction

1.1 Motivation

On August 21, 2017, the United States witnessed its first total solar eclipse since 1979. Unlike the eclipse of 1979, whose path of totality was limited within the United States to the Pacific Northwest, this most recent eclipse swept across the entirety of the country, from Oregon to South Carolina. This rare opportunity to observe a total solar eclipse was seized by millions across the country, with many pausing their daily work schedules in order to witness this event. At the same time, similarly, researchers across the country did not let this opportunity go to waste. One specific area of research focused on the effects of the eclipse on space weather and the ionosphere and, by extension, its effects on signal propagation through Earth's atmosphere.

Signal propagation analysis has had a long history dating back as early as radio itself[7–11]. The difficulty with analyzing signal propagation during the eclipse is the scale of the experiment. Ideally, signal propagation is measured across the entirety of the United States. This requires both a source signal that can be heard anywhere in the United States, as well as receivers geographically spaced across the country. In 2017, GPS was the logical choice[1]. GPS signals are accessible anywhere in the country and GPS monitoring stations can be easily setup wherever needed. While data showed that

the eclipse alone did not affect GPS propagation enough to affect users, its effects were measurable and able to clearly map out the path of the eclipse as seen in Fig. 1.1.



(a) (b)

Figure 1.1. Observations from TEC receivers on (a) 29 August 2017, non-eclipse day, and (b) 21 August 2017, eclipse day presented in [1].

This line of research has helped renew interest in the study of atmospheric signal propagation. Among this renewed interest is specifically interest in investigating propagation of other non-GPS frequencies. As mentioned before, this requires the measurement availability of a geographically broad signal. Conveniently, an RF signal source such as this already exists. WWV radio station is broadcast by the National Institute of Standards and Technology (NIST) on 2.5, 5, 10, 15, and 20 MHz channels out of Fort Collins, Colorado, USA. With an output power of 2.5 kW at 2.5 and 20 MHz and 10 kW at 5, 10 and 15 MHz, WWV can be received across the entire continental United States [7]. Each channel also has excellent frequency accuracy, as one of WWVs primary purposes is the broadcasting of an accurate frequency standard [12]. In addition, its spectrum of channels provide a great series of frequencies for the analysis of signal propagation through the ionosphere.

WWV provides an excellent source of an ionospheric signal, but to be useful in studying propagation, it must be measured at many locations. While building a receiver at any one of WWV's bands is a straightforward task, a receiver that can measure all five WWV channels while remaining simple enough to be built and installed all across the country is more challenging. This provides the motivation to create a net of radio receivers across the country ready to analyze the effects of the 2024 total solar eclipse. It is the topic of this thesis to design and prototype a receiver suitable for the above task.

Decades of CMOS process scaling have greatly reduced the power consumption and cost of digital computing. In particular, FPGA-based software-defined radios (SDRs) have become popular for many RF applications. Unfortunately, the widespread use of SDR-based digital signal processing has resulted in the neglect of simpler analog methods for RF down-conversion and their integrated circuit (IC) realizations. In addition to the eventual goal of measuring the impact on signal propagation of the 2024 eclipse, this work was in large part motivated by the lack of research that presently exists on the subject of Weaver-Hartley radio architecture. Weaver-Hartley radio architecture (as opposed to superheterodyne or direct conversion architectures), has long been underutilized in the design of radio receivers, largely because of the difficulty in realizing these receivers with discrete components. That being said, many of these difficulties do not exist when implemented as an integrated circuit. At the same time, some of the complexities of building a full spectrum WWV receiver match up well with the some of the benefits of a Weaver receiver, primarily its lack of image reject filters (as needed in a superheterodyne receiver) and local oscillator leakage (which can leak back into the input of a direct conversion receiver).

1.2 Research Goals

The goal of this project is to design a CMOS double-quadrature Weaver image-reject receiver for monitoring the five high frequency (HF) channels (2.5, 5, 10, 15, and 20 MHz) broadcast by the NIST-operated time and frequency reference radio station WWV, located in Fort Collins, Colorado, USA[7]. Each band of WWV is double sideband amplitude modulated and contains the same message set to a schedule by NIST. Throughout a given hour the station plays several different highly-precise tones at 440, 500, 600, 1000, and 1500 Hz. A 100 Hz subcarrier also delivers time code information. Additionally, each minute, a human voice reads timing information and twice an hour special announcements. In all, the lower three bands (2.5, 5, and 10 MHz) are allocated 10 kHz in bandwidth, and the upper two bands (15 and 20 MHz) are allocated 20 kHz[13]. Ultimately, the purpose of designing and fabricating this receiver is to characterize WWV signal propagation for ionosphere and space weather studies[14] and all-sky imaging radar[15], with the longer term objective to study these effects during the 2024 solar eclipse.

In order to accomplish this, the receiver needs to be able to meet certain figures of merit. For one, as a measurement device, the receiver should have a relatively high sensitivity and dynamic range to maximize its effectiveness at picking-up WWV broadcasts across various conditions. For the purpose of this project, a sensitivity of less than 1 μV is selected as a reasonable target. A dynamic range of 60 dB is similarly appropriate in order to cover the range of anticipated WWV input signal levels. Gain must also be large enough that lowest input signals are amplified enough to be recorded. In this case, a gain of 60 dB is desirable. In addition to these figures, the receiver must have excellent image rejection to prevent inaccuracies from out-of-band signals, ideally greater than 60 dB. Finally, as these measurements will require multiple receivers spread out geographically

over a wide area, it is important that these receivers are not limited by power consumption. As such, the receiver should minimize power consumption to less than 50 mW. This will enable it to run off a coin-cell battery for upwards of 12 hours, or upwards of a full week if run off a AA battery.

1.3 Literature Review

1.3.1 WWV for Signal Analysis

WWV was officially founded in 1919 in Washington, D.C. by the National Bureau of Standards (NBS) (now the National Institute of Standards and Technology (NIST)), just 18 years after Marconi was able to receive the first trans-Atlantic radio communication. Before founding WWV, the NBS, a branch of the Department of Commerce, had been tasked with researching radio technology for the benefit of nautical navigation. Following World War I, with the ban on private radio stations lifted, the NBS was able to formally establish a radio station for experimentation. By 1923 the station began regularly scheduled frequency broadcasts[7].

Around the same time in the mid 1920's, researchers began experimenting with atmospheric measurements and calculating the heights of the layers of the ionosphere. Two sets of researchers, Appleton and Barnett out of Cambridge University and Breit and Tuve out of the Carnegie Institution of Washington, D.C. wrote a series of papers detailing their research listening for reflected radio signals in the ionosphere. Appleton and Barnett transmitted frequencies between 765-780 kHz (385-392 meters), whereas Breit and Tuve focused on 4.29 MHz (70 meters). This effort was part of the earliest work detailing the day and seasonal cycles of the ionosphere[8–11].

Over the next few decades, WWV went through numerous changes. The location of the transmitter slowly moved further outside of Washington, D.C. into the surrounding Maryland area, and the broadcast frequencies changed frequently[7]. Meanwhile, NBS laboratories were working to constantly improve frequency standards. Perhaps the most abrupt shift in this development began in 1957 with the advent of atomic frequency standards. The redefining of the second and the change from crystal oscillators to atomic clocks drastically improved frequency accuracy[12].

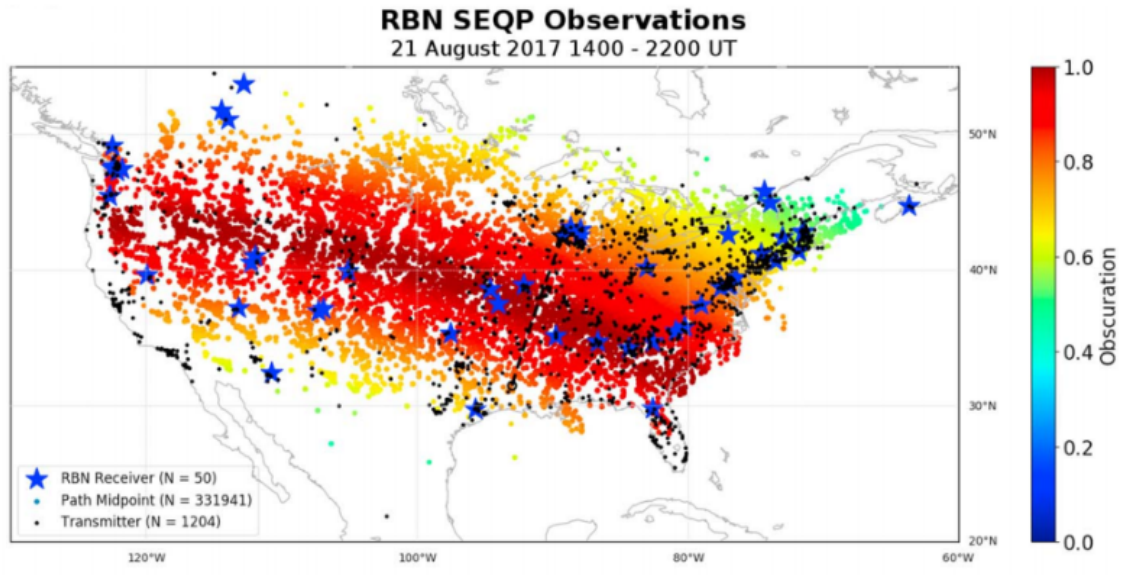


Figure 1.2. RBN observations during the All-American total solar eclipse on 21, August 2017. Midpoints between transmitter and RBN receiver are color coded by their maximum obscuration. RBN receivers are marked as blue stars, and transmitters are represented by black dots. Note the dark path of totality from Oregon to South Carolina[2].

Around this same time researchers began utilizing WWV's broadcasts as a signal source for radio propagation experiments. In 1960 Watts and Davies first measured fading effects by recording WWVs broadcasts over extended periods of time[16]. Fenwick and Villiard performed similar studies in Palo Alto, California over a period of a month and

were able to correlate sudden propagation shifts with sudden magnetic shifts as measured from the same location[17]. Davies continued this work with Baker through the mid to late 1960's[18] while other researchers like Toman, who worked out of Bedford, Massachusetts, focused on the measurement and analysis of the relation between phase and group path[19].

More recent works such as[20] have carried on this legacy of research going further in depth into the analysis of WWV signal paths, while others such as[15] continued to investigate the effects of space weather. The work of this thesis is specifically interested in continuing this research during the next American total solar eclipse in 2024. The effects of solar eclipses on the ionosphere has been studied as far back as Sears' paper on the 1970 eclipse[21]. More recently, during the last American total solar eclipse, researchers across the country setup experiments to analyze its effects on propagation. Researchers at MIT Haystack Observatory were able to map the eclipse from GPS data collected during the event[1]. Another research group, primarily based out of the New Jersey Institute of Technology, recruited a network of amateur radio operators to record their communications during the eclipse on the 1.8, 3.5, 7, and 14 MHz bands, and were also able to effectively map the path across the country, as seen in Fig. 1.2[2,22].

1.3.2 Software Defined Radio (SDR)

Software-defined radio (SDR) has come a long way since its development by the United States Navy in the early 1990's. While the first operational device was so large that it occupied the back of a transport vehicle[23], modern consumer SDRs are available that are the size of a USB thumb drive[3] (Fig. 1.3). It is projected that by the year 2021, the market for SDRs will exceed USD 29 billion[24]. The basic idea of software defined radio is to implement as much of the receiver (and/or transmitter) digitally as possible. In its

Figure 1.3. Commercial USB thumb drive sized SDR[3]

ideal form this would limit the analog hardware to only an analog to digital converter (ADC), directly connected to the antenna. All signal processing would be performed digitally on the microcontroller connected to this ADC. This enables all the features of a receiver to be configurable via software, without the need to change or tune hardware. Modern ADCs are generally not fast or sensitive enough to design an ideal SDR, instead they require some analog front end gain and donwnconversion before being digitized[25].

Ultimately, the high configurability of SDRs available make them extremely flexible, and as such, very desirable. By the year 2020, it is projected that there will be over 7 trillion wireless devices around the world. With so many devices it becomes increasingly helpful to be able to reuse the same hardware for different applications[24]. Using the same hardware benefits greatly from economies of scale, while the software can be configured as required for each application. At the same time, this range and flexibility generally makes SDRs a good measurement tool. In the case of WWV monitoring, the ultra-wide spacing of channels lends itself well to SDR. This, alongside the fact that the

inherent digitization of the signal processing interfaces well with a computer that is often used for collecting and reporting any measurement data, gives SDR consideration for this task.

Table 1.1. Comparison of Quadrature Image-Reject Receivers

Parameter	**RTL-SDR**[3]	**SDRplay RSP1A**[26]	**Airplay HF+**[27] **Discovery**	**KiwiSDR**[28]
RF band	500 kHz – 1766 MHz	1 kHz – 2 GHz	0.5 kHz – 31 MHz 60-260 MHz	10 kHz – 30 MHz
Power	1400 mW	925 mW	1700 mW[29]	1300-5000 mW
Sensitivity	$\approx 3\ \mu$V[30]	0.48-0.89 μV	0.02 μV	3.15 μV[31]
Cost	\$ 29	\$ 109[32]	\$ 169[33]	\$ 299 (full kit)[31]

That being said, ultimately, software defined radio is not necessarily preferable to an all analog approach. The biggest problem with digital signal processing is that it has to be fast enough to sample new data and process it in real time. Therefore, the savings in front-end hardware must be made up for with more powerful digital processing. This trade-off generally manifests itself in two ways, higher cost of the device, and greater power consumption. As seen in Table 1.1, only the newest, and more expensive SDRs available commercially have high enough sensitivities for the operating range in question. The problem is, regardless of price, every option available uses a significant amount of power, at minimum 925 mW. In addition, what Table 1.1 doesn't show, is that most options available to consumers do not operate within the frequency range of WWV. Limited options only allow for more expensive devices that still require significant power.

1.3.3 Comparison of AM Receiver Architectures and Image Rejection Techniques

One of the greatest challenges in the design of AM radio receivers has been the task of separating and removing the image of the desired radio signal. The image itself is a product of the mixing process used when downconverting and demodulating the signal of interest. When the signal of interest is mixed with a local oscillator, the output is both the sum and difference of the two frequencies. Because of this operation, there are always two frequencies that, when mixed with the local oscillator, result in the same output. It is therefore necessary to make sure the second of the two signals, the unwanted image, is removed or risk picking up undesirable interference. With the wide use of wireless signals, the image of a signal of interest often falls outside of its allotted band and will likely interfere with other wireless devices.

Generally, it is accepted that there are three primary strategies for preventing the unwanted image signal from interfering with the desired signal. The simplest and most obvious solution is to filter the input of the receiver such that the signal of interest is within its pass band and the image in its reject band. Alternatively, instead of filtering, the local oscillator used as the second mixing input can be selected to match the signal of interest. If the local oscillator and desired signal's frequencies are the same, the difference component of the output is at baseband. As a result, there is never an image signal to worry about since only the same frequency as the local oscillator results in a zero frequency output. Finally, the last and least common method is through cancellation. This takes advantage of the fact that the message information in the signal of interest and its image, experience equal but opposite phase shifts at the output of the mixer. If multiple

mixing stages are realized along two signal paths, recombining signal paths can cancel the image signal while reinforcing the desired signal.

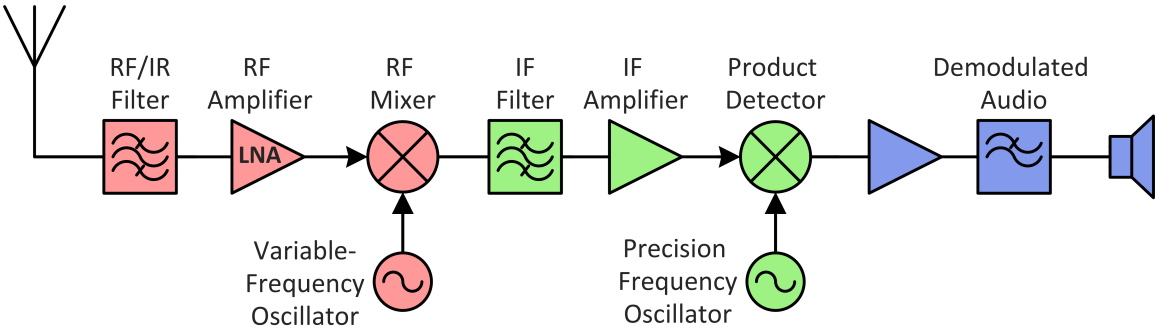


Figure 1.4. Block diagram of a superheterodyne receiver

Each of these techniques is accomplished using a different receiver architecture, each with several advantages and disadvantages. The first of these is the superheterodyne receiver. This architecture utilizes front end image rejection filters at the input to remove unwanted signals. As seen in Fig. 1.4, this design consists of two mixing stages; the first mixes the input with a variable local oscillator that can be adjusted to tune to different channels within the band. This second mixing stage mixes the band-pass filtered output of the first stage with a second local oscillator. The tuning of the first local oscillator is such that the output of this first mixing stage is at the same frequency as the second local oscillator. The result is the demodulated baseband message. The benefit of this is that the first mixing stage can be less accurate since it is actively tuned by the user, while the second mixing stage can be made more accurate as it is only tuned to a single frequency. The downside is that conventional superheterodyne receivers suffer from the need for large image rejection filters, high-Q notch filters, and still depend on variable local oscillators (LOs)[34]. Historically, these issues have been less of a concern when building radios from discrete components. However, in recent years with the advent of monolithic integration, full integration of analog receivers has been restricted by the

difficulty in realizing many of these passive components, specifically the size of on-chip inductors and capacitors required for filtering. Developments in direct digital synthesis (DDS) and PLL-based synthesizers have enabled the integration of programmable LOs, but integrated filtering often remains a problem.

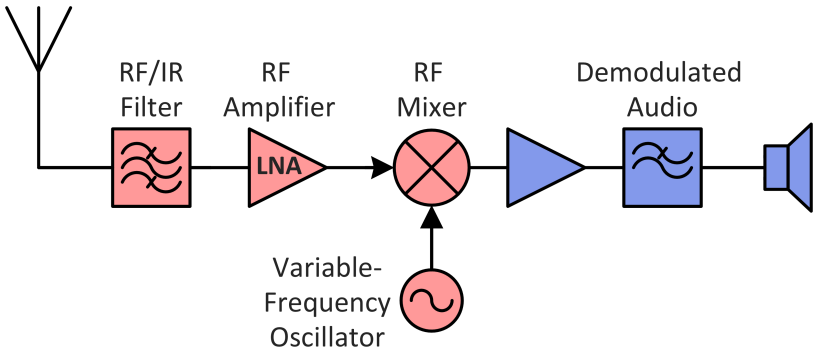


Figure 1.5. Block diagram of a direct conversion receiver

The second of these architectures, direct conversion receivers, solves many of these problems, since they remove the need for image filtering. As seen in Fig. 1.5, this architecture is very similar to the superheterodyne receiver, consisting of only one of the two mixing stages. The second input of this mixing stage, like the first stage in the previous receiver, is fed with a variable local oscillator that is tuned directly to the signal of interest's carrier frequency. This technique directly down-converts the input to baseband and as a result, the image generated from down-converting to baseband is conveniently one of the two sidebands reflected about the carrier. The result is perfect summation of the sidebands, as long as the LO is locked onto the frequency of the carrier. The drawback of this architecture is its sensitivity to the accuracy of LO frequency, as even small errors cause fading due to mismatch between the image and message signals. In addition, direct conversion requires mixing at the same frequency as the RF carrier, which results in LO leakage into the mixer and possibly the antenna[34,35].

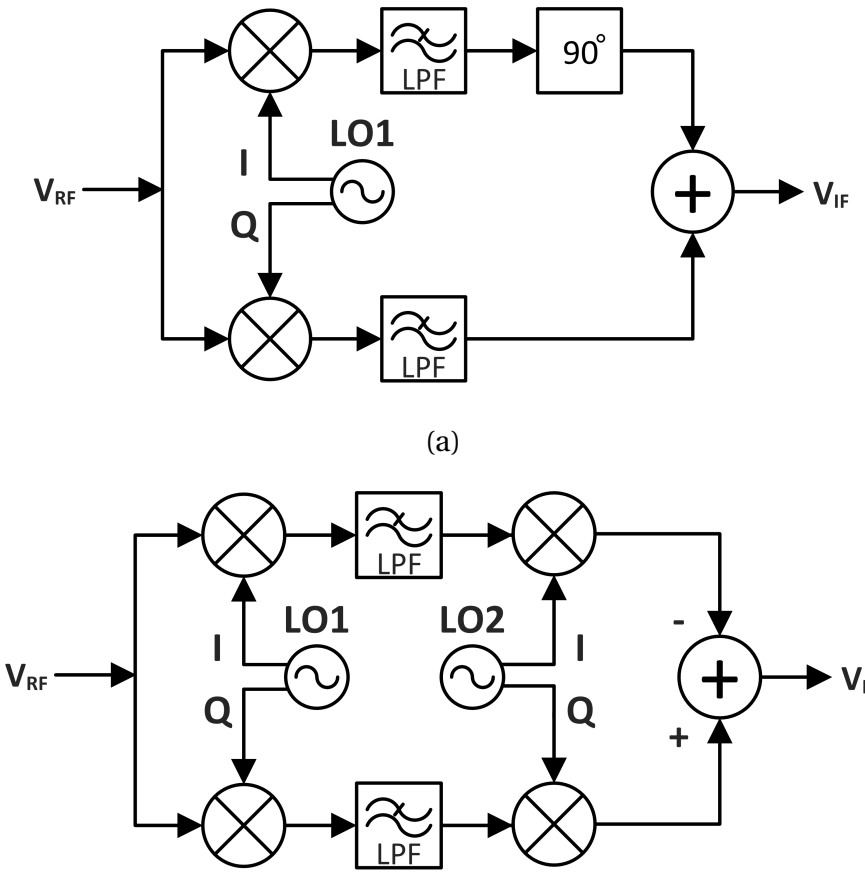


Figure 1.6. (a) Hartley and (b) Weaver image-rejection technique.

This work focuses on a design that employes that last and trickiest image rejection technique. Unlike superheterodyne and direct conversion, Hartley[36] and Weaver[37] image-rejection receivers (see Fig. 1.6) were never widely realized using discrete components. This was mainly due to these architectures' need for i) precise phase control of either the LO or RF signal, and ii) multiple mixers and down-conversion paths with relatively good matching, which increases cost and/or calibration complexity[38]. At the same time, the trade-off between no image reject filters and more mixers works well for

IC realizations. Thus, quadrature image rejection architectures have become more attractive with the advent of improved CMOS technology. The biggest obstacle remains precision phase control of the signal. The Hartley architecture, because a phase shift is created in the signal path, is generally avoided[5]. More common is the Weaver architecture, which uses a second quadrature oscillator but still requires minimization of LO phase and gain errors.

1.3.4 Similar Work

Due to the widespread use of radio receivers, there has been a tremendous amount of work on the design and analysis of the entire range of radio receivers from discrete component to fully integrated designs. While the last section highlighted the main differences between three AM receiver architectures, this section specifically focuses on literature detailing double-quadrature down converting receivers similar to the work presented in this thesis.

Unfortunately, unlike superheterodyne and direct conversion receivers, double-quadrature receivers are under-researched. One reason for this may be the difficulty in designing a discrete component version of the receiver. It is very hard to achieve levels of matching between the six different mixing stages necessary to make this technique effective. The advent of monolithic integration has changed this reality. Nevertheless, the literature on the subject has still been slow to develop. The work that has been done can be separated into three categories. Early work, utilized polyphase filters to generate the 90° LO phase offset with some success[4,34,38,39]. Later work incorporated full calibration loops with tunable delay stages, significantly lowering phase and gain error and improving image rejection[5,40–42]. And finally, recent work focused on digitizing the RF signal at a higher IF frequency, and then implementing the second mixer stage digitally[6,43].

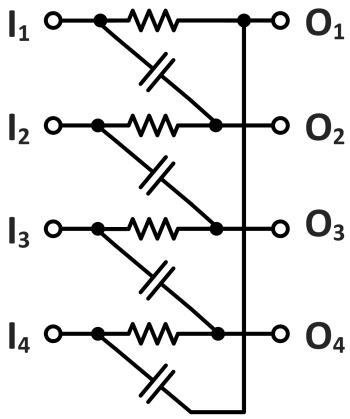


Figure 1.7. Example of passive poly-phase filters presented in[4].

The biggest difficulty in the design of double-quadrature downconverting Weaver receivers is minimizing phase and gain mismatches between signal chains, as these errors are the primary factor in maximizing image rejection. Initial works utilized polyphase filters (see Fig. 1.7) to generate the in-phase and quadrature components of the local oscillators. Careful design of these filters were made to minimize phase error both between I and Q components of each local oscillator[4,34,38,39]. Some designs[4], seen in Fig. 1.8, and[39] incorporate poly-phase filters in the signal path as well to try and minimize mismatch between signal paths. The design of these filters was able to keep phase errors relatively low, but was restricted by the fact that the filters are frequency dependent. As a result, works like[4,34,39] supplement image cancellation with extra internal and external filters. In these cases the image cancellation is used as a technique to improve image rejection by 20-40 dB. On the other hand, works like[38] digitize all four outputs of the second mixing. Doing so enabled the authors to perform a digital automatic gain control (AGC) operation on the signals and drastically reduce gain error.

Later designs[5,40–42] attempted to eliminate the need for precise poly-phase filters in the generation of I and Q components of the local oscillators. Instead, delay stages

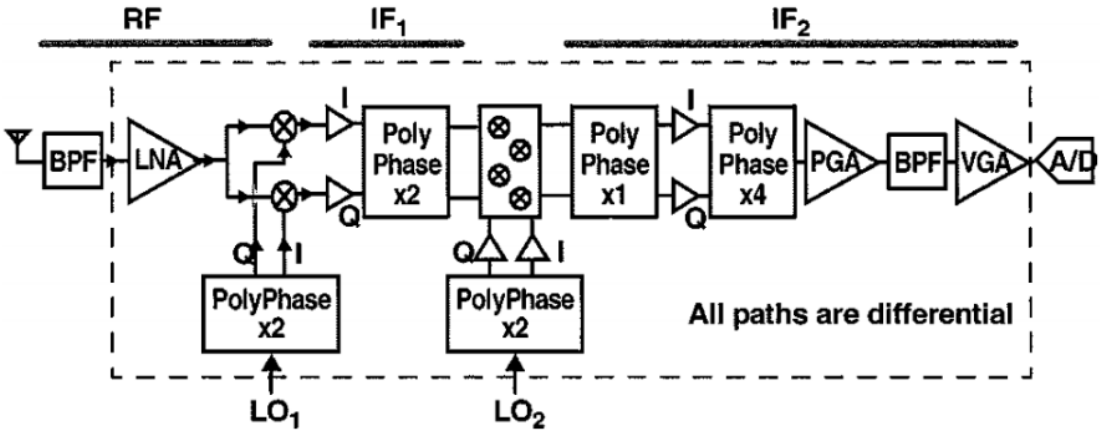


Figure 1.8. Block diagram of receiver presented in[4].

were used in order to directly tune phase between the components. Since they could be easily tuned, the delay stages made it very simple to select between different channels. More importantly, it enabled the implementation of a feedback loop which allowed the direct calibration of the phase. Work such as[40] used simple, single variable feedback loops to calibrate out phase errors. Other works such as[5,41,42] took it a step further and implemented multi-variable least means squared (LMS) calibration loops to account for both phase and gain errors all in one. As seen in Fig. 1.9, feedback from a sign-sign LMS calibration loop adjusts delay in the second local oscillator block and gain amplifiers in the baseband signal path. In all of these cases, the calibration loops improved the image rejection ratios by at least 30 dB.

Unfortunately, the most recent literature on the subject has started to move away from fully integrated receivers. Instead works such as[6,43] focus on utilizing digital signal processing (DSP) as part of the signal chain. Works like[6], seen in Fig. 1.11 only implement the first mixing stage monolithically. The outputs are digitized with an ADC and

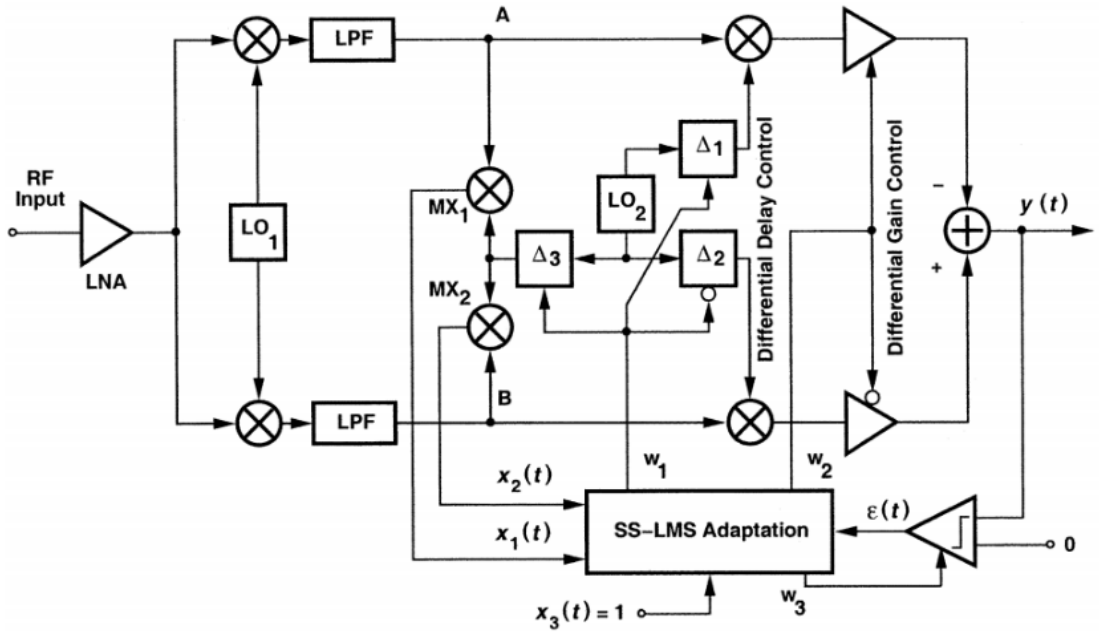
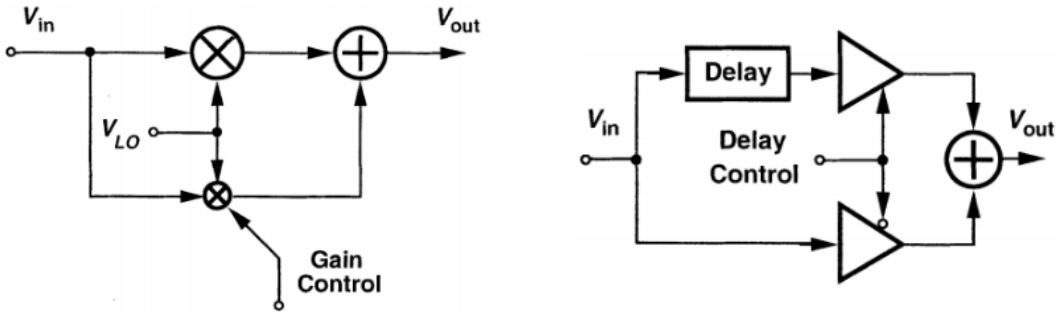


Figure 1.9. Block diagram of receiver presented in[5] with both SS-LMS gain and phase calibration.



(a) (b)

Figure 1.10. (a) Variable gain control and (b) variable delay control presented in[5]

the entire second mixing stage is then implemented digitally. Other works such as[43] realize the calibration loop digitally. In that paper, part of the calibration step includes a

search algorithm designed to find the minimum phase and gain error. Though these designs demonstrate a marked improvement in image rejection, they fall outside the scope of monolithically implemented receivers presented in this thesis.

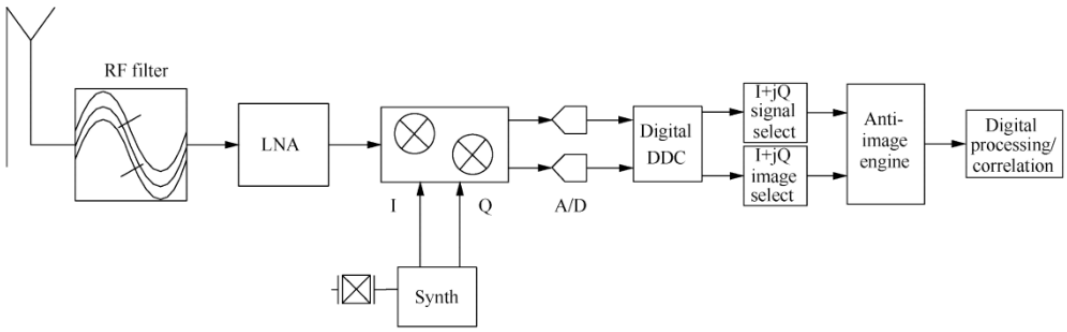


Figure 1.11. Block diagram of receiver presented in[6]. The second quadrature downconversion stage is implemented digitally.

1.4 Structure of Thesis

In this project a full WWV receiver has been designed and fabricated using the TSMC 180 nm CMOS process. A printed circuit board (PCB) was also designed and fabricated to conduct testing of the device. The thesis is broken up into the following parts: Chapter 2 discusses the theory of a double quadrature downconverting Weaver receiver and details in full the design of the chip. Chapter 3 presents the testing setup and resulting measurement data of both the front-end low-noise amplifier and the receiver as a whole. The last chapter, Chapter 4 draws conclusions from the design and test results.

2 Design

2.1 Double Quadrature Downconverting Weaver Architecture

The double quadrature downconverting Weaver receiver derives its architecture from the better-known Weaver single-sideband generation technique first described in Weaver's 1956 paper, A Third Method of Generation and Detection of Single-Sideband Signals[37]. This method uses phase shifted local oscillators to cancel unwanted sidebands and images instead of basic filtering.

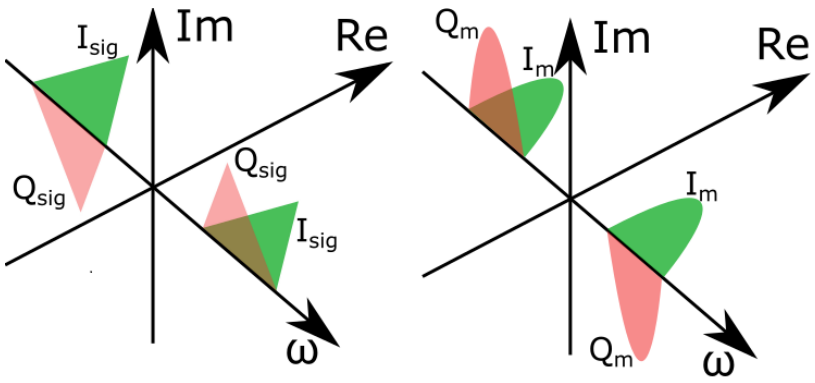


Figure 2.1. Real and imaginary spectra of signal and image for I and Q mixing.

As discussed previously, the Weaver image-rejection architecture is especially useful for monolithic realization of downconverting radio receivers. Much of its advantages derive from the elimination of the superheterodyne architecture's image-rejection bandpass filters. This makes monolithic integration much easier because external filters and

their inductors and capacitors are not needed. Instead, Weaver's architecture utilizes extra mixers for image cancellation, which are much easier and more efficient to realize on an IC. The Weaver double quadrature downconverting receiver is similar to the better-known Weaver single-sideband generation technique in using LO phase shifting to cancel unwanted sidebands and images[37]. It takes advantage of the mismatched response of a signal and its image utilizing quadrature mixing for obtaining quadrature image rejection. When mixed with a quadrature of the LO, the signal and image are still summed together, but are each 90° out of phase with their in-phase equivalents (see Fig. 2.1). The difference is that the image and the signal are rotated in opposite directions and end up 180° out of phase. By implementing a second quadrature mixing stage, the signal and message are both shifted by 90° again, but this time in the same direction (since they are now at the same frequency). The final result is a message signal that is 180° out of phase with the in phase signal path and an image that remains 0° out of phase with its in phase equivalent.

A simple differential amplifier recombines the two signal paths which cancels out the images while reinforcing the message signal. If the second mixing stage directly downconverts the signal to baseband there is no secondary image to consider. However, even if downconverted to low-IF, the second image will undergo the same phase shifts, but in the reverse direction of the first image and thus still cancel out[35]. Real and imaginary spectra of signal and image for I and Q mixing. The Weaver technique provides a single in-phase output. For designs that mix down to zero-IF and need to retain magnitude and phase information (such as the design presented here), both in-phase (I) and quadrature (Q) outputs are necessary. We use two additional mixers in the second mixing stage for this purpose, as shown in Fig. 2.2. Unlike the conventional receiver, each IF

path is mixed with both the in-phase and quadrature phases of the second LO, resulting in four outputs. As in the conventional receiver, the two original mixer outputs are still combined in a differential amplifier to create an in-phase output. However, the two new mixer outputs are also now summed in order to create a quadrature phase output.

2.2 Block Diagram and Receiver Architecture

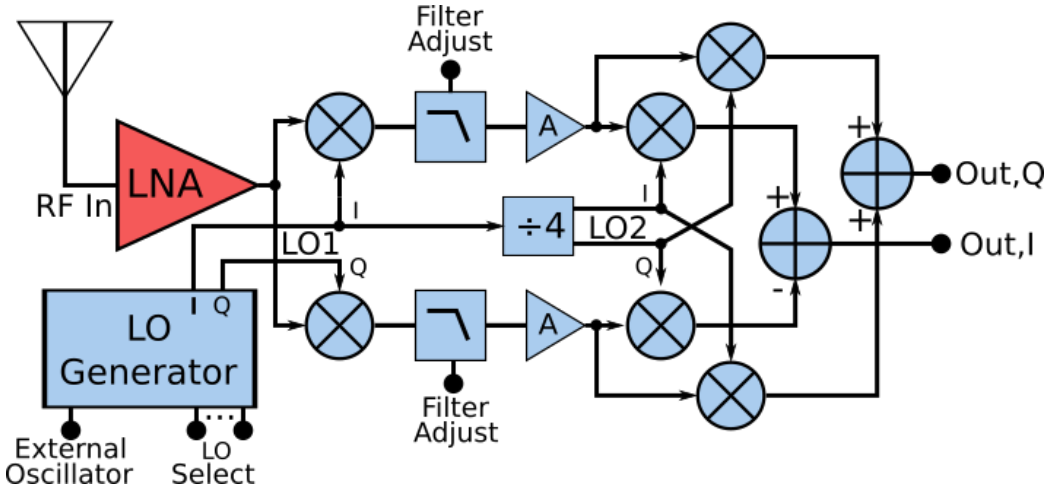


Figure 2.2. Block diagram of the proposed double-quadrature Weaver receiver.

A simplified block diagram of the entire receiver is shown in Fig. 2.2. As discussed in the previous sections, WWV is broadcast over five channels (2.5 MHz, 5 MHz, 10 MHz, 15 MHz, and 20 MHz) with the end channels (2.5 MHz and 20 MHz) broadcast at 2.5 kW and the center channels (5 MHz, 10 MHz, and 15 MHz) broadcast at 10 kW. As a result, field strength across most of the continental United States is greater than 100 $\mu V/m$ under normal conditions[13]. As a measurement device, this project aimed to have sensitivity, high enough to record all five channels, under all conditions, across the entire United States (less than −120 dBm). With the quantization step size of a moderate resolution analog to digital converter around 1 mV, the device needs to have gain of around

60 dB. On the opposite end, the device must be able to handle the strongest signals from WWV as high as −50 dBm. Since device operation prevents output signals greater than about 4 dBm, selectable gain must be used to prevent clipping of inputs larger than about −50 dBm.

As seen in Fig. 2.2, the entire device is comprised of five building blocks: a low noise amplifier, mixers, low pass filters, amplifiers (including the summing amplifiers), and a clock generator. The input of the device is a low noise amplifier (LNA) designed to match a 300 Ω antenna source. This LNA feeds directly into two mixers as part of the first downconversion step. Each of these mixers are passive mixers driven by the I and Q versions of the first local oscillator (LO1). The first local oscillator is created from an external clock source that is digitally divided down by a programmable clock divider to four-fifths the frequency of the desired WWV channel (RF input) which, when mixed with the input, creates an intermediate frequency (IF) of one-fifth the frequency of the input. The output of the mixer is a combination of the sum (nine-fifths the input frequency) of the mixer inputs, the difference (one-fifth the input frequency), and mixer leakage.

In order to remove the undesired components of the mixer outputs, each output is low pass filtered through a tuneable, fourth-order G_m-C filter. Mixer leakage at four times the frequency of the IF is attenuated by greater than −49 dB and the summed product of the mixing stage at nines times the frequency of the IF is attenuated by greater than −76 dB.

The outputs of the low pass filters (LPFs) in both branches are then buffered and amplified by non-inverting, externally programmable and tunable, variable gain amplifiers (VGAs). The externally programmable gain allows the gain of the amplifiers to be

decreased for strong input signals. It should be noted that automatic gain control (AGC) was avoided because this device was specifically designed for the purpose of measuring RF signal propagation characteristics, rather than for wireless communications. Though it is common for other measurement receivers utilize the AGC feedback loop to calculate input signal strength, this technique, in order to be accurate, adds an extra level of complexity that was unnecessary for this initial design.

At this point, each IF path is fed from the gain stage into two mixers which are mixed with the I and Q of the second local oscillator (LO2) in the second downconverting stage. The second local oscillator is one-fourth the frequency of the first local oscillator, the same as the intermediate frequency, so that when mixed with the IF, down converts the signal to baseband. The four mixers used in this stage each result in a baseband output signal that, if low pass filtered, would be the isolated WWV message signal (although the image of the first mixing stage would remain). While it may seem inconvenient that the second mixing stage requires four mixers, this actually comes as an advantage because it makes the design more robust to quadrature unbalance than a conventional Weaver receiver. This is because in both mixing stages the signal path(s) must drive two mixers, resulting in any unbalance being equal in all paths[42]. The outputs of these four mixers represent different components of the message signal at baseband, namely I-I, I-Q, Q-I, and Q-Q. The I-I and Q-Q signal paths are fed into a differential amplifier to create the image-less in-phase message signal, and the I-Q and Q-I signals are summed together to create the image-less quadrature message signal. Finally, both outputs are low-pass filtered off-chip to define the final bandwidth.

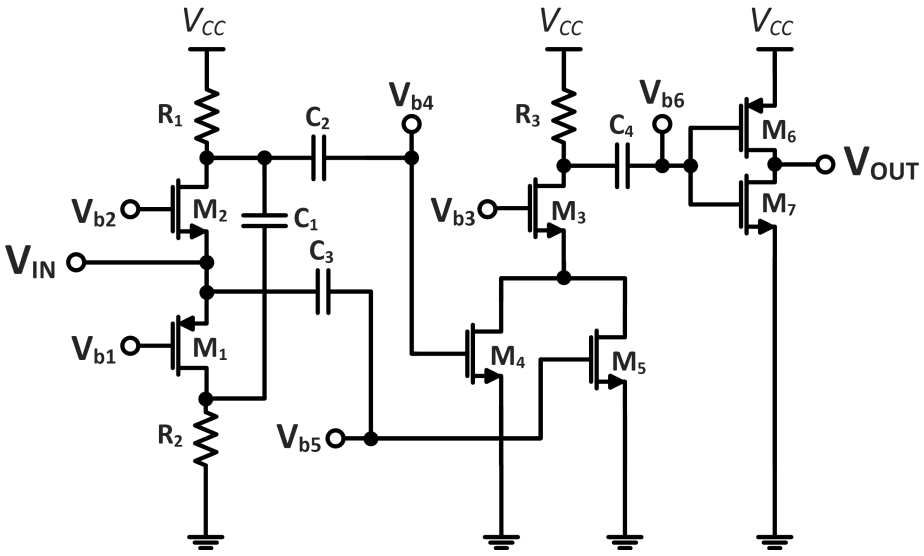
The local oscillators are generated from an off-chip oscillator that is fed into a programmable digital frequency divider. A digital phase splitter divides the output by two

and creates the in-phase and quadrature components of the first local oscillator. The in-phase component of the first local oscillator is divided by two and then fed into another digital phase splitter, further dividing it by two and creating the in-phase and quadrature components of the second local oscillator. Since the frequency ratio between the first and second oscillator is four, the digital frequency divider is programmed such that the first local oscillator is four-fifths the RF frequency of the desired WWV channel. Tying the local oscillators together provides two key benefits. One, frequency selection can be guaranteed through the tuning of only the first oscillator. Two, phase error between each local oscillator is substantially reduced. The second is particularly critical because any phase error between the each downconversion stage comes at the cost of worse image rejection.

2.3 RF Front End

The RF front end of the receiver, as shown in Fig. **??**, consists of a single-input preamplifier based on the modification of the design in[44]. As a WWV measurement device, it is important that this amplifier has a bandwidth wide enough to cover all five channels broadcast by WWV, which span just under a decade (three octaves). At the same time, the receiver must also be highly sensitive so that accurate measurements of WWV can be made across the entire United States, even during periods of poor propagation. In addition, the amplifier's gain must be large enough so that mixer noise in the next stage does not drown out weaker signals.

Normally, many low noise front end amplifiers rely on inductors in their design, however, the low frequencies of WWV channels made it desirable to avoid the use of any inductors. All these factors contributed in the decision to use a modified version of the



M	W/L (μm/nm)
M1	146.7 / 540
M2	58.68 / 540
M3	586.8 / 360
M4	586.8 / 360
M5	899.76 / 360
M6	400 / 360
M7	112 / 360
C	**pF**
C1	100
C2	20
C3	20
C4	20

Figure 2.3. CG-CS broadband noise-canceling LNA used in the RF front-end.

design used in[44], which utilized an inductorless, single input, combined common-gate (CG) and common-source (CS) architecture. The resulting circuit is a three stage amplifier (see Fig. 3) that includes i) a CG input stage (for input impedance matching); ii) a cascoded CS stage for amplification and broadband noise canceling; and iii) a high gain inverting stage for buffering and further amplification. The common gate input stage consists of a PMOS/NMOS pair that reuses the same DC bias current in order to save power. The outputs of each CG amplifier are recombined with a shunt capacitor (C1). The second stage consists a pair of common-source NMOS transistors cascoded together. The input of one NMOS is the output of the common-gate transistors from the first stage and the other is taken from the input of the first stage. This stage, amplifies the signals further and, through the summation of the two common-source NMOS, implements noise cancellation. The final stage is a basic inverting buffer used to add > 30 dB of gain in order to ensure small signals are amplified enough to overcome any noise from

the next mixing stage. As this design is a prototype, each transistor is externally biased through off chip bias voltages.

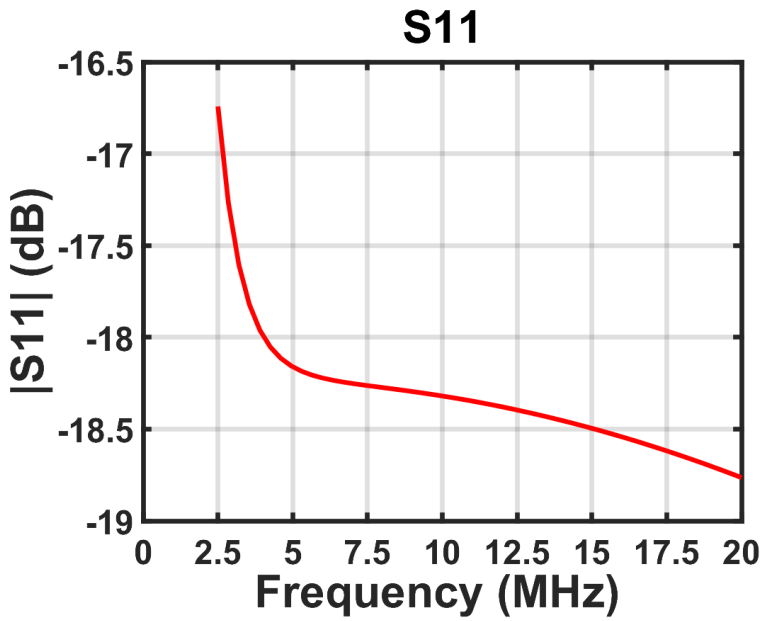


Figure 2.4. Simulated input reflection coefficient $|S_{11}|$ of the LNA.

The LNA is designed to match to a relatively high input impedance of 300 Ω which both helps reduce power consumption further in the CG stage and to minimize noise figure. Additionally, a source impedance of this value is easily obtained using either a dipole antenna with a step-up transformer, or a folded dipole antenna. Simulations show an approximate voltage gain of 140 (43 dB), Fig. 3.4. Simulated input reflection coefficient $|S_{11}|$ of the LNA is shown in Fig. 2.4. Fig. 3.6 shows that the input-referred noise PSD is < 2.25 nV/Hz$^{1/2}$ over all five WWV channels. In fact, it is < 0.69 nV/Hz$^{1/2}$ if we exclude the two low-frequency channels (2.5 MHz and 5 MHz), which are affected by $1/f$ noise, resulting in a NF < 0.4 dB for a 300 Ω source.

2.4 Passive Mixer and Operational Amplifier

The defining feature of a double quadrature downconverting Weaver receiver is its tradeoff of using more mixers in place of high-Q image reject filters. In the context of designing an integrated circuit, this tradeoff is well worth it; while mixers are easy to implement, high-Q, image rejection, bandpass filters are much more difficult to realize monolithically (particularly at the lower frequencies of WWV). At the same time, this tradeoff results in the greatest challenge in the design of a Weaver receiver; its need for a very high level of balance between mixer stages. This balance is necessary to ensure the image is cancelled properly when summed with its inverse in the final stage. Any phase or gain errors from the mixers creates a mismatch in the signal paths, including the image. Any mismatches between the images when they are summed back together leads to ineffective cancellation. The ultimate effect of this is a degradation of the image rejection ratio (IRR), minimizing the effectiveness of this architecture.

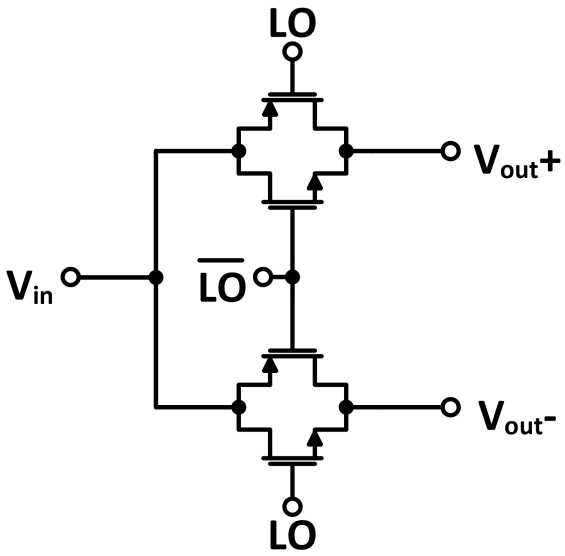


Figure 2.5. Single-balanced passive mixer used throughout the design

For this reason, a passive, single-balanced mixer topology was selected because of its relative simplicity. Each passive mixer, as seen in Fig. 2.5, consists of a pair of transmission gates, each created from an NMOS/PMOS pair which are driven by a local oscillator. In order to minimize mismatch between the transmission gates, common centroid layout is utilized. The resulting balanced outputs are then recombined with a basic operational amplifier setup as a differential amplifier. Besides the mixer's high level of linearity, the simplicity of the design makes it easier to ensure balance between all six mixer cells. In addition, this design utilizes a digital local oscillator which minimizes any mixer gain mismatches and ensures that any phase error is only a result of phase differences between each local oscillator (an error which itself is minimized through dependent local oscillator generation, discussed in section 2.6). Less concern is given to LO leakage since the downconverted IF and baseband signals are far enough from the LO frequency that the leakage can be easily filtered out.

The operational amplifier used to recombine the mixer outputs is the same design as all the non-front end amplifiers used in the entire design. In total it is used twelve times; once in each mixer cell (a total of six), twice as the summing and difference amplifiers in the final stage, twice more in each IF signal path (a total of four) serving to buffer and then amplify each IF signal. The amplifier design, seen in Fig. 2.6, is a basic two stage operational amplifier. The first stage consists of a standard, five transistor, PMOS input, differential pair. This feeds into a second, high gain, NMOS common-source amplifier with feedback through a 227 fF compensation capacitor. Bias for both stages is supplied by a series of current mirrors which, for the purposes of prototyping, are set off chip. Common centroid techniques were also utilized to minimize mismatch of the differential pair as well as to minimize mismatch in the current mirror. The simplicity

of the design makes it easy to use in all twelve blocks where it is needed. However, it also results in a relatively low gain bandwidth product (simulated at 50 MHz). Luckily, as all twelve uses of this amplifier are after the first downconversion stage, the necessary bandwidth of the amplifier falls below its actual bandwidth. With the highest WWV frequency band at 20 MHz, the highest IF will only be 4 MHz, well within the the amplifiers bandwidth. That being said, this does still limit the gain that can be achieved from a single amplifier in the IF signal path.

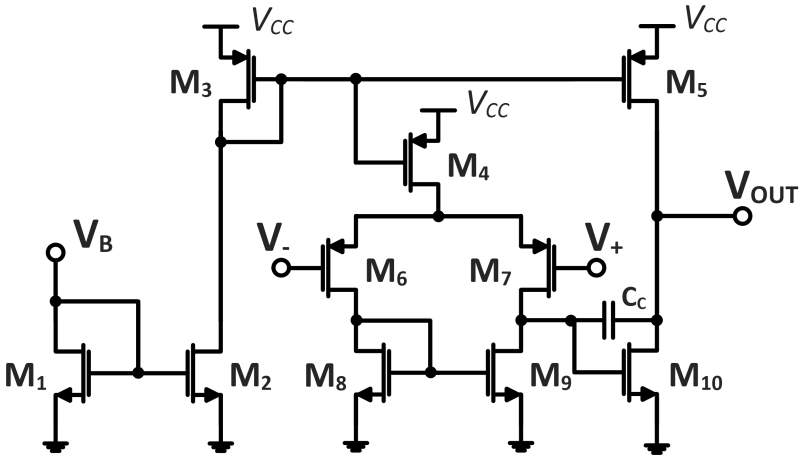


Figure 2.6. Operational amplifier used throughout the design

2.5 Low Pass Filter and OTA

Although the Weaver architecture eliminates the need for difficult to integrate, high-Q bandpass filters, it does not remove the need for filtering altogether. While the double downconversion process takes the place of image rejection filtering, the outputs of each mixing stage still create unwanted high frequency components. This is made up of a combination of unwanted mixing products, local oscillator leakage, input signal leakage, their harmonics and products of their harmonics. In the second mixing stage, this is a

much easier task as the baseband bandwidth is constant across all bands. Additionally, it is not necessary to filter out these signals before summation/differentiation, which serves as the final stage of the entire receiver. As a result, a basic passive off-chip filter is sufficient.

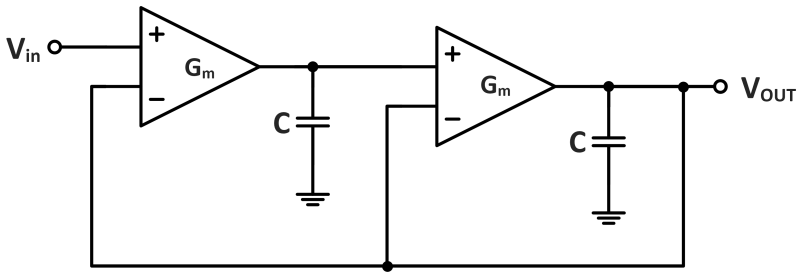


Figure 2.7. Second order G_m-C low pass filter (two are cascaded to create fourth order G_m-C filters)

The first mixing stage, on the other hand, runs into one of the problems specifically avoided by the superheterodyne architecture. Since this architecture's IF varies across each WWV band, the filter cutoff frequency must be tuned for each input band. In terms of on-chip, low pass filtering, there are three popular techniques; passive, switched capacitor, and G_m-C. In this design, a G_m-C topology was selected over passive or switched capacitor filters largely because of its combination of simplicity, small size, ease of realizing high-order filtering, and tunability. By cascading two second-order G_m-C filters, a fourth order LPF was easily realized in each signal path.

Each G_m-C stage consists of two simple operational transconductance amplifiers (OTA) with load capacitors C = 1 pF. The OTA, seen in Fig. 2.8, is an NMOS implementation of the first stage of the operational amplifier described in the previous section, consisting of an NMOS input differential amplifier stage with a high-impedance output. The high-impedance output of the transconductance amplifier acts in the same way as the resistor in a passive RC filter. One of the most useful aspects of this topology is that

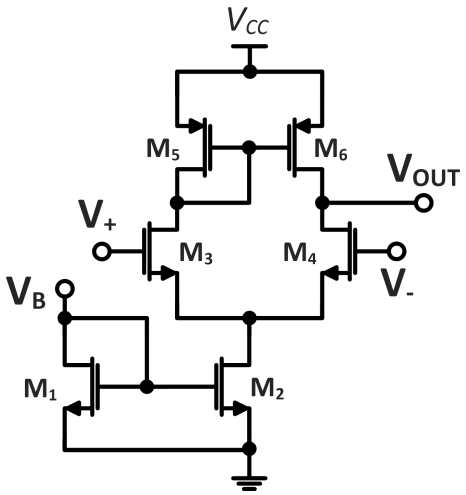


Figure 2.8. Basic operational transconductance amplifier with NMOS input transistors

tuning the bias current of each OTA adjusts the G_m of the OTA, setting the cutoff frequency of the G_m-C stage. A factor of ten change in the OTA's bias current results in approximately a factor of ten change in the cutoff frequency. If all the bias currents of each stage are tied together through current mirrors, the tuning of a single bias current can tune the entire filter. Assuming that the stages are identical, the -3 dB cutoff frequency of such a filter cascade is given by $f_c \approx (\sqrt{2^{1/2N} - 0.75} - 0.5)/(2\pi\tau)$, where N is the number of stages and $\tau = \tau_1 = \tau_2 = C/G_m$. In this case, $N = 2$, resulting in $f_c = 0.1628/(2\pi\tau)$.

2.6 Local Oscillator Generator Block

Historically, one of the most difficult aspects of realizing a Weaver receiver is the generation of local oscillators with low phase errors. This is critical because a mismatch in phase between I and Q signal paths results in poor cancellation of the image signals and

poor reinforcement of the message signals, which can significantly reduce the image rejection ratio. Previous literature[5,40] shows that generally a phase error of less than one percent is necessary for adequate image rejection.

While this may have been a difficult task with early analog signal processing techniques, modern digital synthesis makes it easy to derive both local oscillators and their quadrature components from a single source oscillator. Using a digital oscillator provides two key benefits; for one, a gated oscillator normalizes the oscillator amplitude, eliminating gain mismatch between the two local oscillators and their quadrature components; the other benefit is the high precision of phase splitting and frequency division possible with digital signal processing. To create a digital frequency divider the digital

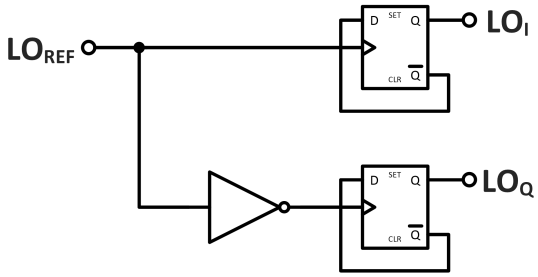


Figure 2.9. Digital phase splitter for generating I and Q components of both local oscillators

signal is fed directly into the clock input of a D flip-flop and the $\overline{Q}$ output is fed back into the D input. The resulting output at Q is exactly one half the frequency of the clock input. Using a similar approach, a digital phase splitter, as seen in Fig. 2.9, is created using two digital frequency dividers. One divider is fed by the digital signal, the other is fed by the inverse of that digital signal. The output of each are both one half the frequency of the input digital signal, but also 90° out of phase of each other.

In the case of this design, these techniques fit in extremely well. Starting with a source oscillator that is twice the frequency of the first local oscillator, a digital frequency

splitter divides the local oscillator by two, and the result is near perfect I and Q generation for the first LO. Further, the in-phase first LO signal is divided by two and put through another digital phase splitter (resulting in a net divide by four) which generates the I and Q of the second LO. The ultimate result is two phase- and frequency-locked LO signals.

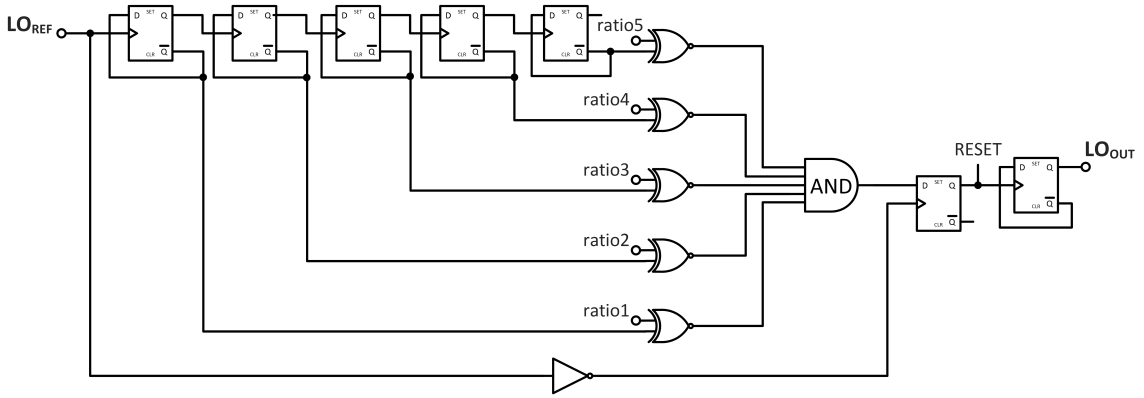


Figure 2.10. Programmable frequency divider

Modern direct digital synthesis integrated circuits create an easy method to generate a source oscillator at nearly any frequency, making this technique robust regardless of frequency. For the implementation of this WWV receiver, since the source oscillator frequency of all five bands share a common multiple of each other, a programmable frequency divider block is included such that a single external oscillator can be used to generator the source oscillator for all five channels. This divider is created using a five-bit programmable counter which works using a cascaded chain of five digital dividers whose $\overline{Q}$ outputs are also fed to one of the inputs of a corresponding XNOR gate. The chain of dividers create a five bit binary counter that counts up one by one for each clock cycle at the input. The second inputs of the five XNOR gates are controlled externally and the outputs of all five are tied together with an AND gate. When the bits in the

divider counter match up with the bits set externally, all the XNOR gates have the same output and the AND gate switches state, triggering a reset of the whole counter. In order to remove glitches resulting from differences in delay paths, a *D* flip-flop, clocked by the inverse of the input of the entire counter is used on the output of the AND. A final digital frequency divider is used one last time to ensure the duty cycle is actually 50 %, because the output of the previous flip-flop will not reliably be 50 %[45]. Since the programmable divider and *IQ* generator divide the oscillator by a minimum of four, an external local oscillator of 192 MHz, as it is the least common multiple required for each band.

2.7 Bias Current Mirror, I/O Buffers, and Variable Gain Resistive DAC

As this is a prototype, it is desirable to have externally tunable bias currents for as many individual blocks as possible. At the same time, it is critical that matched blocks between the *I* and *Q* signal paths have equivalent bias currents to help minimize any differences between the two branches. To accomplish this, a basic current mirror was designed that would mirror an external bias current into two branches. Each branch then supplies equivalent bias currents to the equivalent blocks in each of the *I* and *Q* signal paths. In total, nine current mirrors are used. Common centroid layout is also employed to ensure minimal mismatch between the three current branches in the mirror.

Additionally, thirteen test points are selected throughout the design to help aid with testing and the tuning of each external voltage and current bias. As any measurement equipment will load the test points, a set of 13 analog buffers, one for each test point, is included. These analog buffers are made from the design of the operational amplifier described in section 2.3.

In addition to analog buffers, it is also desirable to include test points for the local oscillators. For these test points a set of digital dividers is incorporated. Each digital buffer is constructed from a chain of four inverters whose size increases by a factor of three with each successive inverter (making a ratio of $1x$ $3x$ $9x$ $27x$ relative to the first inverter). This makes sure each previous inverter has enough drive capability for the next inverter, with the last having enough to drive a measurement probe. Besides being used to buffer the local oscillators, these digital buffers are also used to buffer the 18 different digital inputs. Six of these inputs are used to control the digital frequency divider block (five to program the divide ratio, one to toggle between bypassing the divider itself). The other 12 inputs are used to control IF gain in each branch. Two of these inputs sets the rough gain of both I and Q paths (selectable between gains of 2, 10, and 20). The other 10 are split in half for independent, fine adjustment of the gain in each branch. The IF gain block itself is created from the already described operational amplifier setup as a non-inverting amplifier with two resistors forming the feedback loop. The coarse gain adjustment sets the resistance in the top half of the loop of both amplifiers with a 2 bit resistive DAC. The fine adjustment sets the resistance in the bottom half of the loop of each amplifier individually with a 5 bit resistive DAC.

2.8 Layout

As with all RF designs, good layout techniques are important for achieving performance that agrees with expectations. Neglecting proper layout can result in signal leakages and mismatches that deteriorate and distort signal quality. This design utilizes several layout techniques in order to optimize performance.

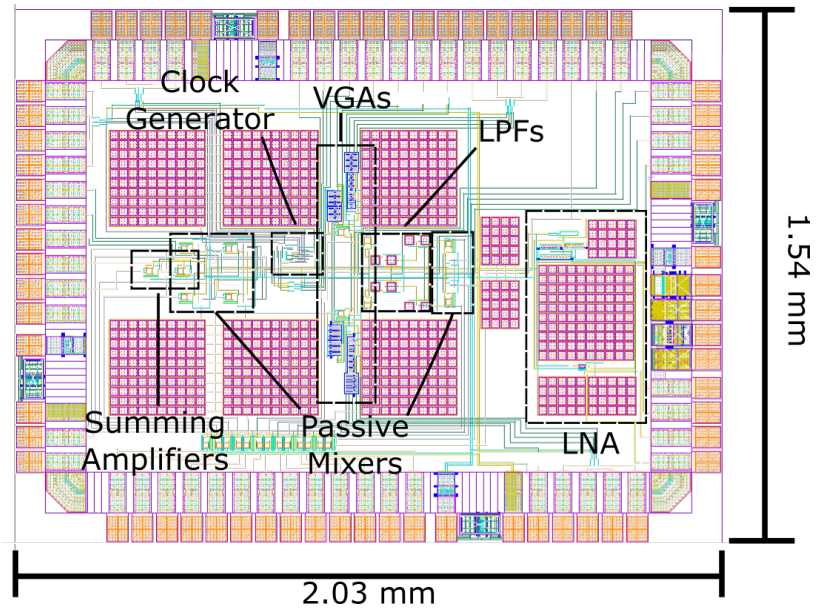


Figure 2.11. Full layout of receiver

First, all differential pairs and current mirrors were laid out using a common-centroid layout. Both differential pairs and current mirrors need their transistor pairs or chains to be as closely matched as possible in order to minimize differential errors between them. By laying out the pairs and chains such that the transistors have two axes of symmetry with each other, common-centroid layout greatly improves these circuits' resilience to any deposition gradient errors, as any errors will equally affect both (or all) transistors. Second, guard rings are used around every transistor to reduce coupled noise through the substrate. For NMOS transistors, an NMOS guard ring tied to ground is used; for PMOS transistors, a PMOS ring is tied to power. In the case of NMOS transistors whose sources were not tied to ground, deep N-wells are used to keep V_{bs} equal to zero thus keeping the V_{th} consistent.

In addition, in general, transistor lengths are kept to a minimum and gate fingering is used so that W/L can be maximized. Gate fingers and gate to gate connections are

made with metal interconnects instead of poly to reduce loss and mismatch. Care is also taken in general to minimize resistance in signal paths between circuit blocks by minimizing metal wire lengths and increasing widths as needed. Multiple vias are also used as needed between metal layers additionally to minimize resistance. Centralized power and ground planes are also utilized to minimize coupled noise.

For the use of passive components, high capacity metal-insulator-metal (MIM) capacitors are used which have a typical capacitance density of 2 fF/μm^2. In the case of resistors, high resistance poly resistors are used with a typical resistance density of 17.75 Ω/μm at minimum feature size width (0.42 μm). Fig. 2.11 shows the complete layout of the receiver, which occupies a total area of 2.03 mm x 1.54 mm.

3 Measurement Results

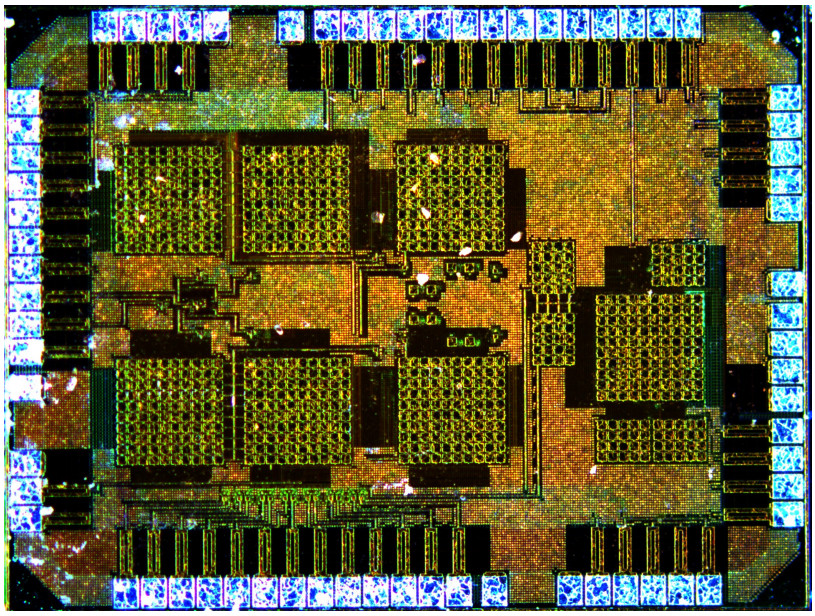


Figure 3.1. Die photograph of the fabricated receiver

3.1 Testing Setup

The chip was fabricated using the TSMC 0.18 um CMOS process through Muse Semiconductor and packaged in an 80-pin QFN by Quik-Pak. As seen in Fig. 3.1, the entire receiver occupies an area of 2.03 mm x 1.54 mm. While an 80-pin package is used for the prototype, a final version of this chip could include just one input pin, two output

pins, power and ground pins, an external local oscillator input pin, and five digital select pins for channel selection, requiring eleven total pins. In addition, pins for gain control may be added as well depending on the finalized design. In the case of this design, many additional pins are included for the purposes of testing and troubleshooting. These include: 12 pins used for adjusting the I and Q signal paths' gain, a common-mode voltage reference pin, 13 pins for setting current and voltage biases of various circuit blocks, 13 pins for analog test points located throughout the circuit, four digital test points for the I and Q signals of both local oscillators, an extra external local oscillator input that bypasses the internal digital divider, and an extra digital select pin to toggle between two external local oscillator inputs. In total, 56 out of 80 available pins in the QFN package were utilized.

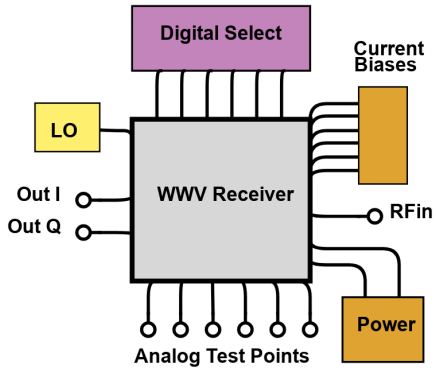
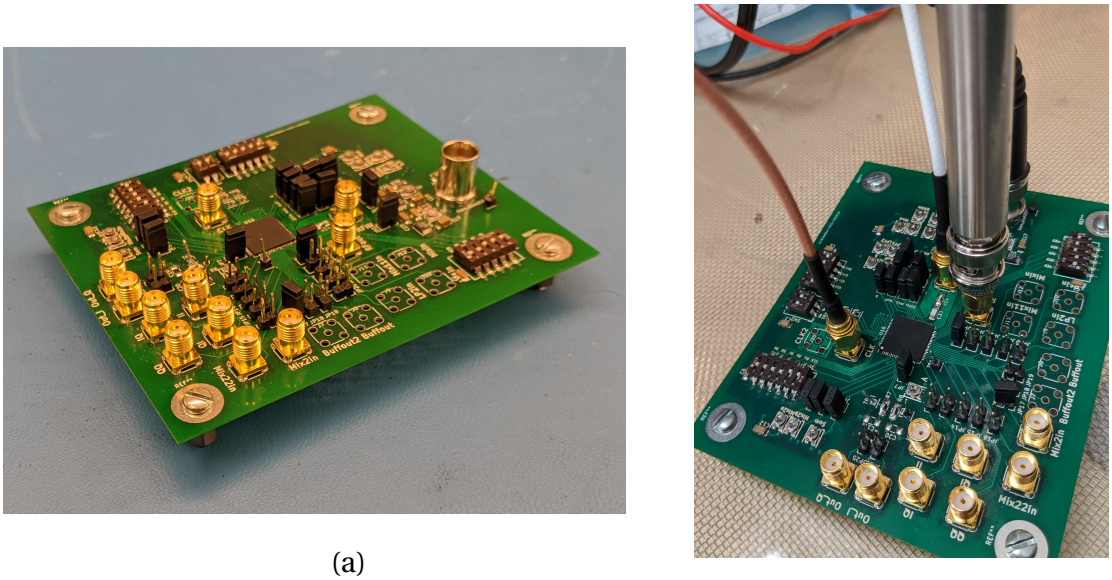


Figure 3.2. Simplified block diagram of the receiver test board.

As seen in Fig. 3.3, a printed circuit board (PCB) was designed with all the necessary off-chip components in order to test the chip. Five volt power is supplied to the board from a benchtop power supply and fed through a BNC connector on the board. The off board supply, powers two LT3042 linear regulators, one of which supplies the

chip with power and the other which powers the common-mode reference pin (approximately half the chip power voltage level). Each regulator is tunable by a 1 kΩ trimmer resistor. Dip switches connected to pull up resistors are used as digital selects and connected directly to these pins. Voltage and current biases are created with tunable voltage dividers and connected to the chip through a two position header enabling each bias to be easily connected or disconnected. Each analog test point is also connected to an SMA connector through a two position header such that the SMAs at each test point can be connected or disconnected. In addition, there is space left within the output signal path for a first order RC LPF in order to define final bandwidth.



(a) (b)

Figure 3.3. (a) Printed circuit board testing platform used for chip testing in (b).

For the purpose of characterizing the receiver, several pieces of off board test equipment were utilized. An Agilent E4430B RF signal generator outputting a 1.6 dBm (1.5 V pk-pk) sine wave and passed through a 0.75 V DC bias is used to create the 192 MHz external local oscillator. The external local oscillator input is buffered by an inverter chain

that amplifies the signal to the point of it oscillating rail to rail providing the correct digital input voltage levels. An Agilent N5181A RF signal generator is used to create a double side band amplitude modulated (DSB-AM) signal with a single 400 Hz message tone to imitate WWV as an input source. An Agilent 4395a network analyzer is used in both spectrum analysis mode and network analysis mode in order to measure the receiver outputs and test points as well as the LNA output respectively. All three pieces of test equipment are also fed by a 10 MHz external reference oscillator generated by a GPS stabilized digital oscillator to improve frequency precision.

3.2 LNA Measurements

The entire WWV receiver can be separated into two distinct operational parts; the analog front end (AFE) low-noise amplifier (LNA) and the double quadrature downconverter. This section will discuss the measurement results of the LNA.

As has been discussed in previous sections, the focus for this analog front end amplifier is low noise and high dynamic range while maintaining considerable gain across all five WWV channels in order to maximize its measurement sensitivity and range. By adjusting bias voltages supplied to the various stages of the LNA, significant adjustment of the gain, bandwidth and noise sensitivity of the amplifier is achieved. The bias voltages are balanced such that gain is greater than 40 dB, noise figure is less than 3 dB, and the total chip consumes less than 25 mW.

Cadence simulations, performed with a simulated 300 Ω impedance source, demonstrated a wideband gain of about 43 dB across all channels. The bandwidth is approximately 1 MHz-100 MHz. As seen in Fig. 3.4, the measured results using the Agilent 4395a network analyzer show a voltage gain of about 35 dB across all bands and are in

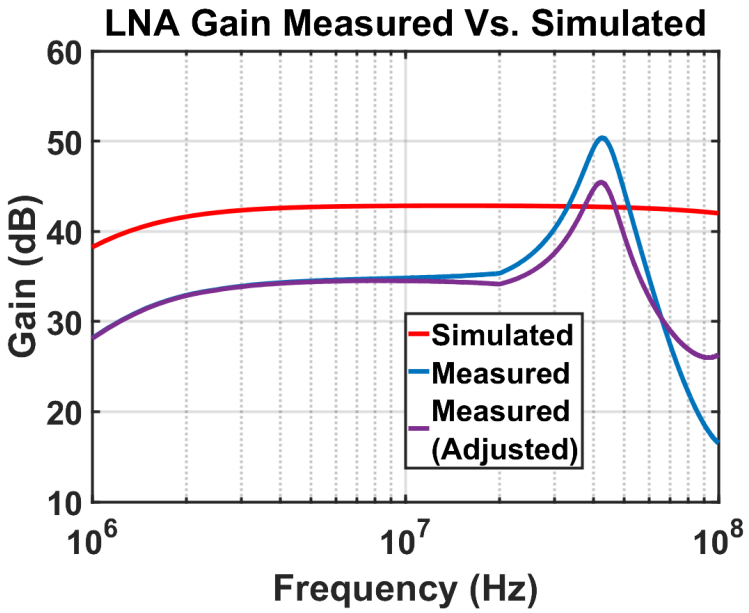


Figure 3.4. Simulated and measured gain of the front end low noise amplifier. Measured gain adjusted for the simulated effects of the analog buffer stage is included as well.

reasonable agreement with the simulations. The measured bandwidth does show a large peak at around 40 MHz and a cutoff frequency around 50 MHz which is in conflict with Cadence simulations. This disagreement is almost definitely a result of the unity gain buffer amplifiers used at each analog test point on the chip. The simulated bandwidth of the unity gain buffer is only around 50 MHz. The measured transfer function, adjusted by the simulated transfer function of buffer amplifier, can be seen in Fig. 3.4 and shows closer agreement to simulated results.

The 1-dB compression point was measured at each channel and shows a worst case compression point of about −38 dBm. As seen in Fig. 3.5, the measured results performed better than expected from the simulations, though this is mostly a result of the lower than expected gain. At better than −38 dBm, this amplifier has maximum input signal of at least 8 mV peak to peak. Although this is somewhat small when compared

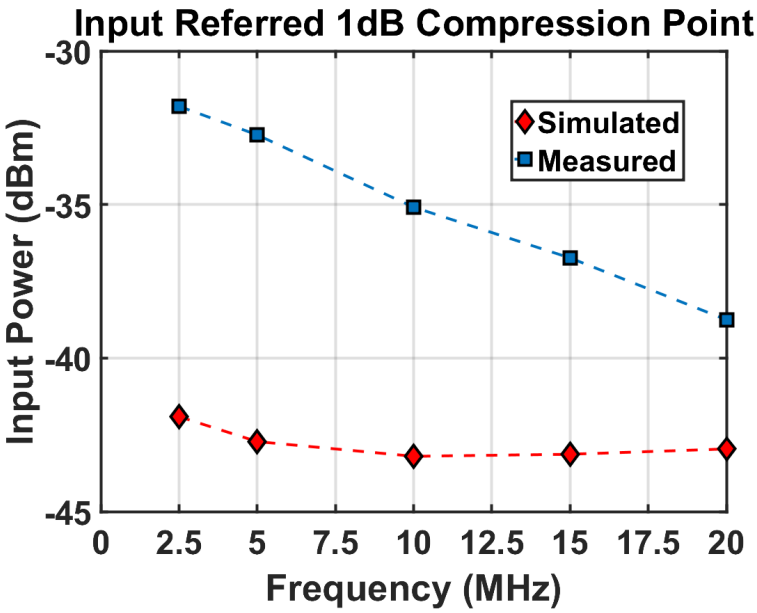


Figure 3.5. Simulated and measured input referred 1dB compression point.

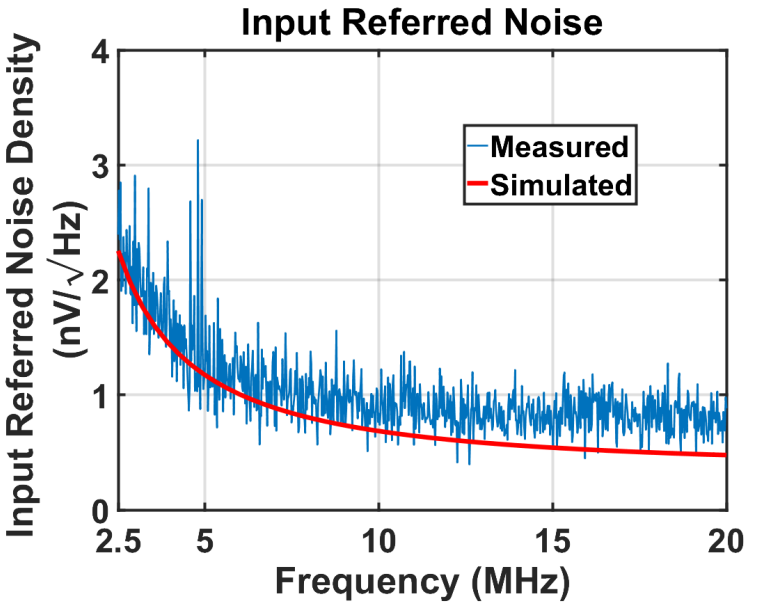


Figure 3.6. Simulated and measured input referred noise of the LNA.

with other analog front ends, for this application, it is more than sufficient as WWV's broadcast strength is at most 10 kW. Radio signal reception of greater than −50 dBm at any reasonable distance from the WWV's source is unlikely.

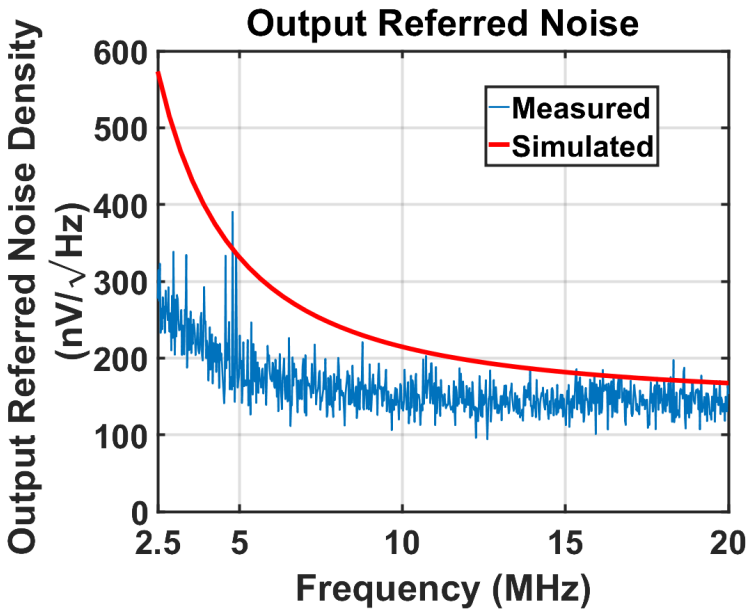


Figure 3.7. Simulated and measured output referred noise of the LNA.

Table 3.1. Measured noise figure

Frequency	**2.5 MHz**	**5 MHz**	**10 MHz**	**15 MHz**	**20 MHz**
NF	2.88 dB	1.45 dB	0.61 dB	0.63 dB	0.44 dB

Finally, Fig. 3.6 shows the measured input referred noise of the amplifier, which is better than < 2.25 nV/Hz$^{1/2}$ across all five WWV channels. These results match incredibly well with the simulated results. In fact, it is better than < 1 nV/Hz$^{1/2}$ if we exclude the two low-frequency channels (2.5 MHz and 5 MHz), which are affected by $1/f$ noise. When connected to a 300 Ω source, the resulting noise figure is better than 2.9 dB for the two low-frequency channels and better than 0.6 dB for the three high-frequency channels. Furthermore, assuming a defined final bandwidth of 10 kHz, the minimum detectable signal is approximately 225 nV at low-frequencies, and drops as low as 63 nV ($-128dBm$-$-140dBm$). As a result, the dynamic range of the LNA is between 90-100 dB across all channels, significantly high for this application.

3.3 Full Receiver Measurements

The total quiescent power of the receiver is measured to be 24.875 mW, most of which is consumed by the LNA (65 %), mixers, and VGAs. This agrees nearly perfectly with the simulated power consumption of 24.9 mW. As has been touched on in previous sections, in order to test the full signal chain of the receiver, a simulated version of each WWV channel and its respective image signal is generated. An Agilent N5181A RF signal generator is used to create a double side band full carrier (DSB-FC) signal with a single 400 Hz message tone at 100 % percent modulation depth which is used to imitate both the five channels of WWV as well as their corresponding image signals. The single tone makes it easier to analyze gain and image rejection at each channel. An input power of −90 dBm was selected around the center of the receiver's dynamic range.

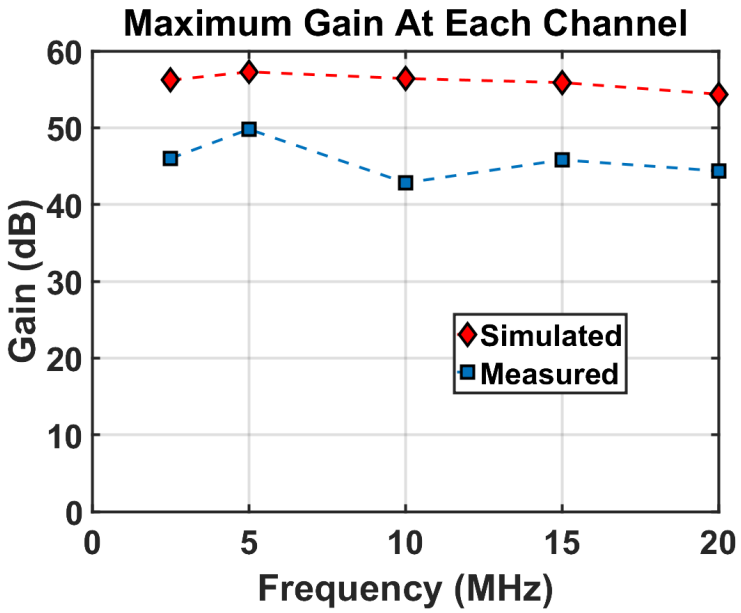


Figure 3.8. Simulated and measured maximum voltage gain for each channel.

Unfortunately, initial testing immediately revealed an error with the design. At its outputs, the receiver amplifies the image signal at each band, and rejects the band itself.

Table 3.2. Simulated power consumption summary.

Section	Power (mW)
LNA	16.16
Mixers	3.70
VGAs	2.46
Bias currents	1.29
Summing amplifiers	1.23
LPFs	0.05
Total	**24.89**

This is the exact opposite of the intended function of the receiver. Looking into this, it was realized that the final stage of the receiver, the summing and differencing amplifiers used to recombine each half of the signal chain were reversed. Whereas the II and QQ signals were supposed to be fed through the differential amplifier and the IQ and QI signals were supposed to be fed through the summing amplifiers, these were accidentally reversed. As a result, the image sum together and the intended message signals cancel each other out.

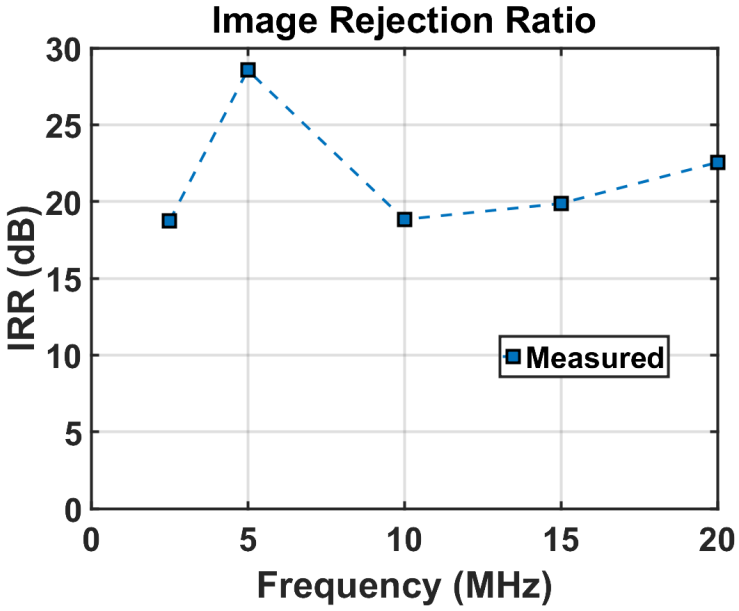


Figure 3.9. Measured IRR of the receiver across the WWV channels.

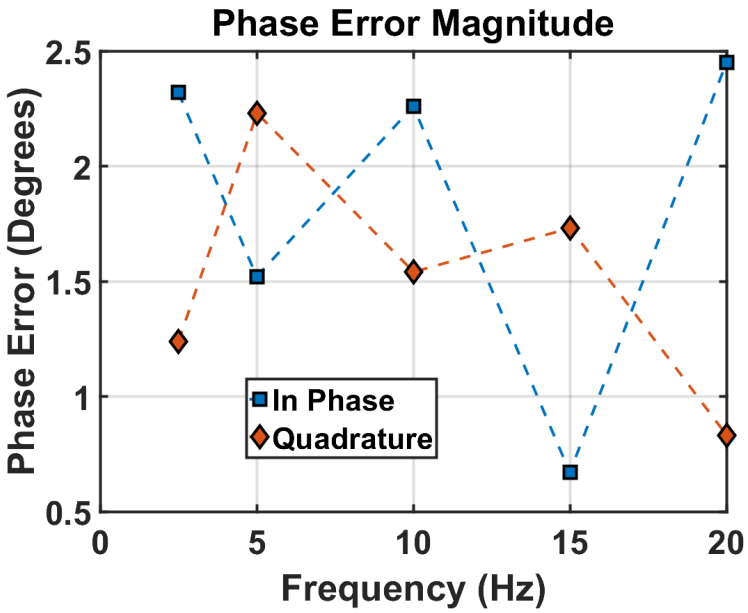


Figure 3.10. Measured average phase error between the baseband image signal paths for in-phase and quadrature outputs.

Fortunately, analog test points at the outputs of each of the four mixers in the second mixing stage enables data collection right before the final summing and differencing stage. As a result, the loss of the last stage of the receiver is actually not critical. These four baseband signals can easily be recombined with off-chip summing and differencing amplifiers if so desired, or simply fed into a low-speed analog to digital converter (ADC) and processed digitally. Even better, in this case, only the output magnitude is required of each signal; there is no information in the message signal that needs to be recovered. Therefore, by measuring the output gain of each mixer and measuring the phase angle between the II and QQ outputs and the IQ and QI outputs, the baseband signals can be recorded, and then summed and differenced digitally using Matlab.

Fig. 3.8 shows the measured maximum small-signal gain across all five channels, which ranges from 43 to 50 dB and in good agreement with simulations. These results

are comparable to the receivers outlined in Ref.[40] Ref.[5] Ref.[41], seen in Table 3.3. Considering a strong signal ("S9") as defined as −73 dBm by the International Amateur Radio Union (IARU) region 1, gain of only additional 20-30 dB is necessary in order to achieve consumer line output levels (3 dBm). A weak signal ("S1" defined as −121 dBm by the IARU) would still see output levels greater than −80 dBm. At the same time, as seen in Fig. 3.9, the image rejection ratio varies from 19-29 dB across all bands without any calibration scheme. Similar to gain, this range of image rejection ratios are comparable with the radio receivers in Ref.[40] Ref.[5] Ref.[41]. Finally, critical in maximizing image rejection, as seen in Fig. 3.10, image-signal differential phase error is reduced to $< 2.5\,^{\circ}$ across all channels.

Table 3.3. Comparison of Quadrature Image-Reject Receivers

Parameter	**Ref.[40]**	**Ref.[5]**	**Ref.[41]**	**This work**
Technology	0.7 μm	0.25 μm	0.35 μm	0.18 μm
RF band	900 MHz	2 GHz	1.8 GHz	2.5 - 20 MHz
Power	500 mW	50 mW	95 mW	25 mW
Noise figure	24 dB	5.2 dB	-	2.9 - 0.44 dB
Input P_{1dB}	-	-30 dBm	-15 dBm	-32 - -39 dB
Gain	9.2 dB	41 dB	-	42.8 - 49.8 dB
IRR (w/o) calibration	17 dB	25 dB	26 dB	18.7 - 28.6 dB

4 Conclusions

This thesis has demonstrated the design, fabrication, and measurement of a fully-integrated double-quadrature down-converting HF Weaver receiver for monitoring the NIST time and frequency reference radio station WWV across multiple channels in the 2.5-20 MHz range. The chip has been fabricated on the TSMC 180 nm CMOS process and measures 2.03 mm x 1.54 mm.

The design consists of relatively simple analog building blocks: a low noise amplifier, mixers, low pass filters, amplifiers (including the summing amplifiers), and a clock generator. Tests of the front end low noise amplifier, a modified version of the amplifier presented in Ref.[44], show it achieves gain of greater than 35 dB and an excellent noise figure of less than 2.9 dB across all channels. The full receiver demonstrates a total gain of greater than 43 dB and image rejection ratios between 19-29 dB across all channels. Power consumption is less than 25 mW, very low compared to earlier work (see Table 3.3), albeit in a lower operating frequency range. The sensitivity of the receiver is better than -128 dBm and has a dynamic range of greater than 90 dB without any inductors or large band-pass filter and with no calibration scheme. The down-converted vector outputs can be digitized by low-sampling-rate ADCs, thus reducing the power consumption of later SDR-based signal processing. Unfortunately, as was discussed,

an error in the design swapped the inputs to the final stage summing and differencing amplifiers. The intended message signal was therefore rejected while the image was amplified. As a result, measurement data for the full receiver had to be taken at the outputs of the second mixing stage and recombined digitally using Matlab.

4.1 Future Work

As the ultimate purpose of this device is to be used as a WWV monitoring instrument, future work would aim to improve the receiver's gain, image rejection ratio, and linearity. Though the receiver's gain is already relatively high, a final version of this measurement device would have a final gain stage to condition the output to efficient levels for whatever listening or recording device is being used. The image rejection ratio would be maximized to minimize any interference and is almost entirely dependant on minimizing phase and gain error between recombined baseband signals.

Aside from the obvious first step of fixing the final stage of the receiver, several changes and improvements can be made to the design. For one, the IF variable gain amplification stage can be replaced with an automatic gain control (AGC) system. The original thinking was that, as a measurement device, gain information should be retained. However, an AGC that outputs its gain value would be just as effective and would enable gain calibration between signal paths. As demonstrated in Ref.[40] Ref.[5] Ref.[41], it is believed that IRR can be improved to > 60 dB. Another improvement that should be considered is replacing the passive mixers with active, double balanced Gilbert cells. With tuning, Gilbert mixers can improve gain matching between signal paths and help reduce signal leakage. The front end LNA also can be improved on in design. This is especially true for

the final stage of the amplifier which could have a feedback loop to help stabilize its output instead of using an externally adjustable bias. Power consumption of the block could also be greatly reduced as a result of this feedback in the final stage. Further power could be saved by increasing the input impedance (An input impedance of 1 kΩ would still be appropriate at these frequencies). Additionally, the layout can be improved to help better match signal paths, reduce conduction loss, and reduce ground noise. Signal paths of the local oscillator can also be improved to help reduce phase errors. Finally, matching between blocks can be improved so that coupling capacitors become unnecessary. Currently, these capacitors take up the largest portion of space on the chip. Removing them would free up space which would both significantly aid layout routing as well as save money on fabrication costs due to reduced die size.

Appendix A
PCB for receiver testing

. This appendix presents the schematic and layout of the PCB board used to test the receiver IC.

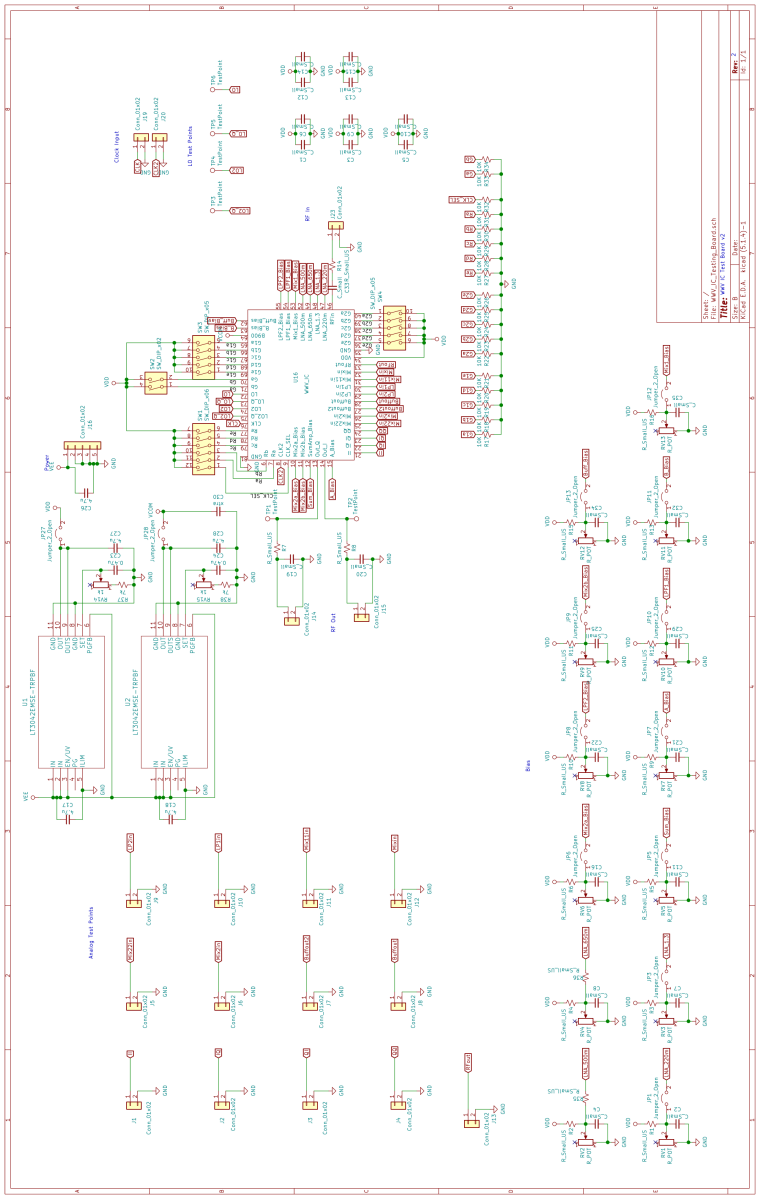


Figure A.1. Schematic of the PCB.

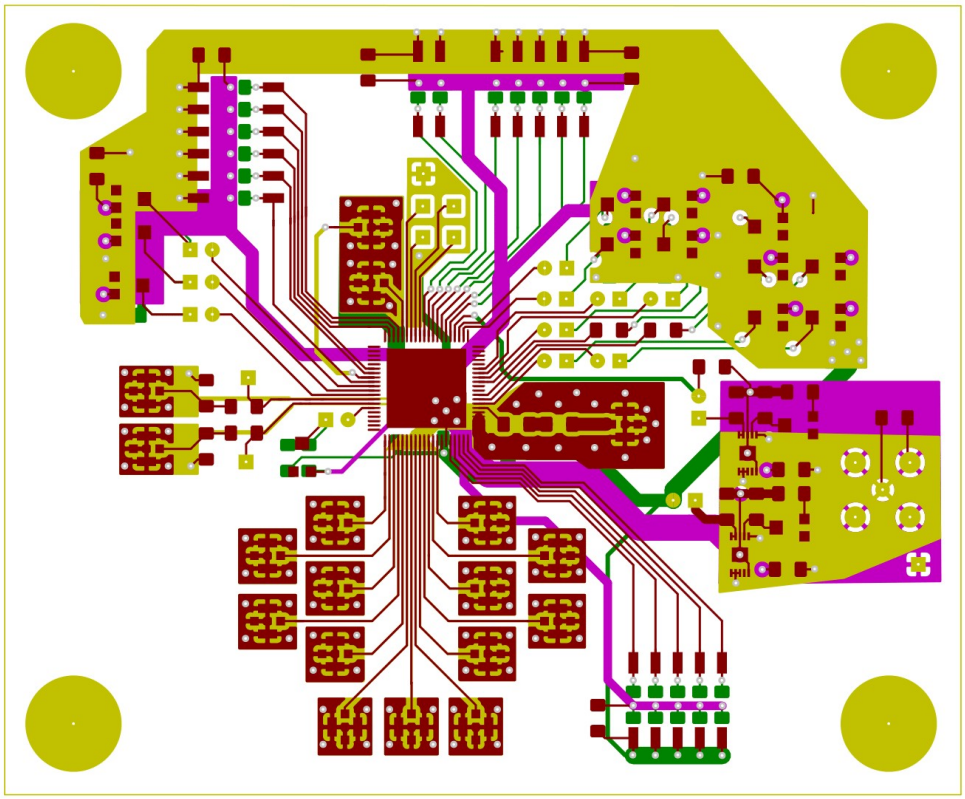


Figure A.2. Layout of the PCB

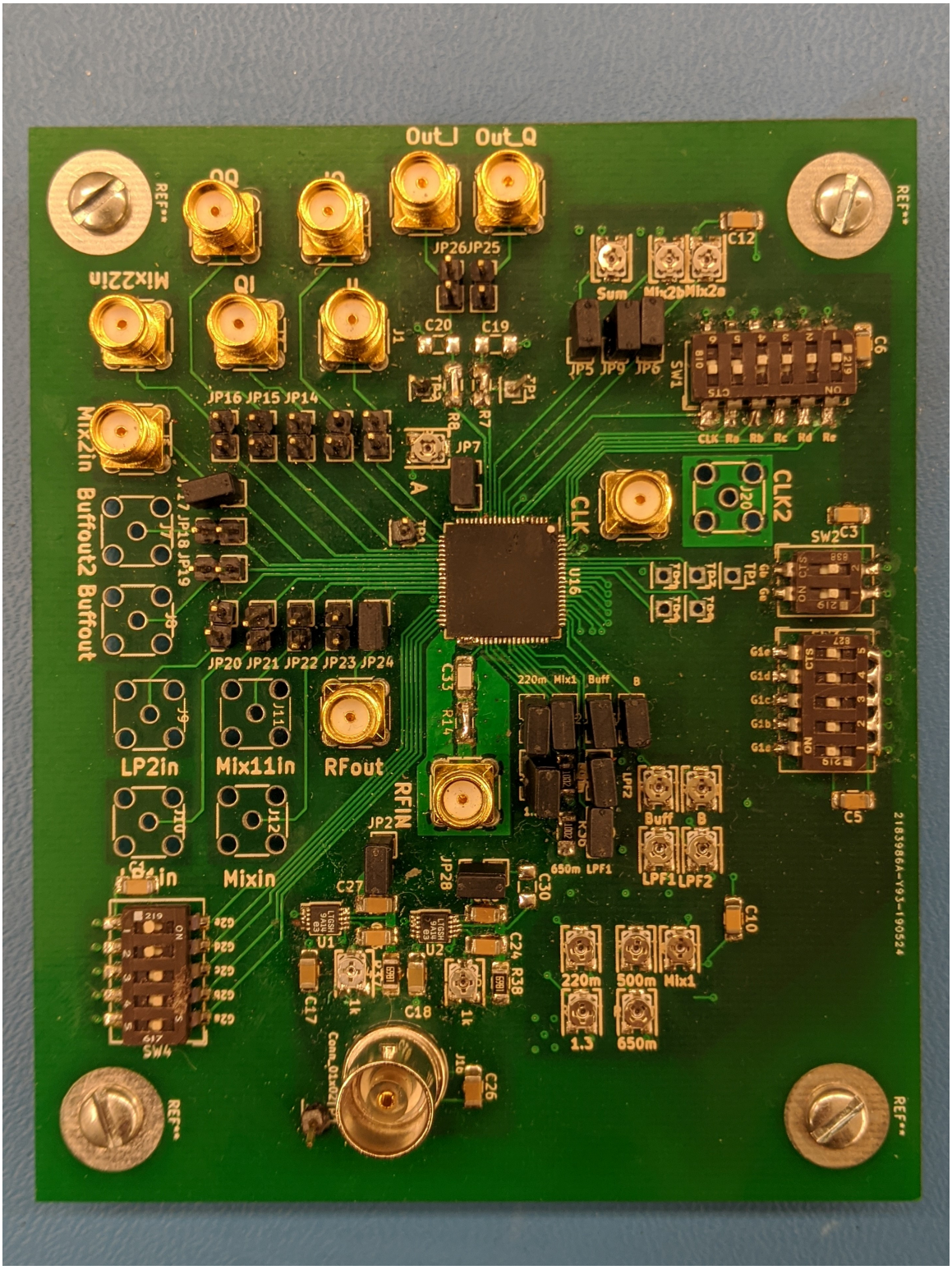


Figure A.3. Picture of the assembled testing board

Complete References

[1] Anthea J Coster, Larisa Goncharenko, Shun-Rong Zhang, Philip J Erickson, William Rideout, and Juha Vierinen. Gnss observations of ionospheric variations during the 21 august 2017 solar eclipse. Geophysical Research Letters, 44(24):12–041, 2017.

[2] NA Frissell, JD Katz, SW Gunning, JS Vega, AJ Gerrard, GD Earle, ML Moses, ML West, JD Huba, PJ Erickson, et al. Modeling amateur radio soundings of the ionospheric response to the 2017 Great American Eclipse. Geophysical Research Letters, 45(10):4665–4674, 2018.

[3] RTL-SDR. Rtl-sdr blog v3 datasheet, 2019.

[4] Farbod Behbahani, John C Leete, Yoji Kishigami, Andreas Roithmeier, Koichi Hoshino, and Asad A Abidi. A 2.4-GHz low-IF receiver for wideband WLAN in 0.6-μm CMOS-architecture and front-end. IEEE Journal of Solid-State Circuits, 35(12):1908–1916, 2000.

[5] Lawrence Der and Behzad Razavi. A 2-GHz CMOS image-reject receiver with LMS calibration. IEEE Journal of Solid-State Circuits, 38(2):167–175, 2003.

[6] Weidong He, Xiaochun Lu, Chengyan He, and Torley James. An anti-image interference quadrature IF architecture for satellite receivers. Chinese Journal of Aeronautics, 27(4):955–963, 2014.

[7] Glenn K Nelson. A century of wwv. Journal of Research of the National Institute of Standards and Technology, 124:1–31, 2019.

[8] Edward V Appleton and MAF Barnett. Local reflection of wireless waves from the upper atmosphere. Nature, 115(2888):333, 1925.

[9] Edward Victor Appleton and MAF Barnett. On some direct evidence for downward atmospheric reflection of electric rays. Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character, 109(752):621–641, 1925.

[10] Gregory Breit and Merle A Tuve. A test of the existence of the conducting layer. Physical Review, 28(3):554, 1926.

[11] Gregory Breit and Merle A Tuve. A radio method of estimating the height of the conducting layer. Nature, 116(2914):357, 1925.

[12] BE Blair and AH Morgan. Control of wwv and wwvh standard frequency broadcasts by vlf and lf signals. Radio Sci. J. Res NBS D, 69:915–928, 1965.

[13] Glenn K Nelson, Michael A Lombardi, and Dean T Okayama. Nist time and frequency radio stations: Wwv, wwvh, and wwvb. NIST Special Publication, 250(67):161, 2005.

[14] JV Eccles, RD Hunsucker, D Rice, and Jan Josef Sojka. Space weather effects on mid-latitude HF propagation paths: Observations and a data-driven D region model. Space Weather, 3(1):1–15, 2005.

[15] J. F. Helmboldt, T. E. Clarke, J. Craig, J. D. Dowell, S. W. Ellingson, J. M. Hartman, B. C. Hicks, N. E. Kassim, G. B. Taylor, and C. N. Wolfe. Passive all-sky imaging radar in the HF regime with WWV and the first station of the long wavelength array. Radio Science, 48(5):491–512, 2013.

[16] JM Watts and K Davies. Rapid frequency analysis of fading radio signals. Journal of Geophysical Research, 65(8):2295–2301, 1960.

[17] Richard C Fenwick and Oswald G Villard Jr. Continuous recordings of the frequency variation of the WWV-20 signal after propagation over a 4000-km path. Journal of Geophysical Research, 65(10):3249–3260, 1960.

[18] Kenneth Davies and Donald M Baker. On frequency variations of ionospherically propagated HF radio signals. Radio Science, 1(5):545–556, 1966.

[19] K Toman. Ionospheric phase-and group-path. Journal of Atmospheric and Terrestrial Physics, 29(8):1019–1023, 1967.

[20] Leo F McNamara, Richard J Barton, and Terence W Bullett. Analysis of hf signal power observations on two north american circuits. Radio science, 41(05):1–17, 2006.

[21] RD Sears. Ionospheric HF doppler dispersion during the eclipse of 7 March 1970 and TID analysis. Journal of Atmospheric and Terrestrial Physics, 34(4):727–732, 1972.

[22] Nathaniel A Frissell, Joshua S Vega, Evan Markowitz, Andrew J Gerrard, William D Engelke, Philip J Erickson, Ethan S Miller, R Carl Luetzelschwab, and Jacob Bortnik. High-frequency communications response to solar activity in september 2017 as observed by amateur radio networks. Space Weather, 17(1):118–132, 2019.

[23] José Raúl Machado-Fernández. Software defined radio: Basic principles and applications. Facultad de Ingeniería, 24(38):79–96, 2015.

[24] Rami Akeela and Behnam Dezfouli. Software-defined radios: Architecture, state-of-the-art, and challenges. Computer Communications, 128:106–125, 2018.

[25] Thangadurai N Chetna Devi Kh. A review on recent trends in software defined radio design and applications. International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), 6(10):21–25, 2017.

[26] SDRplay. Sdrplay general specifications, 2019.

[27] Airspy.com. Airspy hf+ discovery, 2019.

[28] John Seamons. Kiwisdr design review, February 2016.

[29] RTL-SDR.com. Measuring the usb power consumption of various software defined radios, October 2019.

[30] Inc Rafael Microelectronics. R820t high performance low power advanced digital tv silicon tuner datasheet, 2011.

[31] RTL-SDR. A review of the kiwisdr: 10 khz - 30 mhz wideband network sdr, June 2017.

[32] SDRplay. Rsp1a, 2019.

[33] Airspy.us. Airspy hf discovery sdr, 2019.

[34] Jacques C Rudell, J-J Ou, Thomas Byunghak Cho, George Chien, Francesco Brianti, Jeffrey A Weldon, and Paul R Gray. A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications. IEEE Journal of Solid-State Circuits, 32(12):2071–2088, 1997.

[35] Behzad Razavi. RF microelectronics. Prentice Hall, NJ, 2 edition, 1998.

[36] Ralph VL Hartley. Modulation system, April 17 1928. US Patent 1,666,206.

[37] Donald K Weaver. A third method of generation and detection of single-sideband signals. Proceedings of the IRE, 44(12):1703–1705, 1956.

[38] Jan Crols and Michel SJ Steyaert. A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology. IEEE Journal of Solid-State Circuits, 30(12):1483–1492, 1995.

[39] Shahrzad Tadjpour, Ellie Cijvat, Emad Hegazi, and Asad A Abidi. A 900-mhz dual-conversion low-if gsm receiver in 0.35-/spl mu/m cmos. IEEE Journal of solid-state circuits, 36(12):1992–2002, 2001.

[40] Raymond Montemayor and Behzad Razavi. A self-calibrating 900-MHz CMOS image-reject receiver. In European Solid-State Circuits Conference (ESSCIRC), pages 320–323. IEEE, 2000.

[41] Mostafa AI Elmala and Sherif HK Embabi. Calibration of phase and gain mismatches in Weaver image-reject receiver. IEEE Journal of Solid-State Circuits, 39(2):283–289, 2004.

[42] Mostafa AI Elmala and Ghada H Ibrahim. Calibration study of dual-band Weaver–Hartley receiver architecture. Microelectronics Journal, 46(6):439–446, 2015.

[43] Ali Nikoofard, Siavash Kananian, and Ali Fotowat-Ahmady. A fully analog calibration technique for phase and gain mismatches in image-reject receivers. AEU-International Journal of Electronics and Communications, 69(5):823–835, 2015.

[44] Wei-Hung Chen and Ali Niknejad. Designs of Broadband Highly Linear CMOS LNAs for Multiradio Multimode Applications. PhD thesis, University of California, Berkeley, 2009.

[45] Jifu Liang, Yingying Wang, and Soumyajit Mandal. A switched-capacitor-based low-power receiver for electrocardiogram and respiration rate detection. Analog Integrated Circuits and Signal Processing, pages 1–10, 2018.