A 1.2 V Current-Mode RMS-to-DC Converter Based on a Novel Two-Quadrant Electronically Simulated MOS Translinear loop

Maite Martincorena Arraiza, *Student Member, IEEE,* Carlos A. De La Cruz Blas, *Member, IEEE,* José María Algueta Miguel, and Antonio Lopez-Martin, *Senior Member, IEEE*

***Abstract*—A novel current-mode CMOS RMS-to-DC converter using translinear techniques is introduced. It is based on a Squarer/Divider cell that is implemented using an electronically simulated loop with a novel biasing scheme that allows its operation in two quadrants. The cell is designed using a differential input current and a small signal first order filter to implement the voltage averaging, leading to a compact solution that can be used with low voltage supplies. The converter has been fabricated in a standard 130 nm CMOS process, and measurement results are provided to demonstrate the feasibility of the system.**

***Index Terms*—Analog CMOS circuits, current-mode circuits, MOS translinear circuits, RMS-to-DC converters, nonlinear circuits**

I. Introduction

RMS-to-DC conversion is used in applications where information on the average energy content of an electrical signal is required. Biomedical ICs, instrumentation devices, automatic gain control, and internet of things hardware are some of these applications [1].

There are several current-mode solutions reported in the literature that perform a RMS-to-DC conversion [1-13]. Among them, it is worth mentioning those based on the dynamic translinear (TL) principle using BJT transistors [4]. However, these proposals are difficult to implement in modern standard CMOS processes, due to the poor performance of available bipolar devices. Thus, some RMS-to-DC converters based on MOS transistors operating in weak inversion region have been designed mimicking their BJT realization counterparts [5]. However, these systems suffer from low speed and large mismatch [14].

To overcome these shortcomings, RMS-to-DC converters with MOS transistors operating in strong inversion have been proposed using the generalized MOS TL (MTL) principle [15]. In such implementations, a two-quadrant Squarer/Divider (S/D) cell is preferred to avoid a full-wave rectifier at their inputs, thereby up-down MTL loops [6-8, 16] or multi-coupled MTL loops using class-AB transconductors [9] have been proposed. However, in these designs the biasing circuit is complicated and only grounded input currents are allowed, requiring doubling the circuitry to be used in differential structures and hence increasing the power consumption and area of the system. An alternative to solve these issues is the use of Electronically Simulated MTL (ES-MTL) loops. In [10], an ES-MTL loop using floating gate MOS transistors was presented. However, the system suffers from reduced bandwidth and the fact that leakage currents in modern fabrication processes preclude the correct functionality at the floating gate node. To alleviate these limitations, in [11] the voltage averaging in the ES-MTL loop was implemented using a typical CMOS common-mode sensing circuit, but this limits the voltage swing and therefore the maximum current range available.

In this Brief, a new current-mode RMS-to-DC converter designed for low-voltage applications is proposed. It is formed by a novel two-quadrant differential current S/D cell based on an ES-MTL loop, and a simple low-pass filter formed by one capacitor and one diode-connected MOS transistor. The averaging of the voltages in the ES-MTL loop is implemented using two matched metal resistors and the biasing circuit operates with an adaptive common-mode current that allows obtaining a quadratic function with a wide range and symmetry. The paper is organized as follows: Section II describes the principle of operation of the RMS-to-DC converter. In Section III, a novel S/D cell as the main building block of the converter is presented. Effects of process and temperature variations as well as mismatch are treated in Section IV. Measurement results from a fabricated prototype are introduced in Section V. Finally, conclusions are provided in Section VI.

II. Principle of Operation

A current-mode RMS-to-DC conversion is described by:

$$I_{out} = \sqrt{\langle {I_{in}}^2 \rangle} \tag{1}$$

where I_{in} and I_{out} are the input and output currents of the RMS-to-DC converter, respectively, and the operator $\langle ... \rangle$ a time averaging. A mathematically equivalent indirect or implicit approach, with improved offset performance [2], is given by

$$I_{out} = \langle {I_{in}}^2 / I_{out} \rangle \tag{2}$$

The proposed realization of the RMS-to-DC circuit is based on this indirect approach, employing a S/D cell and a Low Pass Filter (LPF) [1], as shown in Fig. 1. Note that for the S/D block a scale factor A has been added for completeness. The output

Manuscript received Jan. 8, 2019. This work was supported by Grant TEC2016-80396-C2-1-R (AEI/FEDER) and Obra Social La Caixa - Fundación Caja Navarra (Convocatoria 2018 de Captación de Talento).

M. Martincorena Arraiza, C. A. De La Cruz-Blas, J. M Algueta Miguel and A. López-Martín are with the Institute of Smart Cities, Public University of Navarre, E-31006 Pamplona, Spain (e-mail: maite.martincorena@unavarra.es).

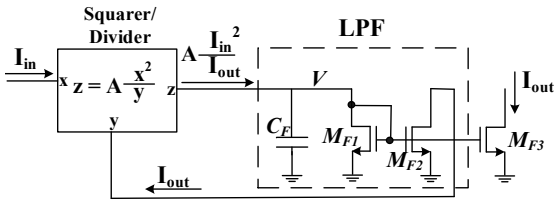

Fig. 1. Block diagram of RMS-to-DC converter.

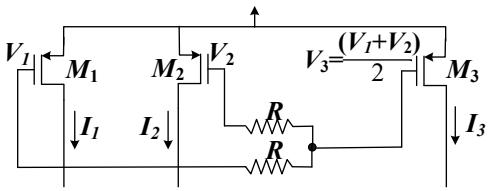

Fig. 2. Electronically Simulated MTL (ES-MTL) Loop.

current I_{out} is fed back to the S/D cell where the quotient between the squared I_{in} and I_{out} is achieved and, subsequently this signal is filtered out to obtain a DC average that corresponds to the RMS value of the input signal.

The proposed current mode LPF is formed by the diode-connected transistor M_{F1} and capacitor C_F that generates the internal voltage $V(t)$; subsequently, this voltage is converted to the output current I_{out} via transistor M_{F2}. To simplify the design, transistors M_{F1}, M_{F2}, M_{F3} have the same W/L, and thus form a small signal first-order filter with unity DC gain and a cutoff frequency of $\omega_{-3dB} = g_{mF}/C_F$. In stationary regime, the voltage V and current I_{out} will be approximately constant; therefore the small signal behavior of the filter can be used to obtain an expression that describes the dynamics of the RMS-to-DC cell. Thus applying KCL at node V:

$$A\frac{{I_{in}}^2(t)}{I_{out}(t)} = C_F\frac{\dot{I}_{out}(t)}{g_{mF2}} + \frac{I_{out}(t)}{g_{mF2}}g_{mF1} \tag{3}$$

Multiplying both sides of eqn. (3) by $2I_{out}(t)$ and noting that $g_{mF1} = g_{mF2} = g_{mF}$:

$$2A{I_{in}}^2(t) = \frac{C_F}{g_{mF}}\frac{d}{dt}({I_{out}}^2(t)) + 2{I_{out}}^2(t) \tag{4}$$

Rearranging and solving for I_{out}, the RMS value in stationary regime of $I_{in}(t)$ can be expressed as [2]:

$$I_{out}(t) = \sqrt{2A\frac{g_{mF}}{C_F}\int_0^t {I_{in}}^2(\tau)e^{-2\left(\frac{g_{mF}}{C_F}\right)(\tau-t)}d\tau} \tag{5}$$

In order to describe the complete dynamic of the RMS-DC converter, Equation (4) must be modified as:

$$A{I_{in}}^2(t) = \frac{C_F}{2}\sqrt{\frac{I_{out}(t)}{k}}\frac{dI_{out}(t)}{dt} + {I_{out}}^2(t) \tag{6}$$

Equation (6) is derived assuming that the I-V characteristic of the MOS transistor is $I_{out}(t) = I_{d,M_{F1}}(t) = k(V(t) - V_{th})^2$, with $k = \frac{1}{2}\mu C_{ox}(W/L)$ and V_{th} the threshold voltage. Unfortunately, (6) does not have an analytical solution, and requires numerical methods to find the solution.

III. Novel Squarer/Divider Cell

The proposed S/D cell is based on an ES-MTL loop. A MTL circuit is formed by connecting the gate and source terminals of an even number of MOS transistors forming a loop. This way the V_{GS} voltages of these transistors add or subtract in the loop. Assuming that transistors operate in strong inversion and saturation, this leads to drain currents related by sums of their square-root values. This relationship can be easily exploited forcing linear combinations of drain currents that, when attached to the MTL circuit, can generate current-mode nonlinear functions such as multiplication, square root, S/D, etc. The most commonly used MTL cell is that formed by four transistors arranged in stacked, up down, or ES topologies. In the ES-MTL arrangement, some sums of V_{GS} voltages are generated electronically, simplifying the design and allowing an odd number of MOS transistors. To the best of the authors' knowledge, only practical ES-MTL circuits with three transistors have been reported [10-13]. In the following paragraphs, a novel ES-MTL circuit will be introduced featuring simplicity, compactness, and allowing differential input currents.

In Fig. 2, an ES-MTL cell composed by three matched PMOS transistors M_1, M_2, and M_3 is shown. Considering that the transistors are operating in strong inversion and saturation, and using the square-law model, their drain currents are given by $I_i = k_i(V_{GS} - V_{th})^2$ for *i* from 1 to 3, with $k_1 = k_2 = k_3$. In this case, the relationship among their gate-to-source voltages is V_{GS3}=$(V_{GS1} + V_{GS2})/2$, since the resistors R yield the average (common-mode) voltage of V_1 and V_2 at the gate of M_3. Thus, expressing the gate-source voltages as a function of the drain currents and substituting them in the above equation, the following expression relating the drain currents in the ES-MTL circuit of Fig. 2 is obtained:

$$\sqrt{I_1} + \sqrt{I_2} = 2\sqrt{I_3} \tag{7}$$

A S/D cell is obtained if I_1, I_2 and I_3 are forced to be:

$$I_1 = I_{CM} - I_{in};\ I_2 = I_{CM} + I_{in};\ I_3 = I_d \tag{8}$$

In this case, squaring both sides of the equation (7) and operating,

$$\sqrt{{I_{CM}}^2 - {I_{in}}^2} = 2I_d - I_{CM} \tag{9}$$

squaring again and solving for I_{CM},

$$I_{CM} = ({I_{in}}^2/4I_d) + I_d \tag{10}$$

where factor A= 1/4 (see Fig. 1). The S/D cell can be obtained easily subtracting I_d from (10),

$$I_{out} = I_{CM} - I_d = {I_{in}}^2/4I_d \tag{11}$$

Note by replacing (10) in (8) that there is no restriction for I_{in} to keep transistors M_1 and M_2 on, since due to their quadratic relationship with I_{in}, I_1 and I_2 will always remain positive enforcing operation in two quadrants with a large output range.

In Fig. 3, the novel S/D circuit is shown where the main ES-MTL cell, formed by M_1-M_2 and M_3, is biased using two Flipped Voltage Followers (FVF) [17] M_6-M_{C6} and M_7-M_{C7}, respectively. Here, the bias currents I_d at the drain terminals of M_{C6} and M_{C7} are injected using cascode current mirrors and a reference bias voltage V_{pB} is set. Note that due to the very low impedance at the output of FVFs (which makes this node ideally a signal ground), the circuit is equivalent to that of Fig. 2 and the MTL principle is not modified, since the same voltage at the source of M_1-M_3 as in Fig. 2 is obtained. This biasing

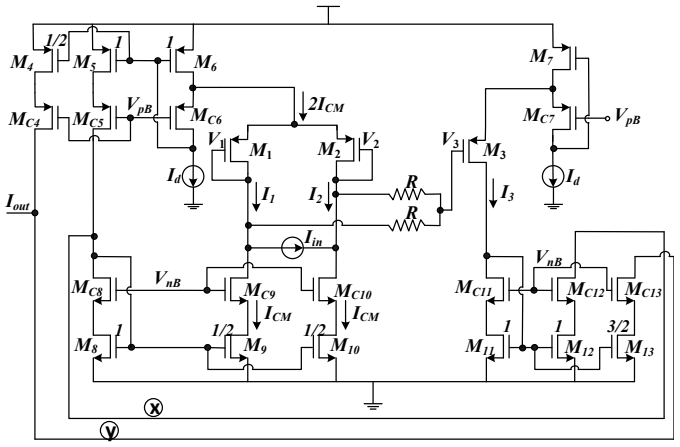

Fig. 3. Proposed squarer/divider cell.

strategy allows controlling the drain currents more efficiently and provides extra versatility, reducing the number of transistors required to implement (8).

Note from Fig. 3 that the MTL loop transistors M_1 and M_2 are diode connected to sense currents I_1 and I_2 and generate the voltages V_1 and V_2, respectively. As mentioned above, the voltage at the gate of M_3, using resistors R, is $(V_1 + V_2)/2$, performing a common mode sensing of the gate voltages of M_1 and M_2. To minimize loading effects, the values of R must be selected larger than $1/g_{m1}$ and $1/g_{m2}$, so that no significant current flows through them, guarantying the correct circuit operation.

Currents I_1 and I_2 are forced to $I_{CM} - I_{in}$ and $I_{CM} + I_{in}$, respectively, since the input current I_{in} is connected between the drains of M_1 and M_2. Note that $2I_{CM}$ is obtained via I_1+I_2 at the sources of M_1 and M_2 (see the current definitions (8)); subsequently, current I_d is added at the drain of M_6 through M_{C6} and $2I_{CM} + I_d$ is mirrored to M_5. On the other hand, M_3 is forced to drive the current $I_3 = I_d$ that is required to complete (8). Afterwards, this current is subtracted from M_5 at node X obtaining a current $2I_{CM}$ that flows through M_{c8}-M_8. This current is fed back to the input by means of properly dimensioned current mirrors M_8-M_9-M_{10} to inject the current I_{CM}. Note that the control current I_3 enforces a correct operating point, and when $I_{in} = 0$, the voltages at the gates of the three transistors M_1-M_3 forming the ES-MTL loop are equal to the bias voltage V_{pB}. When $I_{in} \neq 0$ such a current control forces a constant voltage V_{pB} at the gate of M_3 but a linear differential voltage at the gates of M_1 and M_2. Finally, the squaring/division equation (11) is obtained subtracting $(3/2)\, I_d$ from $(2I_{CM} + I_d)/2$ at node Y by the M_{11}-M_{13} mirror.

IV. PVT Variations and Mismatch Effects

As CMOS technology scales down, the unwanted effects of PVT variations and mismatch become more significant, demanding to explore how robust the designs are against this issue. In TL circuits PVT variations are less relevant than mismatch [15]. Thus, in this Section, analytical expressions are mainly focused on the impact of mismatch on the proposed design. The Section ends with Monte Carlo and temperature simulations to explore both PVT and mismatch effects.

There are two main types of mismatch that can affect the MOS transistor namely, mismatch on the threshold voltage V_{th} (the most significant one) and on the W/L ratios [15]. To include all the mismatch sources in the TL loop, transistors M_{C6} and M_{C7} are also considered, since they set the source voltage of transistor M_1-M_3. Thus, the TL loop equation is modified to $V_{GS3} = V_{GSc7} - V_{GSc6} + (V_{GS1} + V_{GS2})/2$ resulting in:

$$\sqrt{\frac{I_{CM}-I_{in}}{1}} + \sqrt{\frac{I_{CM}+I_{in}}{1+\Delta_2}} + \sqrt{k_1}\Delta V_{th} = 2\left(\sqrt{\frac{I_d}{1+\Delta_3}} + \sqrt{\frac{I_d}{1+\Delta_{C6}}} - \sqrt{\frac{I_d}{1+\Delta_{C7}}}\right), \tag{12}$$

where $\Delta V_{th} = V_{th,1} + V_{th,2} + 2V_{th,C7} - 2V_{th,3} - 2V_{th,C6}$. The deviations of k_i, (for i =2, 3, C6 and C7) with respect to k_1 are defined by $k_i = k_1 + \delta k_i$, leading to dimensionless constants $\Delta_i = \delta k_i / k_1$ in (12).

To provide more insight into the design, a study is realized independently for each type of mismatch. For the case of the variations of V_{th}, it is considered that $\Delta_i = 0$. Now solving (12) for I_{CM} results:

$$I_{CM} = \frac{{I_{in}}^2}{(-2\sqrt{I_d} + \sqrt{k_1}\Delta V_{th})^2} + \frac{1}{4}(-2\sqrt{I_d} + \sqrt{k_1}\Delta V_{th})^2 \tag{13}$$

Note that, comparing with (10), mismatch in the threshold voltages causes an offset and a scaling factor in ${I_{in}}^2$, which can be partially compensated by the current I_d. However, the quadratic characteristic is unaffected. On the other hand, considering $\Delta V_{th} = 0$, mismatch in the W/L ratios and consequently in k_i, leads to:

$$I_{CM} \approx \frac{\frac{{I_{in}}^2}{1+\Delta_2} + 4{I_d}^2 + 2I_d\Delta_2 I_{in}}{\sqrt{4{I_{in}}^2\frac{\Delta_2}{1+\Delta_2} + \frac{16{I_d}^2}{1+\Delta_2} - \frac{8I_d\, I_{in}\, \Delta_2}{1+\Delta_2}}} \tag{14}$$

Equation (14) is derived only considering first order terms and neglecting higher order ones for clarity. Mismatch between M_1 and M_2 introduces additional terms in both the denominator and numerator of the expression of I_{CM} when it is compared with (10). Equation (14) shows that mismatch with M_3, M_{C6}, and M_{C7} is not relevant (at least in a first order approximation), and special layout techniques should focus on the other transistors. Note that from (13) and (14), without mismatch, i.e. $\Delta V_{th} = 0$ and $\Delta k_2 = 0$, both equations reduce to (10) as expected.

Finally, simulations including mismatch/process variations via Monte Carlo and temperature drift are provided in Fig. 4. A Monte Carlo analysis [18] was performed using Spectre with 1000 runs. A DC sweep of I_{in} from -30 µA to 30 µA was chosen, with $I_d = 6$ µA. The simulation results are shown in Fig. 4 (a) using a box plot [19] for each value of the input current. In each box plot, the line in the middle of the box represents the median of the output current (50th percentile); the bottom and top edges of the box indicate the 25th and 75th percentiles, respectively. The whiskers are represented as dashed lines extending vertically from the boxes and ended with a horizontal dash that represents the 2.5·(75th percentile) - 1.5·(25th percentile) and 2.5·(25th percentile) - 1.5·(75th percentile) for the top and bottom dash, respectively. The

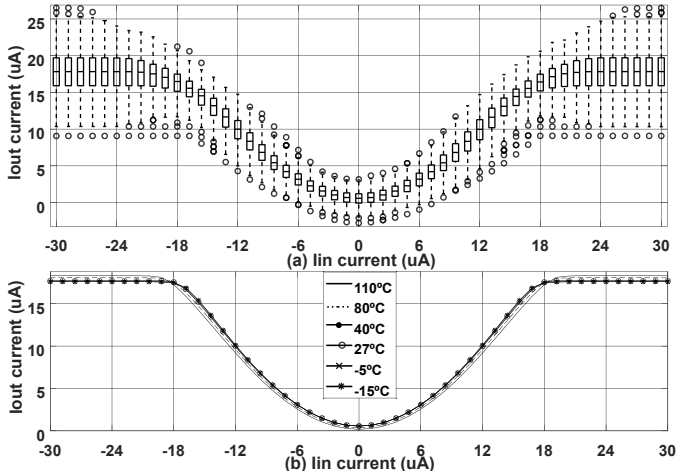

Fig. 4. Simulation results of the squarer/divider cell with $I_d = 6\ \mu A$ (a) Monte Carlo mismatch/process simulation; (b) Temperature variations.

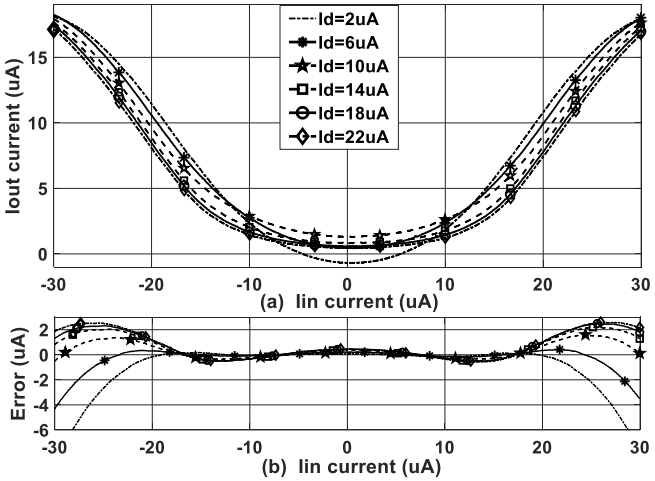

Fig. 5. (a) Measured output currents of the squarer/divider cell for a sweep of the input current and different I_d; (b) Error with an ideal squarer function.

outliers are shown by circles (o) and they are values outside of the whiskers.

Fig. 4 (b) shows simulations at different temperatures using the same currents as in Fig. 4(a). Note that the output current is not affected significantly, obtaining relative errors with respect to room temperature of 0.03%, 0.17%, -4.88% and -9.84% for temperatures of -15ºC, -5ºC, 80ºC and 110ºC, respectively.

As can be seen from Fig. 4 (a) and (b), the output current tendency is a squarer function for input currents from -18 µA to 18 µA, also in this zone the whiskers and outliers are practically the same. Out of this range, the output current is saturated and the proposed cell is not working properly. In the following Section, measurement results from a fabricated prototype are shown which are consistent with the simulated data of Fig. 4.

TABLE I
TRANSISTOR ASPECT RATIOS IN FIG. 2.

	M_{1-3}	M_4	M_{5-7}	M_{C4-C7}	$M_{8-11-12}$	M_{9-10}	M_{13}	M_{C8-C13}
L (µm)	0.51	0.31	0.31	0.51	0.5	0.5	0.5	0.5
W (µm)	12	0.5	1	12	6	3	9	6

V. MEASUREMENT RESULTS

The proposed RMS-to-DC converter was fabricated in a GlobalFoundries 130 nm 8-metal CMOS technology with $V_{th} \cong 0.25\,V$. A 100 nF external capacitor was employed to implement C_F and the value of R was 150 kΩ, V_{DD} was 1.2 V and bias voltages V_{pB} and V_{nB} were set to 0.5 V. Dimensions for the transistors forming the S/D cell are shown in Table I. The value of $1/g_{m1,2}$ for the operating current values is around 15 kΩ that is lower than the value of R=150 kΩ guarantying the correct voltage averaging at the gate of M_3. The total chip area of the circuit is 0.0025 mm^2, approximately.

The input signal was provided by the Agilent 33522A Waveform Generator and converted to a differential current through an external differential Mirrored Modified Howland current source composed of two Analog Devices AMP03 precision unity-gain differential amplifiers whose differential output voltages where converted to currents via TL082CN operational amplifiers and 100 kΩ resistors. The output currents of the circuits were externally converted to voltage via transresistance amplifiers made by a TL082 operational amplifier and a 100 kΩ resistor in negative feedback configuration. First the output characteristic of the S/D cell will be tested and subsequently the complete RMS-to-DC converter.

The measured output current of the S/D cell for different input currents and different values of I_d is shown in Fig. 5 (a). Note that the output current begins to saturate for input currents larger than 20 µA. Although the FVFs in Fig. 3 provide class AB operation, transistors M_{C9} and M_{C10} enter triode region for these currents, due to the large drain currents driven by M_1 and M_2 decreasing the voltages V_1 and V_2, respectively. Note also that for $I_d = 6$ µA, the measurement results are in good agreement with Fig. 4 (a) since they fall outside the boxes of the sample but inside the whiskers or outliers. Thus, owing to process variations the measured results show larger input range, but smaller output range than the median value (the designed input-output ranges).

In order to validate the accuracy of the S/D circuit response, an error plot, defined as the difference between the output current of the S/D cell and an ideal squarer function generated by the "Curve Fitting" function in Matlab, is shown in Fig. 5 (b). The plot is for different values of I_d, and it shows that the error is lower than 1 µA for input currents up to 20 µA, with a total input range of 10- 44 µA with a ±10% error, corresponding to a relative error of ±3% for output currents ranging from 1 µA to 10 µA with $I_d \leq 6$ µA. Also, note that the output current is affected by scaling and offset errors. These effects can be mainly attributed to the V_{th} mismatch, as is predicted by (13).

To verify the correct operation of the RMS-to-DC converter, measurement results with a 1 kHz unipolar square input signal of amplitude 15 µA with different duty cycles were obtained. Fig. 6 (a) shows the measured transient response of I_{out} for a 60% duty cycle of the input signal, and Fig. 6 (b) shows I_{out} and its relative error, as defined in (15), for different duty cycles of the input signal. The output current I_{out} is approximately proportional to the square root of the duty cycle as expected [7] with errors lower than ±5 %. These variations are mainly due to saturation of output current for small duty cycles and inaccuracy of the square/divider cell for large duty cycles.

$$Error = \frac{calculated - measured}{calculated} \times 100\% \qquad (15)$$

TABLE II
COMPARISON WITH PREVIOUS RMS-TO-DC CONVERTERS

	[9]	[10]	[5]	[6]	[7]	This work
Basic principle	Class-AB transconductance	SDR FG-MOS	Log-domain FG-MOS	MTL loop	MTL cell (SCMC)	ES-MTL principle
Technology	0.5 µm	0.6 µm	0.35 µm	0.18 µm	0.5 µm	0.13 µm
Voltage Supply	1.5 V	1.2 V	0.9 V	1.2 V	2.5 - 5 V	1.2 V
Transistor number	40	14 MOS + 1 FG	7 MOS + 6 FG	18	18	16
Verification type	Fabrication	Simulation	Simulation	Simulation	Fabrication	Fabrication
Operation area of input	1 quadrant	2 quadrants	2 quadrants	2 quadrants	2 quadrants	2 quadrants
Static Power	-	-	-	< 100 µW	> 88 µW	68.8 µW (I_d = 6 µA)
Silicon Area	0.1 mm^2	-	-	-	0.064 mm^2	0.0025 mm^2
Relative error at input range	10% @ 11-28 µA	3% @ 5-30 µA	2% @ 0.6-400 nA	6% @ 2-32 µA	3% @ 200-390 µA	10% @ 10-44 µA
Maximum input frequency	-			-	> 2MHz	3 MHz *

* Maximum frequency of the S/D's input signal.

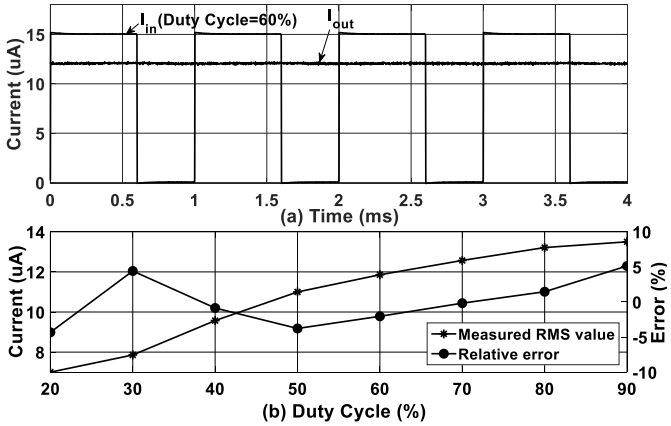

Fig. 6. (a) Measured output current of the RMS-to-DC converter for a rectangular input signal with 60% duty cycle; (b) Measured output current and relative error of the for different duty cycles of the rectangular input signal.

Table II shows a comparison with previous proposals. Even though the comparison is difficult due to the differences between simulation and measurement results, the proposed circuit is competitive with former works allowing a large differential output range and avoiding floating gates that are prone to suffer from leakage currents in modern CMOS fabrications processes. The LPF simplicity and the fact that all S/D internal nodes have low impedance allows relatively large input frequency (which is difficult to get in implicit RMS-to-DC converters due to feedback). The S/D load is the main limiting factor, so larger $1/g_{mF1}$ and C_F reduce the maximum input frequency but also reduce the output ripple [2], leading to a tradeoff between speed and averaging performance.

VI. CONCLUSION

A 1.2 V two-quadrant RMS-to-DC converter has been presented. The resulting circuit features a simple yet novel structure composed of a S/D cell, based on the ES-MTL principle with internal common mode generation allowing a differential input current, and a simple current-mode LPF. Mismatch effects analyzed via derived analytical expressions and Monte Carlo simulations are provided to explore the robustness of the cell. Measurement results of a 130 nm CMOS test chip prototype demonstrate the symmetry and wide input range of the circuit.

REFERENCES

[1] C. Kitchin and L. Counts, *RMS to DC Conversion Applications Guide*, 2nd ed. Dallas, TX: Analog Devices, 1986.
[2] D. R. Frey, "Exact analysis of implicit RMS converters," *Electron. Lett.*, vol. 40, no. 5, pp. 1455–1456, Mar. 2004.
[3] R. Vargas-Bernal and C. De la Cruz Blas, "A Survey on the Static and Dynamic Translinear Paradigm". In: *Integrated Circuits for Analog Signal Processing*. New York, NY: Springer, 2013.
[4] J. Mulder, A. Van der Woerd, W. Serdijn and A. Van Roermund, "An RMS-DC converter based on the dynamic translinear principle", IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1146-1150, 1997.
[5] E. Farshidi and S. M. Sayedi, "A micropower multi decade dynamic range current-mode true RMS-to-DC converter," IEEE Northeast Workshop on Circuits and Systems, Montreal, Canada, 2007, pp. 1493-1496.
[6] E. Farshidi, and H. Asiaban, "A new true RMS-to-DC converter using up-down translinear loop in CMOS technology," *Analog Integrated Circuits and Signal Processing*, vol. 70, no. 3, pp 385–390, Mar. 2012.
[7] M. Shaterian, C. M. Twigg, and J. Azhari "MTL-based implementation of current-mode CMOS RMS-to-DC converters," *International Journal of Circuit Theory and Applications*, vol. 43, no. 6, pp. 793–805, Jun. 2015.
[8] A. Lopez-Martin and A. Carlosena, "A 1.5V current-mode CMOS RMS-to-DC converter," *Analog Integrated Circuits Signal Processing,* vol. 36, pp. 137-143, 2003.
[9] C. A. De La Cruz-Blas, A. Lopez-Martin, A. Carlosena and J. Ramirez-Angulo, "1.5-V current-mode CMOS true RMS-DC converter based on class-AB transconductors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 7, pp. 376-379, Jul. 2005.
[10] E. Farshidi, and S. M. Sayedi "A 1.2 V current-mode true RMS–DC converter based on the floating gate MOS translinear principle," *Microelectronics Journal,* vol. 39, no. 2, pp. 293-298, Feb. 2008.
[11] S. Vlassis, "CMOS current-mode pseudo-exponential function circuit," *Electronics Letters*, vol. 37, no. 8, pp. 471-472, Apr. 2001.
[12] E. Farshidi, "A current-mode true RMS-DC converter based on electronically simulated translinear principle," in *Proc. International Conference on Signals, Circuits and Systems*, Monastir, 2008, pp. 1-4.
[13] K. Gupta, M. Bhardwaj, B. P. Singh and R. Choudhary, "Design of Low Power Low Cost True RMS-to-DC Converter," in *Proc. 2012 Second International Conference on Advanced Computing & Communication Technologies*, Rohtak, Haryana, 2012, pp. 364-367.
[14] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer. *Analysis and Design of Analog Integrated Circuits.* 5th ed., New York, NY, USA: Wiley, 2009,
[15] R. J. Wiegerink. *Analysis and Synthesis of MOS Translinear Circuits*. Norwell MA: Kluwer 1993.
[16] C. A. De La Cruz Blas and A. Lopez, "A novel two quadrant MOS translinear Squarer-divider cell," in *Proc. 15th IEEE International Conference on Electronics, Circuits and Systems*, Malta, 2008, pp. 5-8.
[17] R. G. Carvajal et al., "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 7, pp. 1276-1291, Jul. 2005.
[18] D. P. Landau and K. Binder, *A Guide to Monte Carlo Simulations in Statistical Physics,* 3rd ed., Cambridge Univ. Press, Cambridge, UK. 2009
[19] J. W. Tukey, *Exploratory Data Analysis*. Addison-Wesley, Reading, MA. 1977, pp 39-43.