# NeSe: Near-Sensor Event-Driven Scheme for Low Power Energy Harvesting Sensors

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Abstract-Digital technologies have made it possible to deploy visual sensor nodes capable of detecting motion events in the coverage area cost-effectively. However, background subtraction, as a widely used approach, remains an intractable task due to its inability to achieve competitive accuracy and reduced computation cost simultaneously. In this paper, an effective background subtraction approach, namely NeSe, for tiny energyharvested sensors is proposed leveraging non-volatile memory (NVM). Using the developed software/hardware method, the accuracy and efficiency of event detection can be adjusted at runtime by changing the precision depending on the application's needs. Due to the near-sensor implementation of background subtraction and NVM usage, the proposed design reduces the data movement overhead while ensuring intermittent resiliency. The background is stored for a specific time interval within NVMs and compared with the next frame. If the power is cut, the background remains unchanged and is updated after the interval passes. Once the moving object is detected, the device switches to the high-powered sensor mode to capture the image.

#### I. INTRODUCTION

From energy-harvested surveillance and monitoring systems in smart cities to smart human-machine interfaces in mobile devices, smart, low-power, connected sensors are attracting increasing interest in a wide variety of applications. Moreover, our environment can be best described through vision, which is becoming increasingly ubiquitous in video monitoring applications. Human observers monitor several cameras to detect unusual activity and provide immediate feedback. Unfortunately, human observers lose 90% of their concentration capability after only 20 minutes of following ten cameras attentively, which defeats the purpose of this approach. Therefore, the automatic detection of unusual events in embedded applications is becoming increasingly significant. Machine vision applications often begin with background subtraction, making it an essential component. Inputs from background subtraction are given to higher-level processes, such as object tracking. An online video background subtraction usually consists of two stages: initialization of the background model, in which the bootstrapping is performed, and the background model's maintenance, which involves updating the parameters online. Interpreting a scene, however, requires large amounts of computing power and data-intensive vision algorithms. As they are highly parallelizable, pixel-level foreground detectors are ideal for embedded platforms. CMOS imagers with on-chip feature extraction and compression have been developed extensively in the last decade with the primary goal of optimizing computing resources and reducing overall power consumption [1]–[3].

In this work, we propose a near-sensor event-driven architecture, namely *NeSe*, allowing for a trade-off between accuracy and power efficiency. NeSe is capable of operating in different modes, 12 in total, regarding the precision and box sizes, which will be explained in the following. To the best of our knowledge, this work is the first that utilizes nonvolatile elements to store the static background, which leads to a notable reduction in standby power consumption.

## II. NEAR-SENSOR PROCESSING BACKGROUND

In the same way that eyes and brains work together, the sensors that detect the field of view generate a stream of pixels that represent the scenic event and are sent to a backend processor. Although there are 130 million pixels on the retina, the brain only has 1.3 million synaptic connections, which indicates a high sparsity ratio. This massive sparsity can significantly reduce power consumption and latency. A further improvement can be made by reducing the amount of redundant information sent to the brain. By inspiring from the observations and taking steps to mitigate the abovementioned issues, the integration of computing and sensing has been extensively studied, reducing data movement and ADC bandwidth. The research outcomes are classified into three designs, processing-near-sensor (PNS) [4], [5], processingin-sensor (PIS) [6]-[8], and finally processing-in-pixel (PIP) [9], [10]. Most computer vision systems perform background subtraction as a first step in detecting moving objects within a video stream without having prior knowledge of the objects themselves [11]. A background model is generally created during the background subtraction process. The easiest way to do this is to manually set a static image for the background that has no moving objects. Each video frame is then compared to the static image to compute the absolute difference, referred to as Static Frame Difference, and is represented by:  $|F_i - B| > TH$ . In the event of changing ambient lighting, a static image may not be the best choice since the foreground segmentation may fail completely. Alternately, the previous frame may be used instead of a static image, referred to as Frame Difference, and is expressed by:  $|F_i - F_{i-1}| > TH$ . Due to its sensitivity to threshold TH, this technique may only work properly under certain frame rates and object speeds, e.g., it fails if the moving object stops suddenly. Thus, Authors in [12] modeled the background more accurately using the average, arithmetic mean, or weighted mean of several previous frames. The equation for the past *n* frame is:  $B_j = \frac{1}{n} \sum_{i=0}^{n-1} F_{j-i}$ . In order to store more frames in off-chip memory, this model requires high memory



Fig. 1. (a) The NeSe architecture, including (b) an MRAM array and (c) a pixel. (d) Schematic and biasing of an MRAM, and (e) pixel's transient waveform. storage. Consequently, additional computations and memory voltage drops, then it subtracts the pixel reset voltage and accesses are needed, which conflict with resource-constrained converts the output signal. Accordingly, the ADC can skip

#### III. PROPOSED DESIGN

We propose NeSe as an efficient and reconfigurable alwayson intelligent visual perception architecture as shown in Fig. 1(a) that realizes a near-sensory processing scheme with event detection capabilities. NeSe consists of a  $600 \times 600$  pixel array (PA), a non-volatile Spin-Orbit Torque Magnetic Random Access Memory (SOT-MRAM) array, a row controller (Ctrl), a command decoder, a sensor timing Ctrl, a memory/computing unit, and readout/ADC/SA/comparator circuitry. The storage element in SOT-MRAM is SHE-MTJ [13] Each cell located in the MRAM array is connected with a Write Word Line (WWL), Write Bit Line (WBL), Read Word Line (RWL), Read Bit Line (RBL), and Source Line (SL). The bit-cell structure of 2T1R SOT-MRAM and its biasing conditions are shown in Fig. 1(d). The proposed architecture operates in two modes, i.e., sensing and event detection. The NeSe architecture captures the input as a static background and then writes the central pixels according to the configured settings into the MRAM cells. Due to the non-volatility feature of MRAMs, if the power of NeSe is cut, the initial background is still held. Once the moving object is detected, the architecture switches to the sensing mode to detect the object(s). To reduce the overall power consumption, NeSe only updates (sends) the modified pixels on the MRAM array.

## A. Pixel and MRAM arrays

tiny devices.

Illustrated in Fig. 1(c), conventional NeSe's pixel consists of a three-transistor/one-photodiode (PD) sensor. In the sensing mode, by initially setting Rst='high', the PD connected to the  $T_1$  transistor turns into inverse polarization and the readout component captures a  $V_1$  = VDD voltage. By turning off  $T_1$ , PD generates a photo-current with respect to the external light intensity which in turn leads to a voltage drop ( $V_{PD}$ ) at the gate of  $T_2$ . Therefore, the voltage values before and after the image light exposure, i.e.,  $V_1$  and  $V_2$ , are sampled by the readout circuit, and the difference between the two voltages is sensed, amplified, and then converted to digital data by an ADC. This value is proportional to the voltage drop on  $V_{PD}$ . Figure 1(e) depicts the functionality of one proposed pixel. It is worth pointing out that each ADC samples when the

voltage drops, then it subtracts the pixel reset voltage and converts the output signal. Accordingly, the ADC can skip to the next row of the array. NeSe is equipped by a nearsensor CMOS bit-wise XNOR comparator, as shown in Fig. 1(a), to efficiently compare such row-wise digitized pixel data with the corresponding captured background in the MRAM array to detect events. To enable this, one row of the MRAM array, shown in Fig. 1(b), is selected, sensed out, and loaded as the first operand into a register at the comparator where the second register is loaded by the pixel data. Accordingly, a single-cycle XNOR operation is accomplished. If a mismatch is detected, i.e., an event observed, the MRAM array holding the central pixels requires to be updated. Computationally, this stage requires n MRAM write operation. To achieve an ultrafast low-energy write operation, the SOT-MRAM cells are developed with a  $20K_bT$  energy barrier. As experimentally shown in [14], this will reduce the write energy consumption by half compared with the conventional  $40K_bT$  design at the cost of lower retention time.

## B. Event-Detection Mode

The primary task of the always-on NeSe architecture is to detect an event using background variations. NeSe supports 12 various implementations to consider both efficiency and accuracy design metrics. Different designs are determined by the *box\_size*  $\in \{3, 5, 7\}$  and *precision*  $\in \{1, 2, 3, 4\}$ , where box\_size represents height and width of defined groups, and precision denotes the bit-width of ADCs. Each  $n \times n$  pixel box includes only one ON pixel, (n-1) Disconnect pixels, and  $(n^2 - n)$  OFF pixels. An implementation with a larger box size reduces power consumption at the cost of accuracy degradation. In NeSe, each column is enabled via a distinct but common  $V_{DD}$ , and each row is chosen using a common row selector (R) signal. Thus, the ON, Disconnect, and OFF pixels are formed when R and the column are enabled, Ris disabled, but the column is enabled, and the column is disabled regardless of the R value, respectively. The R signal is valued using (nx-1), where  $n \in \{3, 5, 7\}$  and x is the row index  $\in \{1, 2, \dots, |600/n|\}$ . Consequently, all the columns without central pixels are disconnected from the power supply (OFF), while the rest of the pixels in the columns containing the central pixel is disconnected using R signal. For instance, as shown in Fig. 2, by setting box\_size to 3, all the pixels are grouped into a  $3 \times 3$  shape, where the central pixel (e.g.,



Fig. 2. Boxing pixels with the size of  $3 \times 3$  with the possible situations.  $P_{2,2}$ ) is ON, other two pixels (e.g.,  $P_{1,2}$  and  $P_{3,2}$ ) in the same column are disconnected from ADCs because of *R* values, and the rest (e.g.,  $P_{1,1}, P_{2,1}, P_{3,1}, P_{1,3}, P_{2,3}$  and  $P_{3,3}$ ) are OFF.

The power consumption and the total number of boxes regarding different box sizes are summarized in Table II. Larger box sizes (e.g.,  $7 \times 7$ ) consist of the lower number of central pixels (7396), which leads to more power saving at the cost of accuracy loss. Another reconfigurable capability of NeSe is the precision's bit-width, which defines the number of compared bits between a pixel and its previous stored value in an MRAM. A lower precision requires a smaller number of comparisons and write-back operations that decreases the power consumption but again at the cost of accuracy loss. Thus, a trade-off between efficiency and accuracy can be determined by the user w.r.t available resources, criteria, etc. Figure 3 depicts different scenarios, including various box sizes, precisions, light situations, and updating the background. First, NeSe captures Fig. 3(a) and stores it as a static background within MRAM cells. Then, an event has occurred in Fig. 3(b), and its results related to different precisions are shown. Interestingly, even 1-bit precision removes the background efficiently. Figure 3(c) illustrates the results for varied box sizes. After comparing the new input  $(t_{i+n+5})$  with the stored background at time  $t_i$ , we detect that the chair is moved, and the mug is left on the desk. A smaller box size (e.g.,  $3 \times 3$ ) provides sharper output. After a while, as shown in Fig. 3(d) time  $t_{i+2n}$ , light status changed, but NeSe functions appropriately. Finally, in Fig. 3(e), the background is updated by these pixels because the chair locations and the mug remain unchanged for a while. The comparison results using the high accuracy  $3 \times 3$  boxes exhibit no difference between Fig. 3(e) and the new background.

Algorithm1 shows all the steps, including the eventdetection and sensing modes provided by the NeSe architec-

 TABLE I

 EFFECT OF BOX SIZE IN NESE PROPERTIES.

Box	# Transistors			Power	# Doweg
Size	ON	OFF	Disconnected	$(\mu W)$	# DOXES
$3 \times 3$	1	6	2	1.31	40000
$5 \times 5$	1	20	4	1.48	14400
$7 \times 7$	1	42	6	1.64	7396

## Algorithm 1 NeSe Algorithm

1:	<b>Input<sub>2</sub>:</b> $box\_size \in \{3, 5, 7\}$ & $precision \in \{1, 2, 3, 4\}$ -bit						
2:	: Input <sub>3</sub> : threshold <sub>nixels</sub> , $time_{\tau}$						
3:	<b>Output:</b> sensor_mode status						
4:	$turn_on_list = []$						
5:	procedure EVENT-DETECTION						
6:	if time $\geq time_{\tau}$ : $\triangleright$ Merge steady objects with the background.						
7:	update (background)						
8:	for $i = \left \frac{box\_size}{2}\right  + 1$ to 600 with step= $box\_size$						
9:	activate (row <sub>i</sub> )						
10:	pixel_values $\leftarrow parallel_read$ (column <sub>i,j</sub> ) $\triangleright$						
	$j \in \{\lfloor \frac{box\_size}{2} \rfloor + 1, \dots, 600\}$ , with step= box_size						
11:	num_changes $\leftarrow$ <b>parallel_comp</b> ( <i>precision</i> , pixel_values, old_values)						
12:	if num_changes $\geq$ threshold <sub>pixels</sub> :						
13:	turn_on_list. <b>push</b> (i) $\triangleright$ i is row index.						
14:	if (length (turn_on_list) !=0)						
15:	time $+= 1$ $\triangleright$ Use it to update the background.						
16:	enable SENSOR MODE						
17:	else:						
18:	time = $0$						
19:	end procedure						
20:	procedure Sensor Mode						
21:	while (length (turn_on_list) !=0) do						
22:	$row = turn_on_list.pop$						
23:	$\texttt{transfer} (row - \lfloor box\_size \rfloor \texttt{to} row + \lfloor box\_size \rfloor)$						
24:	end while						
25:	end procedure						

ture. The algorithm takes the size of the box, precision, and two thresholds, threshold<sub>pixels</sub>, and time<sub> $\tau$ </sub>. The former is used for minimum changes, whereas the latter is leveraged to update the background. First, every row containing a central pixel, line (9), is activated, and the parallel comparison is performed in line 11 between all the central values and the previous value of the same pixel. The **parallel comp** function takes the precision, which determines the required number of compared bits. For example, if precision = 1, only the most significant bits of pixels are compared. In line 12, if the number of changes is greater than or equal to threshold<sub>pixels</sub>, the row index is held in the turn\_on\_list. After checking all rows, the length of the turn\_on array is checked. In the case of non-equality to zero, the mode is changed to the sensor mode, and the time counter is increased by one. This variable indicates how many times NeSe is switched to sensor mode continuously. If this variable reaches time<sub> $\tau$ </sub>, we need to update the background with the new values (line 7). As shown in Fig.3(e), after updating the background to (d), most of the compared pixels are black.

### C. Sensing Mode

In the sensing mode, all the enabled columns, connected to  $V_{dd}$ , and rows based on the R signal are connected to ADCs. We assume that the background has already been stored in the co-processor, e.g., digital on-chip deep learning accelerator. Thus, in the sensing mode, only row indices in the  $turn_on_list$  should be updated instead of all rows, which results in a considerable power saving.

#### **IV. PERFORMANCE EVALUATION**

# A. Power Consumption

Table II reports the power consumption for event detection, i.e., to detect a mismatch between a digitized pixel value and the pre-stored background in MRAM cells assuming two different ADC precisions. The total power consumption for the central pixel comparison can be estimated by  $P_{total} = P_{pixel} + P_{MRAM} + P_{compare}$ , where  $P_{pixel}$  represents the pixel sensing



Fig. 3. Detecting object timeframes using NeSe, (a)  $\rightarrow$ (b) detects a person leveraging different precision (1 to 4 bit), (a)  $\rightarrow$ (c) calculates differences in the images based on different box sizes, (c)  $\rightarrow$ (d) detects light variation as a new object, and (d)  $\rightarrow$ (e) updates new background.

power that largely depends on the ADC precision.  $P_{MRAM}$ is the SOT-MRAM's read power and  $P_{compare}$  denotes the power consumed by the near-sensor CMOS bit-wise XNOR comparator. Assuming a 2-bit ADC structure, every central pixel after readout has to be compared with two SOT-MRAM cells holding the background value. This means  $2 \times P_{MRAM}$ are considered in the evaluations. We observe that the higher the ADC precision is (here from 4-bit to 2-bit), the higher power budget is required for the edge device to perform such a near-sensor computation and within a particular ADC precision, the larger box size brings higher power efficiency to the system at the cost of lower accuracy as discussed above.

### B. Intermittent-Robust Operation

Power supplies in energy harvesting systems are limited in capacity. Besides, a CMOS-based design loses data when powered down, so restoring (writing back) information after a new power-up consumes power and time. Energy harvesting devices may undergo a charge/discharge cycle hundreds of times per second, which means the system might consume a significant portion of its entire power supply capacity to restore data. Although NV-MRAMs provide power failure tolerant designs, the required power consumption of write operations for non-volatile elements remains an issue. Thermal barriers between 40 - 60 kT are generally chosen for MRAM to provide a retention time ( $\tau = \tau_0 exp(\Delta/kT)$ ) of 10-15 years, while the critical spin-current is linearly proportional to the thermal barrier  $\Delta$ . Thus, for our application that does not require retention times of years, we reduce the thermal barrier of nanomagnets by means of uniaxial anisotropy. Herein, MRAM components with 20kT energy barriers are investigated that can achieve retention times ranging from minutes to hours while providing at least 75% energy reduction. By reducing the charge currents required for the write operation, significant

 TABLE II

 POWER CONSUMPTION FOR EVENT DETECTION W.R.T. ADC PRECISION.

Box size	3×3	5×5	7×7
# of XNOR (2-bit ADC)	80,000	28,800	14,792
Power (mW)	842	561.3	374.2
# of XNOR (4-bit ADC)	160,000	57,600	29,584
Power (mW)	1,852.4	1,234.9	823.2

energy savings can be achieved due to a quadratic relationship between the Ohmic  $(I^2R)$  losses and the input write currents.

## V. CONCLUSION

This paper proposed a practical background subtraction approach, NeSe, for tiny energy-harvested sensors leveraging MRAMs. NeSe allows the accuracy and efficiency of event detection to be adjusted at runtime based on the application's requirements. Furthermore, the proposed design reduces data movement overhead due to the near-sensor implementation of background subtraction. Moreover, MRAMs ensure intermittent resiliency, meaning if the power is cut, the background remains unchanged. Finally, if the moving object is detected, the device switches to the high-powered sensor mode.

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#### REFERENCES

- F. D. Oliveira *et al.*, "Cmos imager with focal-plane analog image compression combining dpcm and vq," *IEEE TCASI*, vol. 60, no. 5, pp. 1331–1344, 2013.
- [2] I. Cevik and S. U. Ay, "An ultra-low power energy harvesting and imaging (ehi) type cmos aps imager with self-power capability," *IEEE TCASI*, vol. 62, no. 9, pp. 2177–2186, 2015.
- [3] N. Cottini *et al.*, "A  $33 \ \mu w \ 64 \times 64$  pixel vision sensor embedding robust dynamic background subtraction for event detection and scene interpretation," *IEEE JSSC*, vol. 48, no. 3, pp. 850–863, 2013.
- [4] Q. Li et al., "Ns-fdn: Near-sensor processing architecture of featureconfigurable distributed network for beyond-real-time always-on keyword spotting," *IEEE TCASI*, vol. 68, no. 5, pp. 1892–1905, 2021.
- [5] T.-H. Hsu *et al.*, "A 0.5-v real-time computational cmos image sensor with programmable kernel for feature extraction," *IEEE JSSC*, vol. 56, no. 5, pp. 1588–1596, 2020.
- [6] H. Xu *et al.*, "Utilizing direct photocurrent computation and 2d kernel scheduling to improve in-sensor-processing efficiency," in 2020 57th ACM/IEEE DAC. IEEE, 2020, pp. 1–6.
- [7] S. Angizi *et al.*, "Pisa: A binary-weight processing-in-sensor accelerator for edge image processing," *arXiv preprint arXiv:2202.09035*, 2022.
- [8] M. Abedin *et al.*, "Mr-pipa: An integrated multi-level rram (hfo x) based processing-in-pixel accelerator," *IEEE JXCDC*, 2022.
- [9] H. Xu *et al.*, "Macsen: A processing-in-sensor architecture integrating mac operations into image sensor for ultra-low-power bnn-based intelligent visual perception," *IEEE TCASII*, vol. 68, no. 2, pp. 627–631, 2020.
- [10] S. Tabrizchi et al., "Ocelli: Efficient processing-in-pixel array enabling edge inference of ternary neural networks," *JLPEA*, vol. 12, no. 4, p. 57, 2022.

- [11] B. Garcia-Garcia et al., "Background subtraction in real applications: Challenges, current models and future directions," Computer Science *Review*, vol. 35, p. 100204, 2020.[12] A. H. Lai and N. H. Yung, "A fast and accurate scoreboard algorithm
- [12] A. H. La and N. H. Yung, A fast and accurate scoreboard algorithm for estimating stationary backgrounds in an image sequence," in *1998 IEEE ISCAS*, vol. 4. IEEE, 1998, pp. 241–244.
  [13] X. Fong *et al.*, "Spin-transfer torque devices for logic and memory: Prospects and perspectives," *IEEE TCAD*, vol. 35, no. 1, pp. 1–22, 2015.
  [14] A. Roohi and R. F. DeMara, "NV-Clustering: Normally-Off Computing Using Non-Volatile Datapaths," *IEEE TC*, vol. 67, no. 7, pp. 949–959, Vol. 2016.
- July 2018.